ML7396A/B/E

Sub GHz band short range wireless transceiver IC

■GENERAL DESCRIPTION

The ML7396 family (ML7396A (915MHz band), ML7396B (920MHz band), and ML7396E (868MHz band)) are ICs for transmitting/receiving data which integrate the RF, IF, MODEM and HOST interface sections into one chip for the specified low power radio communication. The ML7396 family is used for FCC PART15, ARIB STD-108(specified low-power radio station, 920MHz-band telemeter, telecontrol and data transmission radio equipment), ETSI EN 300 220 compliant radio station, and uses a packet transmission function of IEEE802.15.4d and IEEE802.15.4g.

■FEATURES

- Compliant to ARIB STD T-108 (ML7396B)
- Compliant to FCC Part15 (ML7396A)
- Compliant to ARIB STD T-108 ETSI EN 300-220 (ML7396E)
- High accurate modulation implemented by direct modulation scheme using fractional-N PLL.
- Modulation : GFSK / GMSK, FSK / MSK
  (MSK is FSK transmission of modulation degree: m=0.5)
- Data rates: 10 / 20 / 40 / 50 / 100 / 150 / 200 kbps and 400 kbps(option)
- Data coding: NRZ and Manchester codes
- Applicated channel filter suited to data transmission speed
- Programmable modulation frequency shift
- Polar conversion for TX and RX data bits
- 36MHz oscillator
- TCXO direct inputs available
- load capacitance control function of oscillation circuit
- Frequency trimming function (frequency fine tuning by oscillation circuit and fractional-N PLL)
- Host interface: SPI
- Built-in power amplifier (PA) with output power control function
  (output power select function among 20mW/10mW/1mW, trimming function)
- External PA control
- Receive Signal Strength Indicator (RSSI) reporting function and threshold comparison function
- AFC function at RX
- Support 2 antenna diversity
- Test pattern generator(PN9, CW, 01 pattern, all-1s, all-0s)
- FEC function
- IEEE802.15.4d/g support
  - Separate 256-byte TX and RX buffers
  - Max packet length 2047Byte（IEEE802.15.4g case）
  - Preamble pattern detection function (Preamble length can be prgrammable between 1 to 15 Byte）
  - Programmable TX preamble length（Max 255 Byte）
  - SFD detection function (Max 4 Byte, available for TX and RX)
  - CRC function（CRC32, CRC16-IBM, CRC16, CRC8 or no-CRC）
  - Whitening function
  - Address filtering function
  - Automatic Acknowledge (Ack TX or RX) function
  - FEC function (with IEEE802.15.4g mode)

- Power supply: 1.8 to 3.6V (TX power 1mW mode)
  2.3 to 3.6V (TX power 10mW mode)
  2.6 to 3.6V (TX power 20mW mode)
- Operating temperature: -40 to +85 deg.C
- Power consumption (920MHz)

Sleep mode		0.9 μA (Typ.) (registor value retention)
Idle mode		1.4mA (Typ.)
TX	20mW	32 mA (Typ.)
	10mW	24 mA (Typ.)
	1mW	13 mA (Typ.)
RX		15 mA (Typ.) (@100kbps)

- Package
  40 pin WQFN P-WQFN40-0606-0.50
  Pb free, RoHS compliant

■BLOCK DIAGRAM

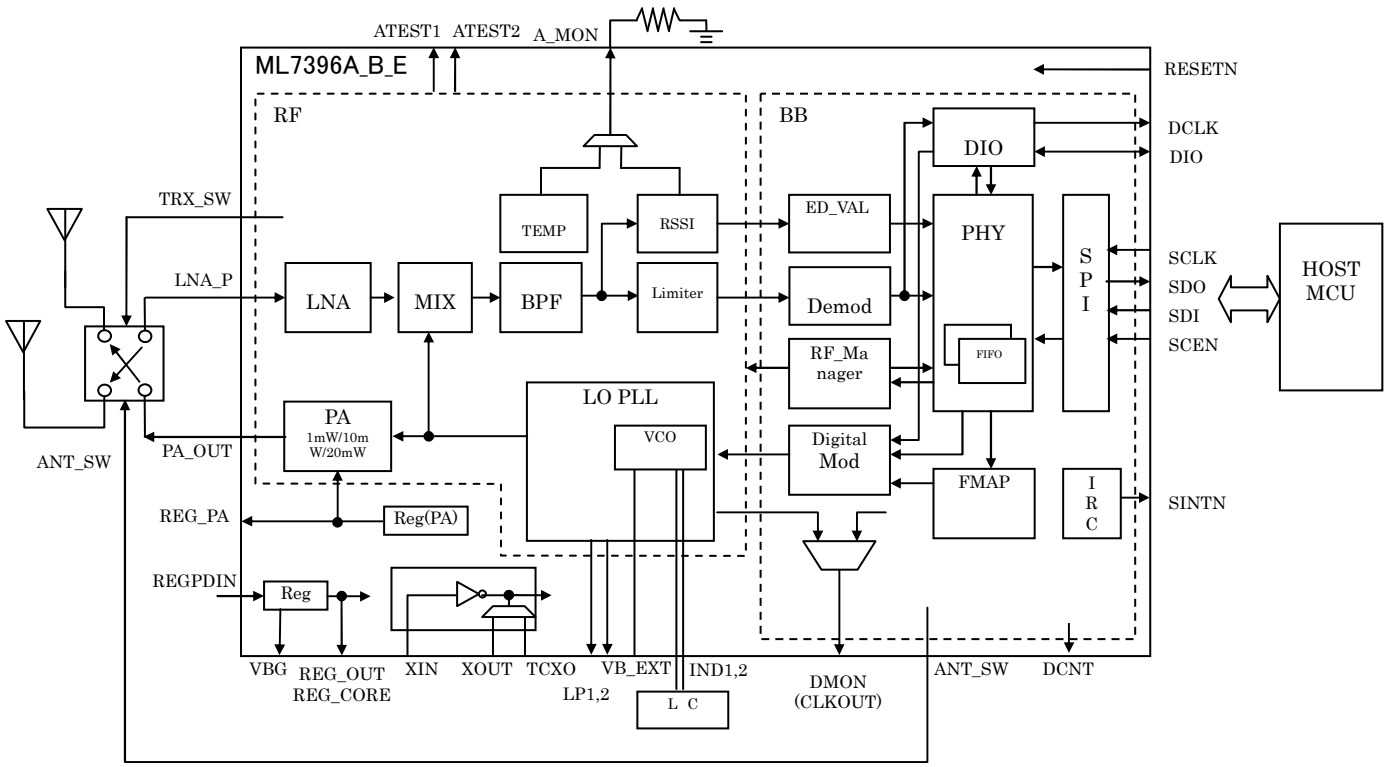
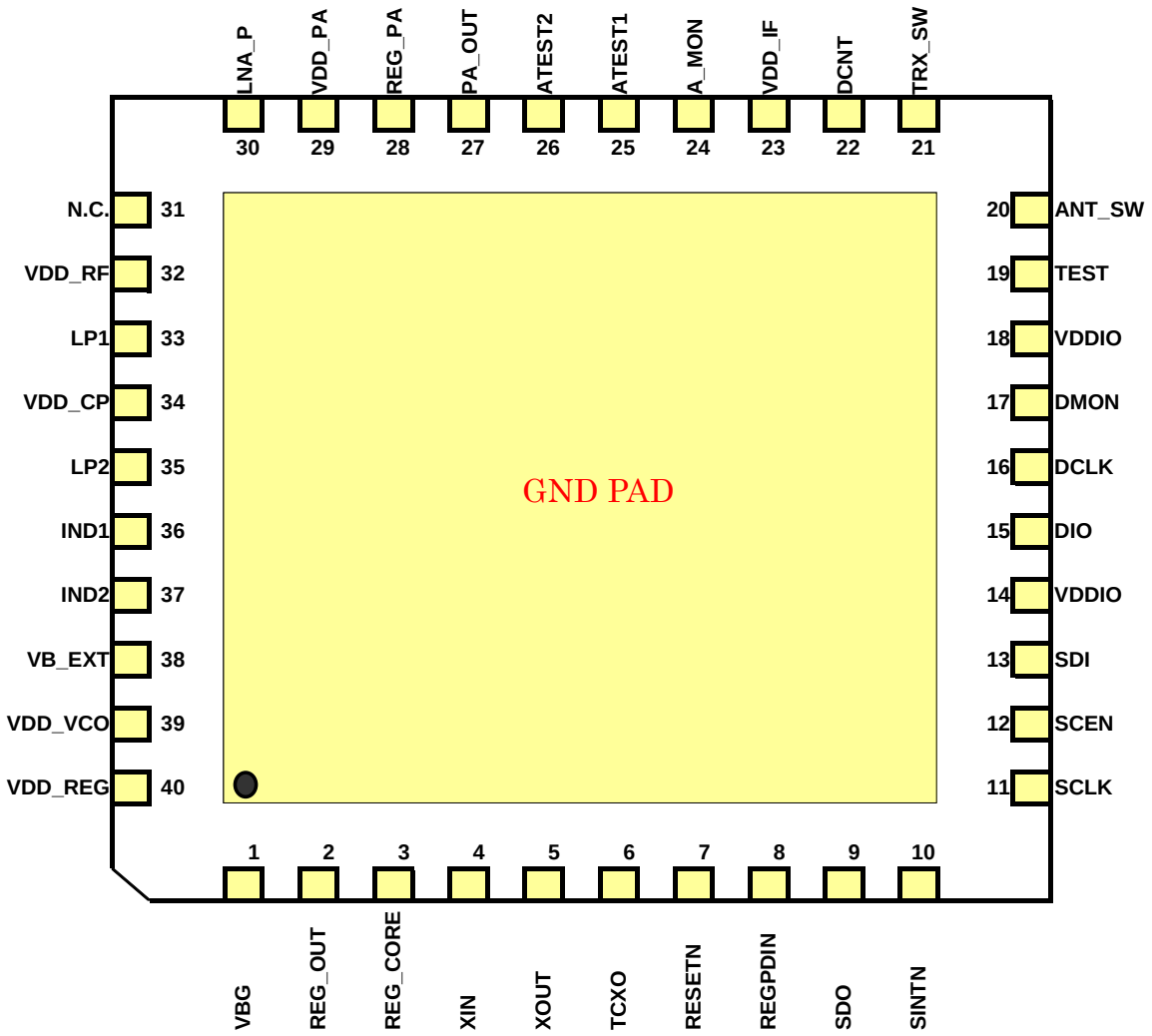


Fig.2-1 Block diagram

■PIN ASSIGNMENT

●Pin Location



NOTE) Pattern shown in the centre of the chip is located at bottom side of the chip (GND PAD)

■PIN DEFINITION

Symbols

I_{RF} : RF input
O_{RF} : RF output
I_A : Analog input
I_{OS} : Oscillator input
O_{OS} : Oscillator output
I : Digital input
O : Digital output
Is : Shmidt Trigger input

●RF part

Pin name	Pin No	Direction	Active Level	Dir/state at reset	Detail function
LNA_P	30	I_{RF}	-	I	RF antenna input
PA_OUT	27	O_{RF}	-	O	RF antenna output
IND1	36	-	-	-/-	Pin for external inductor
IND2	37	-	-	-/-	Pin for external inductor
LP1	33	-	-	-/-	Pin for PLL loop filter
VB_EXT	38	-	-	-/-	Pin for capacitor averaging internal bias
ATEST1	25	O_{RF}		Hi-Z	Test pin for IF and analog test circuit. *Left open when in normal use
ATEST2	26	O_{RF}		Hi-Z	Test pin for IF and analog test circuit. *Left open when in normal use
A_MON	24	O_{RF}		Hi-Z	Test pin for analog monitor, IF block and analog test circuit*1

[Description]

*1 Analog monitor signal can be configured by register [RSSI/TEMP_OUT] address (B1 0x03), no signal assigned as default condition.

PIN DEFINITION(continued)

●SPI interface

Pin name	Pin No	Direction	Active Level	Dir/state at reset	Detail function
SCLK	11	Is	P or N	I/-	SPI clock input
SCEN	12	Is	L	I/-	SPI enable input
SDI	13	Is	H or L	I/-	SPI data input
SDO	9	O	H or L	O/L	SPI data output
SINTN	10	O	L	O/H	SPI interrupt output

●DIO interface

Pin name	Pin No	Direction	Active Level	Dir/state at reset	Detail function
DCLK	16	O	P or N	O/L	DIO clock output
DIO	15	I/O	H or L	O/L	DIO data input/output

●Regulator part

Pin name	Pin No	Direction	Active Level	Dir/state at reset	Detail function
REG_OUT	2	-	-	-/-	Regulator output（typ.1.5V） (Cap 10uF)
REG_PA	28	-	-	-/-	Regulator output for PA block
VBG	1	-	-	-/-	External Capacitor pin (Cap 0.1uF)
REGPDIN	8	I	H	I/-	Power down pin for regulator * Fix “L” when in normal use
REG_CORE	3	-	-	-/-	Monitor pin for power supplyfor digital core(typ.1.5V) (Cap 10uF)

PIN DEFINITION(continued)

●Miscellaneous

Pin name	Pin No	Direction	Active Level	Dir/state at reset	Detail function
RESETN	7	Is	L	I/L	Hardware reset
XIN	4	Ios	P or N	-	36MHz crystal pin1 *Fixed to GND level when external clock generator is used
XOUT	5	Oos	P or N	-	36MHzcristal pin2 *Fixed to GND level when external clock generator is used
TCXO	6	I_A	-	I	External clock (TCXO) input pin. *Fixed to GND level when crystal oscillator is used.
TRX_SW	21	O	H or L or OD	O/L	TX and RX switch signal (0:RX /1:TX)
ANT_SW	20	O	H or L or OD	O/L	Diversity control signal
TEST	19	I	H	I/-	Test mode input Fixed to “L” when in normal use
DMON*1	17	O	H	O/L	Monitor output pin for clock or digital signals Primary function: Clock output (6MHz) Secondary function: PLL_LD output Third function: FIFO trigger output
DCNT	22	O	H or L or OD	O/L	External PA control signal
N.C.	31,35	-	-	-	Non connection

[Description]

*1 Function of DMON pin can be selected by following condition. Clock output as a default.
Please refer to each register description for more details.
Primary function will have higher priority when multiple function are configured simultaneously.

Configuration of DMON output

Function Name	Configuration register name	Address	Bit position (bit symbol)
CLK output	CLK_SET	B0 0x02	bit4 (CLKOUT_EN)
PLL_LD output	PLL_MON/DIO_SEL	B0 0x69	bit4 (PLL_LD)
FIFO trigger output	CRC_AREA/FIFO_TRG	B0 0x77	bit0 (FIFO_TRG_EN)

●Power supply

Pin name	Pin No	Direction	Active Level	Dir/state at reset	Detail function
VDDIO	14,18	PWR	-	-/-	Power supply for digital IOs (Typ.3.3V)
VDD_REG	40	PWR	-	-/-	Power supply for regulator input (Typ.3.3V)
VDD_PA	29	PWR	-	-/-	Power supply for PA block (Typ.3.3V)
VDD_RF	32	PWR	-	-/-	Power supply for LNA,MIX blocks (Typ.1.5V)
VDD_IF	23	PWR	-	-/-	Power supply for IF block (Typ.1.5V)
VDD_VCO	39	PWR	-	-/-	Power supply for VCO block (Typ.1.5V)
VDD_CP	34	PWR	-	-/-	Power supply for Charge Pump block (Typ.1.5V)
-	EL	GND	-	-/-	GND PAD

●Unused pins

Followings are recommendation for unused pins

Pin Name	Recommendation
XOUT	Fixed to GND (When TCXO is used)
XIN	Fixed to GND(When TCXO is used)
TCXO	Fixed to GND(When Cristal OSC is used)
ATEST1	Left OPEN
ATEST2	Left OPEN
A_MON	Left OPEN
ANT_SW	Left OPEN
DMON	Left OPEN *1
DCNT	Left OPEN

*1 If not using DMON, it is necessary to stop clock out (default output on DMON) by bit4 (CLKOUT_EN) of register [CLK_SET] address (B1 0x02). Left open with enableing clock out causes the perfoemance down on RX sensitivity.

■ELECTRICAL CHARACTERISTICS

●Absolute maximum ratings

Item	Symbol	Condition	Rating	Unit
Power Supply（I/O）(*1)	V_{DDIO}	Ta=-40 to 85℃ GND=0V	-0.3 to +4.6	V
Power Supply（RF）(*2)	V_{DDRF}		-0.3 to +2.0	V
Digital Input Voltage	V_{DIN}		-0.3 to V_{DDIO}+0.3	V
RF Input Voltage	V_{RFIN}		-1.0 to +2.0	V
Analog Input Voltage	V_{AIN}		-0.3 to V_{DDIO}+0.3	V
Analog Input Voltage2 (*3)	V_{AIN2}		-0.3 to V_{DDRF}+0.3	V
TCXO Input Voltage	V_{TCXO}		-0.3 to +1.75	V
Digital Output Voltage	V_{DO}		-0.3 to V_{DDIO}+0.3	V
RF Output Voltage	V_{RFO}		-0.3 to V_{DDRF}+1.9	V
Analog Output Voltage	V_{AO}		-0.3 to V_{DDIO}+0.3	V
Analog Output Voltage2 (*4)	V_{AO2}		-0.3 to V_{DDRF}+0.3	V
Digital Input Current	I_{DI}		-10 to +10	mA
RF Input Current	I_{RF}		-2 to +2	mA
Analog Input Current	I_{AI}		-2 to +2	mA
Analog Input Current2 (*3)	I_{AI2}		-2 to +2	mA
TCXO Input Current	I_{TCXO}		-2 to +2	mA
Digital Output Current	I_{DO}		-8 to +8	mA
RF Output Current	I_{RFO}		-2 to +60	mA
Analog Output Current	I_{AO}		-2 to +2	mA
Analog Output Current2 (*4)	I_{AO2}		-2 to +2	mA
Power Dicipatin	P_d	Ta=+25℃	300	mW
Storage Temperature	T_{stg}	—	-55 to +150	deg.C

*1 VDD_IO, VDD_REG, VDD_PA pins
*2 VDD_RF, VDD_IF, VDD_VCO, VDD_CP pins
*3 XIN, TCXO pins
*4 XOUT pin

●Recommended operating conditions

Item	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply (I/O)	V_{DDIO}	VDD_IO, VDD_REG pins	1.8	3.3	3.6	V
Power Supply (PA)	V_{DDPA}	VDD_PA pin TX power <= 1mW	1.8	3.3	3.6	V
		VDD_PA pin TX power = 10mW	2.3	3.3	3.6	V
		VDD_PA pin TX power = 20mW	2.6	3.3	3.6	V
Power Supply (RF) (*3)	V_{DDRF}	VDD_RF, VDD_IF, VDD_VCO, VDD_CP pins	1.4	1.5	1.6	V
Ambient Temperature	T_a	−	-40	+25	+85	deg.C
Rising time Digital Input	T_{IR}	Digital input pins (*1)	−	−	20	Ns
Falling time Digital Input	T_{IF}	Digital Input pins (*1)	−	−	20	Ns
Output loads Digital Ouput	C_{DL}	All Digital Output pins	−	−	20	pF
36MHz Xtal frequency (Master Clock1)	F_{MCK1}	XIN, XOUT pins	-20ppm (*3)	36	+20ppm (*3)	MHz
36MHz TCXO frequency (Master Clock2)	F_{MCK2}	TCXO pin	-20ppm (*3)	36	+20ppm (*3)	MHz
TCXO Input	V_{TCXO}	DC cut	0.8	-	1.5	Vpp
SPI clock frequency	F_{SCLK}	SCLK pin	0.032	2	16	MHz
SPI clock duty ratio	D_{SCLK}	SCLK pin	45	50	55	%
RF channel frequency	F_{RF}	LNA_P,PA_OUT pins	863	-	960	MHz

*1 Those pins with symbol I, Is at pin definition section
*2 Use REG_OUT output of this LSI.
*3 It's max.+10ppm and min.-10ppm at 10kbps setting.

[Note]
Electrical characteristics are in the above recommended operating conditions without special instruction.

* Following “Typ” value is not guaranteed value studied variation of IC but typical centre value.

●Power consumption

Item	Symbol	Conditions	Min	Typ (*2)	Max	Unit
Power Consumption (*1)	IDD1	Sleep state (Maintain register values)	−	0.9	3.0(*3)	μA
	IDD2	Idle state	−	1.4	3.0	mA
	IDD3	RF RX state (*4)	−	15.0	20.0	mA
	IDD4	RF TX state (1mW) (*4)	−	13.0	20.0	mA
	IDD5	RF TX state (10mW) (*4)	−	24.0	35.0	mA
	IDD6	RF TX state (20mW) (*4)	−	32.0	43.0	mA

*1 Power consumption is sum of current consumption of all power supply pins
*2 “Typ” value is centre value under condition of VDDIO=3.3V, 25deg.C.
*3 “Typ”, “Max” values are under condition of 25deg.C
*4 Current value when the data rate is 100kbps and the frequency is 920MHz.

●DC characteristics

Item	Symbol	Conditions	Min	Typ (*2)	Max	Unit
Voltage Input High	VIH1	Digital input/inout pins	V_{DDIO} x0.75	–	V_{DDIO}	V
	VIH2	XIN pin	V_{DDRF} x0.9	–	V_{DDRF}	V
Voltage Input Low	VIL1	Digital input/inout pins	0	–	V_{DDIO} x0.18	V
	VIL2	XIN pin	0	–	V_{DDRF} X0.1	V
Threshold Voltage High level	VT+	Digital pins with shmitt trigger gate	–	1.2	V_{DDIO} x0.75	V
Threshold Voltage Low level	VT-	Digital pins with shmitt trigger gate	V_{DDIO} x0.18	0.8	–	V
Input Leakage Current	IIH1	Digital input pins	-1	–	1	ìA
	IIH2	XIN pin	-0.3	–	0.3	ìA
	IIL1	Digital input pins	-1	–	1	ìA
	IIL2	XIN pin	-0.3	–	0.3	ìA
Output Leakage Current 3-state pins	IOZH1	Digital inout pins	-1	–	1	ìA
	IOZL1	Digital inout pins	-1	–	1	ìA
Voltage Ouput level H	VOH	IOH=-4mA /-2mA (*1)	V_{DDIO} x0.8	–	V_{DDIO}	V
Voltage Ouput level L	VOL	IOL=4mA /2mA (*1)	0	–	0.3	V
Regulator output voltage	REG_CORE (*2)	Sleep state	0.95	1.3	1.65	V
		Other states	1.40	1.5	1.60	V
Pin Capacitance	CIN	Input pins	–	6	–	pF
	COUT	Output pins	–	9	–	pF
	CRFIO	RF inout pins	–	9	–	pF
	CAI	Analog input pins	–	9	–	pF

*1 DMON pin
*2 REG_CORE pin and REG_OUT pin

●RF characteristics

Data Rate : 10kbps/ 20kbps/ 40kbps/ 50kbps/100kbps/ 150kbps/200kbps/ 400kbps
Modulation scheme : GFSK
Channel spacing : 200kHz/400kHz/600kHz
Frequency : Support 750MHz to 1GHz by changing L/C components between IND1 and IND2 pins

[TX]

Item	Condition	Min	Typ	Max	Unit
TX Power	20mW(13dBm) mode	9	13	15	dBm
	10mW(10dBm) mode	6	10	12	dBm
	1mW(0dBm) mode	-4	0	2	dBm
Adjustment range of frequency shift [Fdev] (*1)		—	—	2,250	kHz
920MHz band (920.5MHz to 928.1MHz)					
Occupied bandwidth	n : number of channel	—	—	200 x n	kHz
Power at edge of channel	20mW mode (920.5MHz to 922.3MHz)	—	—	-7	dBm
	10mW mode	—	—	-10	dBm
	1mW mode	—	—	-20	dBm
Adjacent Channel Power	20mW mode ±1CH, bandwidth 200kHz)	—	-33	-15	dBm
	10mW mode +/-1ch bandwidth: 200kHz	—	-39	-18	dBm
	1mW mode +/-1ch bandwidth: 200kHz	—	-47	-26	dBm
Modulation index accuracy	In IEEE802.15.4g opetation	-20	—	+20	%
Unnecessary emission level (20mW mode)	710MHz or lower, 100kHz band	—	-65	-36	dBm
	Higher than 710MHz to 900MHz, 1MHz band	—	-70	-55	dBm
	Higher than 900MHz to 915MHz, 100kHz band	—	-72	-55	dBm
	Higher than 915MHz to 930MHz, 100kHz band (Excluding within 200 + 100xnkHz above and below the channel frequency, however, within 100 + 100xnkHz above and below for 920.5MHz to 922.3MHz. n is the number of concurrently used channels)	—	-51	-36	dBm
	Higher than 930MHz to 1000MHz, 100kHz band	—	-70	-55	dBm
	Higher than 1000MHz to 1215MHz, 1MHz band	—	-75	-45	dBm
	Higher than 1215MHz, 1MHz band (2nd harmonics or higher)	—	-40	-30	dBm
	710MHz or lower, 100kHz band	—	-65	-36	dBm
	Higher than 710MHz to 900MHz, 1MHz band	—	-70	-55	dBm
RF Frequency	LNA_P,PA_OUT	750.0	—	1000.0	MHz
915MHz band (902MHz to 928MHz)					
6dB bandwidth	Frequency shift=171kHz	500	—	—	kHz
Power spectrum density	20mW mode, frequency shift = 171kHz, 3kHz band	—	—	8	dBm
Unnecessary emission level (20mW mode)	900MHz or lowe	—	-65	-56	dBm
	Higher than 960MHz (2nd harmonics or higher)	—	-50	-41	dBm
868MHz band (863MHz to 870MHz) (*2)					
Unnecessary emission level (10mW mode)	Higher than 1000MHz (2nd harmonics or higher)	—	-35	-30	dBm

*1 While the adjustment range is described as above, the possible maximum value depends on the RF channel frequency to be used.
RF channel frequency ± frequency shift should not include a multiple of 36MHz (864MHz, 900MHz, 936MHz, and so on).
Example) For 902MHz, 2,000kHz can be set at a maximum.

*2 863.5MHz to 866.2MHz cannot be used. For details, see section "Setting channel frequency."

[RX]

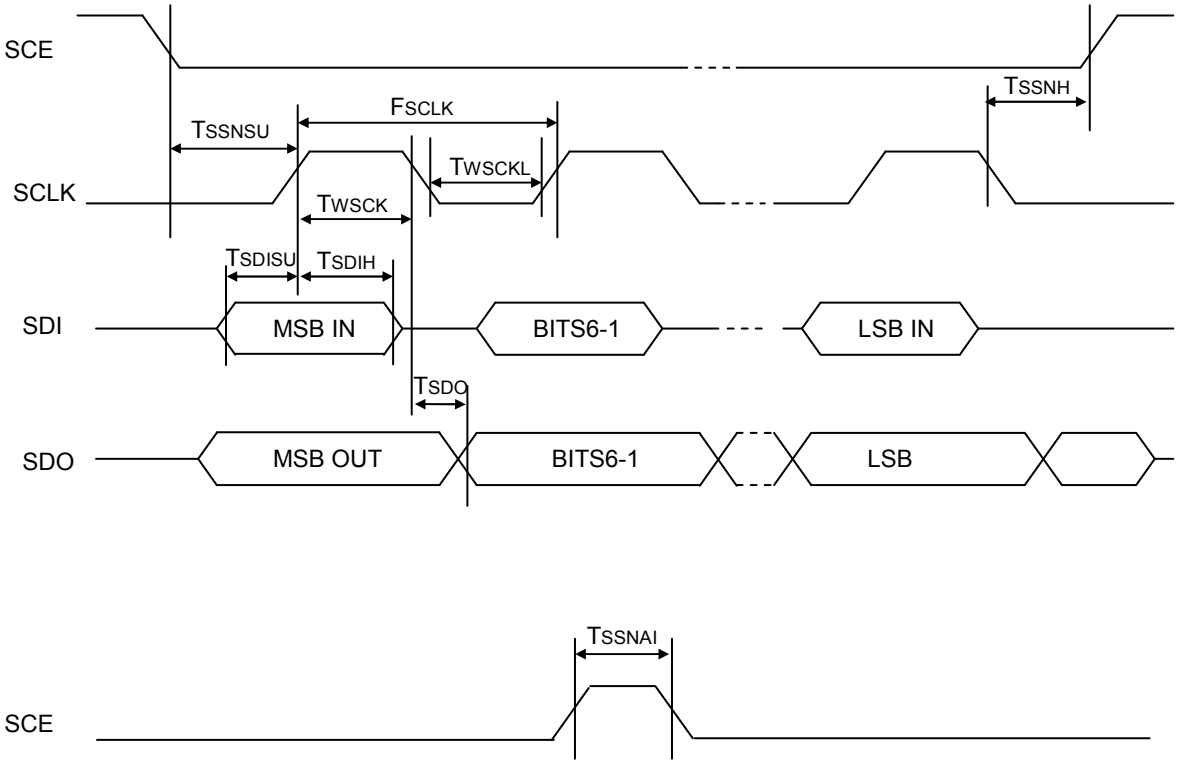
Item	Condition	Min	Typ	Max	Unit
920MHz band (920.5MHz to 928.1MHz)					
Minimum RX sensitivity BER<0.1%	50kbps mode（NBO_SEL=0）	―	-107	-102	dBm
	100kbps mode（NBO_SEL=0）	―	-105	-100	dBm
	200kbps mode（NBO_SEL=0）	―	-102	-97	dBm
Maximum input level	50kbps mode/100kbps mode/200kbps mode	0	―	―	dBm
RX C/I Adjacent Channel	50kbps mode	20	35	―	dB
	100kbps mode	20	35	―	dB
	200kbps mode	20	35	―	dB
RX C/I second adjacent interference	50kbps mode	30	45	―	dB
	100kbps mode	30	45	―	dB
	200kbps mode	30	45	―	dB
Minimum power detection level		―	―	-100	dBm
Power detection range		60	70	―	dB
Power detection accuracy		-6	―	+6	dB
Spurious Emission level ARIB T108 measurement condition 915.9MHz~916.9MHz 920.5MHz~929.7MHz	Compliant with FCC, ARIB, ETSI standard	―	―	TBD	dBm
		―	―	TBD	dBm
		―	―	TBD	dBm
		―	―	TBD	dBm
		―	―	TBD	dBm
		―	―	TBD	dBm
		―	―	TBD	dBm
		―	―	TBD	dBm
		―	―	TBD	dBm
915MHz band (902MHz to 928MHz)					
Minimum receiver sensitivity BER<0.1%	100kbps mode (when NBO_SEL is 0, the modulation index is 1)	―	-105	-99	dBm
	150kbps mode (when NBO_SEL is 0, the modulation index is 0.5)	―	-102	-96	dBm
	200kbps mode (when NBO_SEL is 0, the modulation index is 1)	―	-102	-96	dBm
	100kbps mode (frequency shift: 171kHz)	―	-100	-87	dBm
	150kbps mode (frequency shift: 171kHz)	―	-97.5	-84	dBm
	200kbps mode (frequency shift: 171kHz)	―	-96.5	-83	dBm
868MHz band (863MHz to 870MHz) (*1)					
Minimum receiver sensitivity BER<0.1%	50kbps mode (when NBO_SEL is 0)	―	-107	-102	dBm
	100kbps mode (when NBO_SEL is 0)	―	-105	-100	dBm
	200kbps mode (when NBO_SEL is 0)	―	-102	-97	dBm
Collateral emission level	1000MHz or lower (local frequency)	―	-63	-57	dBm
	Higher than 1000MHz	―	-57	-47	dBm

*1 863.5MHz to 866.2MHz cannot be used. For details, see section "Setting channel frequency."

●SPI interface

Item	Symbol	Condition	Min	Typ	Max	Unit
SCLK clock frequency	FSCLK	Load capacitance CL=20pF	0.032	2	16	MHz
SCEN input setup time	TSSNSU		30	−	−	ns
SCEN input hold time	TSSNH		30	−	−	ns
SCLK high pulse width	TWSCKH		28	−	−	ns
SCLK low pulse width	TWSCKL		28	−	−	ns
SDI input setup time	TSDISU		5	−	−	ns
SDI input hold time	TSDIH		15	−	−	ns
SCEN Negation interval	TSSNAI		60	−	−	ns
SDO output delay	TSDO		−	−	22	ns

[Note]
All timing parameter is defined at voltage level of V_{DDIO} x 20% and V_{DDIO}.

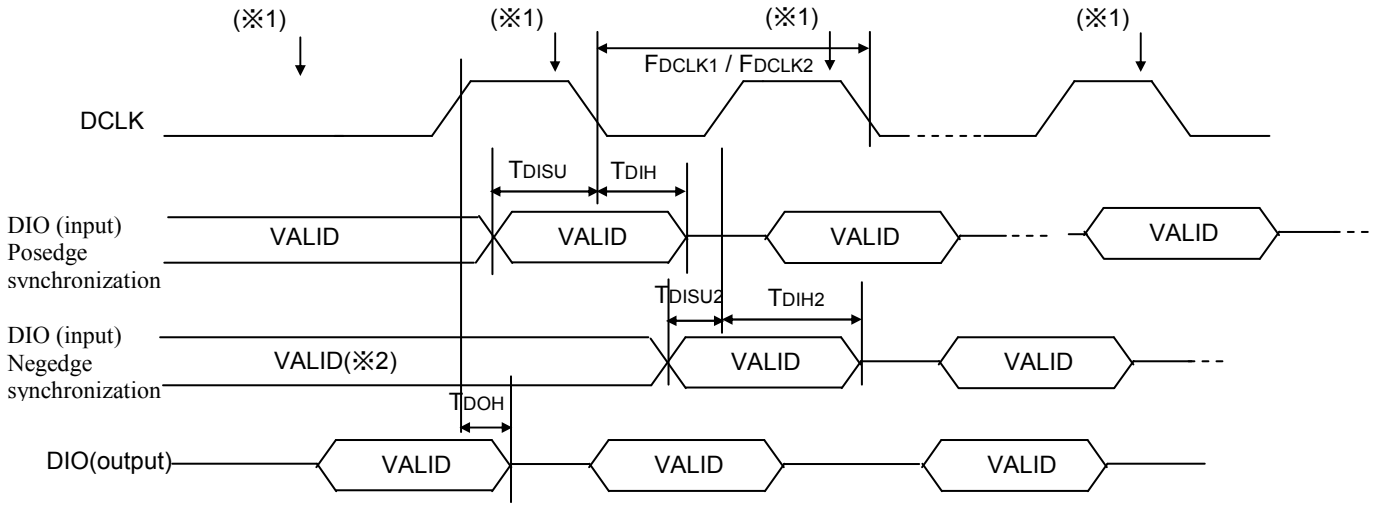


●DIO interface

Item	Symbol	Condition	Min	Typ	Max	Unit
DIO input setup time (DCLK Posedge synchronization)	TDISU	Load capacitance CL=20pF	1	—	—	us
DIO input setup time (DCLK Negedge synchronization)	TDISU2		0	—	—	us
DIO input hold time (DCLK Posedge synchronization)	TDIH		0	—	—	ns
DIO input hold time (*3) (DCLK Negedge synchronization)	TDIH2		10 5 2.5	—	—	us
DIO Output hold time	T_{DOH}		20	—	—	ns
DCLK clock frequency (*1) (*3) (TX)	F_{DCLK1}		-20ppm	50 100 200	+20ppm	kHz
DCLK clock frequency (*2) (*3) (RX)	F_{DCLK2}		-4%	50 100 200	+4%	kHz
DCLK clock output duty ratio (TX)	D_{DCLK}		—	50	—	%
DCLK clock output duty ratio (RX)	D_{DCLK}		40	—	60	%

*1 DCLK clock frequency in TX mode will be varied depending on the variance of master clock frequency.
*2 DCLK clock frequency in RX mode will be varied by reproduced clock and its jitter.
*3 These characteristics are depend on data rate value of bit2-0(RATE [2:0]) of register [DATA_SET].
(upper: 50kbps, mid: 100kbps, lower: 200kbps)

[Note]
All timing parameter is defined at voltage level of V_{DDIO} x 20% and V_{DDIO}.



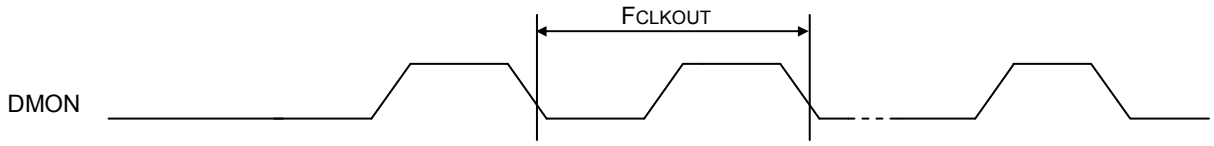
(*1) Timing when this LSI takes the DIO input.
(*2) For the Negedge synchronization, the first two bits of data to be input from DIO have the same data.

●Clock output

Register [CLK_SET] address (B0 0x02) sets if clock output enable or not(Initial value:enable), freaquency output to DMON pin.

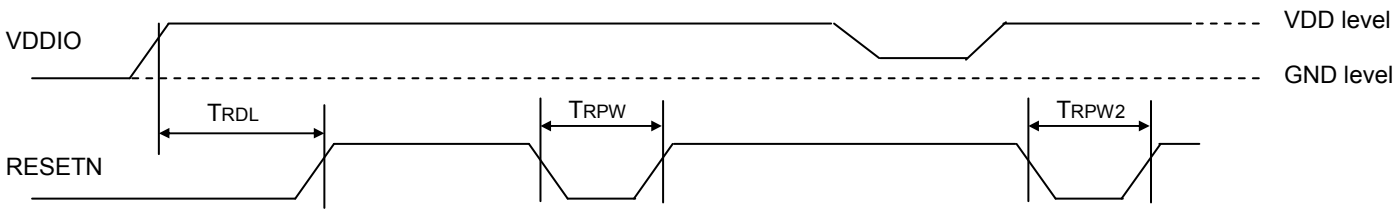
Item	Symbol	Condition		Min	Typ	Max	Unit
Clock output frequency	F_{CLKOUT}	Load capacitance CL=20pF		0.0088	6	36	MHz
Clock output duty ratio (*1)	D_{CLKOUT}		12MHz	30	-	70	%
			Other than above	48	50	52	%

*1 Duty ratio will be H:L = 1:2 when output frequency is 12MHz.. See register [CLK_OUT] address (B0 0x03).



●Reset

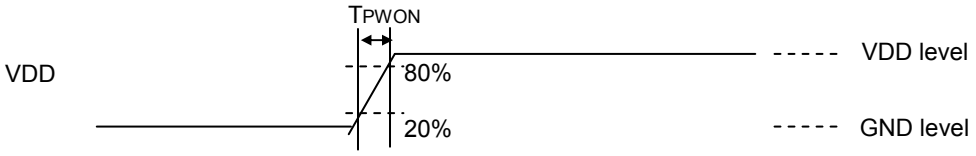
Item	Symbol	Condition	Min	Typ	Max	Unit
RESETN delay time（Power on）	T_{RDL}	All power supply pins (After power on)	1.5	–	–	ms
RESETN assert time (pulse width) (When starting from VDDIO=0V)	T_{RPW}		200	–	–	ns
RESETN pulse time 2 (*1) (When starting from VDDIO≠0V)	T_{RPW2}	VDD>1.8V	1.5	–	–	ms



(*1) When starting from VDDIO≠.0V, input a pulse to the RESETN signal after VDDIO exceeds 1.8V.

●Power on sequence

Item	Symbol	Condition	Min	Typ	Max	Unit
Power on time differences	T_{PWON}	Power on state (All power supply pins)	−	−	5	ms



■REGISTERS

●Register map

It is consist of 3bank, BANK0, BANK1, BANK2. Each BANK has address space of 0x00 to 0x7F 128 byte in total.
The space shown as gray highlighted part is not implemented in LSI or reserved bits. TX/RX FIFO is implemented in PHY block, those register except for FIFO is implemented in SPI block. The address not exisit in the memory map is not accesible. Also, the address is not accessible during the VCO calibration.

For registers whose setting value is specifically shown in the register list, please set the value shown in the list and do not change it.

: Implemented as functionable register
: Impelemted as reserved bits

BANK0

Address	Symbol (# test register)	Bit 7	6	5	4	3	2	1	0	Description
0x00	BANK_SEL									Register access destination (BANK) select
0x01	RST_SET									Software reset control
0x02	CLK_SET									Clock configuration
0x03	CLKOUT									Frequency setting of CLKOUT output
0x04	RATE_SET1									Data rate conversion setting 1
0x05	RATE_SET2									Data rate conversion setting 2
0x06-0x07	Reserved									Reserved
0x08	#ADC_CLK_SET									ADC clock setting for RSSI
0x09-0x0a	Reserved									Reserved
0x0b	#OSC_ADJ									Load capacitor trimming in oscillation circuit
0x0c	#RF_TEST_MODE									RF TX test pattern configuration
0x0d-0x0e	Reserved									Reserved
0x0f	# PHY_STATE									PHY state display
0x10	#FIFO_BANK									FIFO bank display
0x11	#PLL_LOCK_DETECT									Parameter setting for PLL lock detection
0x12	CCA_IGNORE_LEVEL									ED threshold level to exclude CCA judgement
0x13	CCA_LEVEL									Threshold level for CCA operation
0x14	CCA_ABORT									Time parameter to terminate CCA operation during AUTO_ACK case
0x15	CCA_CNTRL									CCA control setting and reporting result
0x16	ED_RSLT									Readout register for ED (Energy Detection) values
0x17	IDLE_WAIT_L									Time parameter to judge as IDLE state during CCA operation. (lower 8bits)
0x18	IDLE_WAIT_H									Time parameter to judge as IDLE state during CCA operation (upper 2bits)
0x19	CCA_PROG_L									Elapsed time as IDLE state during CCA operation (lower 8bits)
0x1a	CCA_PROG_H									Elapsed time as IDLE state during CCA operation (upper 2bits)
0x1b	ED_CNTRL									ED (Energy Detection) control
0x1c	GAIN_MtoL									Threshold level to switch from middle gain to low gain
0x1d	GAIN_LtoM									Threshold level to switch from low gain to middle gain
0x1e	GAIN_HtoM									Gain update setting and threshold level to switch from high gain to middle gain
0x1f	GAIN_MtoH									Threshold level to switch from middle gain to high gain
0x20	RSSI_ADJ_M									RSSI offset value in middle gain range
0x21	RSSI_ADJ_L									RSSI offset value in low gain range
0x22	RSSI_STABLE_TIME									Time parameter for RSSI value become stable after gain switch
0x23	RSSI_VAL_ADJ									RSSI scale factor for ED value conversion.
0x24	INT_SOURCE_GRP1									FIFO clear setting, interrupt status for INT05 to INT00
0x25	INT_SOURCE_GRP2									Interrupt status for INT15 to INT8
0x26	INT_SOURCE_GRP3									Interrupt status for INT23 to INT16
0x27	INT_SOURCE_GRP4									Interrupt status for INT25 to INT24
0x28	PD_DATA_REQ									Data transmission request
0x29	PD_DATA_IND									Data reception reporting
0x2a	INT_EN_GRP1									Interrupt mask for INT03 to INT00
0x2b	INT_EN_GRP2									Interrupt mask for INT15 to INT08
0x2c	INT_EN_GRP3									Interrupt mask for INT23 to INT16
0x2d	INT_EN_GRP4									Interrupt mask for INT25 and INT24
0x2e	CH_EN_L									Channel enable setting for lower 8ch
0x2f	CH_EN_H									Channel enable setting for upper 8ch
0x30	IF_FREQ_AFC_H									IF frequency setting in AFC mode. (upper 8bits)
0x31	IF_FREQ_AFC_L									IF frequency setting in AFC mode (lower 8bits)
0x32	BPF_AFC_ADJ_H									Capacitor trimming of band pass filter in AFC mode operation (upper 2bits)
0x33	BPF_AFC_ADJ_L									Capacitor trimming of band pass filter in AFC mode operation (lower 8bits)
0x34	AFC_CNTRL									AFC mode configuration
0x35	TX_ALARM_LH									Alert level setting for remaining size of TX FIFO (alarm for FIFO full)
0x36	TX_ALARM_HL									Alert level setting for remaining size of TX FIFO (alarm for TX empty)
0x37	RX_ALARM_LH									Alert level setting for remaining size of RX FIFO (alarm for RX full)

BANK0 (continued)

Address	Symbol (# test register)	Bit 7	6	5	4	3	2	1	0	Description
0x38	RX_ALARM_HL									Alert level setting for remaining size of RX FIFO (alarm for RX empty)
0x39	PREAMBLE_SET									Preamble pattern setting for TX/RX operation
0x3a	SFD1_SET1									Frame synchronization pattern (max 4byte) of 1st byte of 1st pattern
0x3b	SFD1_SET2									Frame synchronization pattern (max 4byte) of 2nd byte of 1st pattern
0x3c	SFD1_SET3									Frame synchronization pattern (max 4byte) of 3rd byte of 1st pattern
0x3d	SFD1_SET4									Frame synchronization pattern (max 4byte) of 4th byte of 1st pattern
0x3e	SFD1_SET1									Frame synchronization pattern (max 4byte) of 1st byte of 2nd pattern
0x3f	SFD2_SET2									Frame synchronization pattern (max 4byte) of 2nd byte of 2nd pattern
0x40	SFD2_SET3									Frame synchronization pattern (max 4byte) of 3rd byte of 2nd pattern
0x41	SFD2_SET4									Frame synchronization pattern (max 4byte) of 4th byte of 2nd pattern
0x42	TX_PR_LEN									TX preamble length (max 255 byte)
0x43	RX_PR_LEN/SFD_LEN									RX preamble comparison length (max 16byte) and SFD length setting
0x44	SYNC_CONDITION									Tolerance of error bit in RX preamble detection and SFD detection (max 15bits)
0x45	PACKET_MODE_SET									Configuration for Packet mode (FIFO in use)
0x46	FEC/CRC_SET									FEC and CRC configuration in TX packet
0x47	DATA_SET									Configuration of TX and RX data
0x48	CH0_FL									Frequency parameter for ch0 (lower 8bits)
0x49	CH0_FM									Frequency parameter for ch0 (middle 8bits)
0x4a	CH0_FH									Frequency parameter for ch0 (upper 4bits)
0x4b	CH0_NA									N counter and A counter value for ch0
0x4c	CH_SPACE_L									Frequency spacing setting to next channel (lower 8bits)
0x4d	CH_SPACE_H									Frequency spacing setting to next channel (upper 8bits)
0x4e	F_DEV_L									Frequency deviation setting for GFSK modulation (lower 8bits)
0x4f	F_DEV_H									Frequency deviation setting for GFSK modulation (upper 8bits)
0x50	ACK_TIMER_L									Ack timer setting for Auto_Ack operation (lower 8bits)
0x51	ACK_TIMER_H									Ack timer setting for Auto_Ack operation (upper 8bits)
0x52	ACK_TIMER_EN									Ack timer configuration
0x53	ACK_FRAME1									Frame Control Field (2bytes) setting in Ack packet (lower byte)
0x54	ACK_FRAME2									Frame Control Field (2bytes) setting in Ack packet (upper byte)
0x55	AUTO_ACK_SET									Configuration of Auto_Ack function
0x56-x58	Reserved									Reserved
0x59	GFIL00 / FSK_FDEV1									Gaussian filter parameter 1 / 1st set of frequency deviation parameter for FSK modulation
0x5a	GFIL01 / FSK_FDEV2									Gaussian filter parameter 2 / 2nd set of frequency deviation parameter for FSK modulation
0x5b	GFIL02 / FSK_FDEV3									Gaussian filter parameter 3 / 3rd set of frequency deviation parameter for FSK modulation
0x5c	GFIL03 / FSK_FDEV4									Gaussian filter parameter 4 / 4th set of frequency deviation parameter for FSK modulation
0x5d	GFIL04									Gaussian filter parameter 5
0x5e	GFIL05									Gaussian filter parameter 6
0x5f	GFIL06									Gaussian filter parameter 7
0x60	GFIL07									Gaussian filter parameter 8
0x61	GFIL08									Gaussian filter parameter 9
0x62	GFIL09									Gaussian filter parameter 10
0x63	GFIL10									Gaussian filter parameter 11
0x64	GFIL11									Gaussian filter parameter 12
0x65	FSK_TIME1									Timing parameter for Frequency deviation in FSK modulation (FDEV3)
0x66	FSK_TIME2									Timing parameter for Frequency deviation in FSK modulation (FDEV2)
0x67	FSK_TIME3									Timing parameter for Frequency deviation in FSK modulation (FDEV1)
0x68	FSK_TIME4									Timing parameter for Frequency deviation in FSK modulation (FDEV0)

BANK0 (continued)

Address	Symbol (# test register)	Bit								Description
		7	6	5	4	3	2	1	0	
0x69	PLL_MON/DIO_SEL									Output configuration of PLL lock detection and DIO mode configuration
0x6a	FAST_TX_SET									Trigger timing for start of transmission in FAST_TX mode
0x6b	CH_SET									TX/RX channel setting
0x6c	RF_STATUS									RF status register
0x6d	2DIV_ED_AVG									The number of averaging process in ED computation for 2 diversity mode
0x6e	2DIV_GAIN_CNTRL									Gain control mode setting
0x6f	2DIV_SEARCH									Timing parameter in 2 diversity mode
0x70	2DIV_FAST_LV									Threshold value setting in 2 diversity mode
0x71	2DIV_CNTRL									Miscellaneous function in 2 diversity mode
0x72	2DIV_RSLT									Status register for 2 diversity mode
0x73	ANT1_ED									ED value register for ANT1
0x74	ANT2_ED									ED value register for ANT2
0x75	RF_CNTRL_SET									Configuration of RF control pin (ANT_SW, TRX_SW, DCNT)
0x76	Reserved									Reserved
0x77	CRC_AREA/FIFO_TRG									CRC computation area and FIFO trigger setting
0x78	RSSI_MON									RSSI data output
0x79	TEMP_MON									Temperature data output
0x7a	PN9_SET_L									Initial root value for PN9 hardware used for Whitening process (lower 8bits)
0x7b	PN9_SET_H									Initial root value for PN9 hardware used for Whitening process (upper 1bit) and enable control
0x7c	RD_ FIFO_LAST									FIFO remaining size or address of FIFO
0x7d	Reserved									Reserved
0x7e	WR_TX_FIFO									TX FIFO data
0x7f	RD_RX_FIFO									RX FIFO data

BANK1

Address	Symbol	Bit								Description
		7	6	5	4	3	2	1	0	
0x00	BANK_SEL									Register access destination (BANK) select
0x01	DEMOD_SET									Demodulator setting
0x02	RSSI_ADJ									RSSI data adjustment
0x03	RSSI/TEMP_OUT									Output setting for RSSI and Temperature data
0x04	PA_ADJ1									PA adjustment register1
0x05	PA_ADJ2									PA adjustment register2
0x06	PA_ADJ3									PA adjustment register3
0x07	PA_CNTRL									External PA control and PA mode setting
0x08	SW_OUT/RAMP_ADJ									Timing parameter for ANT_SW/TRX_SW signal control
0x09	PLL_CP_ADJ									Current adjustment for PLL charge pump
0x0a	IF_FREQ_H									IF frequency setting (upper 8bits)
0x0b	IF_FREQ_L									IF frequency setting (lower 8bits)
0x0c	IF_FREQ_CCA_H									IF frequency setting during CCA operation (upper 8bits)
0x0d	IF_FREQ_CCA_L									IF frequency setting during CCA operation (lower 8bits)
0x0e	BPF_ADJ_H									Bandwidth adjustment in Band-Pass-Filter (upper 2bits)
0x0f	BPF_ADJ_L									Bandwidth adjustment in Band-Pass-Filter (lower 8bits)
0x10	BPF_CCA_ADJ_H									Bandwidth adjustment in Band-Pass-Filter during CCA operation (upper 2bits)
0x11	BPF_CCA_ADJ_L									Bandwidth adjustment in Band-Pass-Filter during CCA operation (lower 8bits)
0x12	RSSI_LPF_ADJ									Time constant adjustment for RSSI output
0x13	PA_REG_FINE_ADJ									Trimming adjustment for PA regulator
0x14	IQ_MAG_ADJ									Amplitude balance adjustment for IF I/Q signals
0x15	IQ_PHASE_ADJ									Phase balance adjustment for IF I/Q signals
0x16	VCO_CAL_MIN_FL									VCO minimum operating frequency (lower 8bits)
0x17	VCO_CAL_MIN_FM									VCO minimum operating frequency (middle 8bits)
0x18	VCO_CAL_MIN_FH									VCO minimum operating frequency (upper 4bits)
0x19	VCO_CAL_MAX_N									VCO maximum operating frequency
0x1a	VCO_CAL_MIN									Status register for lower side of VCO calibration result
0x1b	VCO_CAL_MAX									Status register for upper side of VCO calibration result
0x1c	VCO_CAL									Status register for current VCO calibration value
0x1d	VCO_CAL_START									VCO calibration control
0x1e	BPF_ADJ_OFFSET									Offset data for BPF adjustment
0x1f-0x2a	Reserved									Reserved
0x2b	# ID_CODE									ID code
0x2c-0x32	Reserved									Reserved
0x33	# PA_REG_ADJ1									PA regulator adjustment register1
0x34	# PA_REG_ADJ2									PA regulator adjustment register2
0x35	# PA_REG_ADJ3									PA regulator adjustment register3
0x36-0x39	Reserved									Reserved
0x3a	# PLL_CTRL									RF adjustment
0x3b-0x3e	Reserved									Reserved
0x3f	# RX_ON_ADJ2									RX_ON adjustment register 2
0x40-0x48	Reserved									Reserved
0x49	# LNA_GAIN_ADJ_M									LNA gain adjustment in middle gain operation
0x4a	# LNA_GAIN_ADJ_L									LNA gain adjustment in lower gain operation
0x4b-0x4d	Reserved									Reserved
0x4e	# MIX_GAIN_ADJ_M									Mixer gain adjustment in middle gain operation
0x4f	# MIX_GAIN_ADJ_L									Mixer gain adjustment in lower gain operation
0x50-0x54	Reserved									Reserved
0x55	#TX_OFF_ADJ1									TX_OFF adjustment register 1
0x56-0x59	Reserved									Reserved
0x5a	# RSSI_SLOPE_ADJ									RSSI slope adjustment
0x5b-0x7f	Reserved									Reserved

BANK2

Address	Symbol	Bit								Description
		7	6	5	4	3	2	1	0	
0x00	BANK_SEL									Register access destination (BANK) select
0x01-0x11	Reserved									Reserved
0x12	# SYNC_MODE									Mode setting for bit synchronization
0x13-0x1d	Reserved									Reserved
0x1e	# PA_ON_ADJ									Timing adjustment for PA_ON signal
0x1f-0x21	Reserved									Reserved
0x22	# RX_ON_ADJ									Timing adjustment for RX_ON signal
0x23	Reserved									Reserved
0x24	# RXD_ADJ									Timing adjustment for RXD signal
0x25-0x2b	Reserved									Reserved
0x2c	#RAMP_CNTRL									Lamp control
0x2d-0x5f	Reserved									Reserved
0x60	ADDFILCNTRL									Address filtering function control
0x61	PANID_L									PANID setting for address filtering function (lower 8bits)
0x62	PANID_H									PANID setting for address filtering function (upper 8bits)
0x63	64ADDR1									64bit address setting for address filtering function (1st byte lowest byte)
0x64	64ADDR2									64bit address setting for address filtering function (2nd byte)
0x65	64ADDR3									64bit address setting for address filtering function (3rd byte)
0x66	64ADDR4									64bit address setting for address filtering function (4th byte)
0x67	64ADDR5									64bit address setting for address filtering function (5th byte)
0x68	64ADDR6									64bit address setting for address filtering function (6th byte)
0x69	64ADDR7									64bit address setting for address filtering function (7th byte)
0x6a	64ADDR8									64bit address setting for address filtering function (8th byte, upper byte)
0x6b	SHT_ADDR0_L									Short address0 (16bits) setting for address filtering function (lower 8bits)
0x6c	SHT_ADDR0_H									Short address0 (16bits) setting for address filtering function (upper 8bits)
0x6d	SHT_ADDR1_L									Short address1 (16bits) setting for address filtering function (lower 8bits)
0x6e	SHT_ADDR1_H									Short address1 (16bits) setting for address filtering function (upper 8bits)
0x6f	DISCARD_COUNT_L									Number of discarded packet in address filtering function (lower 8bits)
0x70	DISCARD_COUNT_H									Number of discarded packets in address filtering function (upper 8bits)
0x71-0x7f	Reserved									Reserved

●Register BANK0

0x00[BANK_SEL]

Function: Register access destination (BANK) select
Address: 0x00
Defalut value: 0x00

Bit	Symbol	Description	Default Value	R/W
7	TST_ACEN	Test register access enable (*2) 0: Access forbidden 1: Access permitted	0	R/W
6-2	Reserved	Reserved	000_00	R/W
1-0	BANK[1:0]	BANK select BANK[1:0]＝x00: Access to BANK0 x01: Access to BANK1 x10: Access to BANK2 x11: Forbidden (*1)	00	R/W

[Notes]
*1 Writing x11 to this field is forbbiden.
*2 This bit will affect permission of register access, see “register map” section.

0x01[RST_SET]

Function: Software reset control
Address: 0x01
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7	RST3_EN	Reset enable control 0: Reset forbidden 1: Reset enabled	0	R/W
6	RST2_EN		0	R/W
5	RST1_EN		0	R/W
4	RST0_EN		0	R/W
3	RST_3	Reset PHY Function block (Perform reset by 1)	0	R/W
2	RST_2	Reset RF Function block (Perform reset by 1)	0	R/W
1	RST_1	Reset MODEM Function block (Perform reset by 1)	0	R/W
0	RST_0	Reset SPI Function block (Perform reset by 1) (*1) All resiter value return to “Default Value”	0	R/W

[Details description]
1. Reset enable contol bits (bit7 to bit4) and Reset bits (bit3 to bit0) should be configured at same time. RST_0 bit will return to 0 automatically.
2. Reset process will be terminated 2usec after executed reset bits (bit3 to bit0)

The following table shows the software reset operations for each state.

	Transmitting/receiving state	SLEEP state	IDLE state
RST_3:PHY	The FIFO pointer is cleared. The state transitions to IDLE, RF starts, and then the state transitions to the SET_TRX setting value. During CCA or diversity search, it is initialized and restarted. Do not input RST_3 during transmission.	The FIFO pointer is cleared after SLEEP is released (internal clock is supplied).	The FIFO pointer is cleared. During VCO_CAL, it is initialized and restarted.
RST_2:RF	The PLL circuit is cleared, and the PLL lock is released. Do not input RST_2 during transmission and reception.	The PLL circuit is cleared after SLEEP is released (internal clock is supplied). (This does not affect the operation.)	The PLL circuit is cleared. (This does not affect the operation.)
RST_1:MODEM	The synchronization is cleared at reception. The unmodulated data is output at transmission. Do not input RST_1 during transmission and reception.	The modem circuit is cleared after SLEEP is released (internal clock is supplied). (This does not affect the operation.)	The modem circuit is cleared. (This does not affect the operation.)
RST_0:SPI	All registers are initialized.(* 1) The SET_TRX register is also initialized for TRX_OFF.	All registers are initialized after SLEEP is released (internal clock is supplied).(* 1)	All registers are initialized.(* 1)

* 1 : Only bit6 (TCXO_EN) of the [CLK_SET] register (B0 0x02) is not initialized by the software reset.

0x02[CLK_SET]

Function: Clock configuration
Address: 0x02
Default Value 0x9F

Bit	Symbol	Description	Default Value	R/W
7	CLK_Done	Clock status flag 0: Stop or starting up status 1: Clock is stable stauts	1	R
6	TCXO_EN (*2)	TCXO input control 0: Disabled 1: Enabled	0	R/W
5	SLEEP_EN (*1)	Sleep mode control 0: Normal mode 1: Sleep mode	0	R/W
4	CLKOUT_EN	CLKOUT output control 0: Clock output stop 1: Clock output enabled	1	R/W
3	CLK3_EN	RF Function block clock control 0: Clock stop 1: Clock enabled	1	R/W
2	CLK2_EN	TX Function block clock control 0: Clock stop 1: Clock enabled	1	R/W
1	CLK1_EN	RX Function block clock control 0: Clock stop 1: Clock enabled	1	R/W
0	CLK0_EN	PHY Function block clock control 0: Clock stop 1: Clock enabled	1	R/W

[Detailed description]

1. SPI access will be available while CLK_Done bit is 0b0, RF operation must be done while CLK_Done bit is 0b1. Do not access the BANK1 register during VCO calibration.

[Note]

*1: TCXO_EN bit has to be 0b1, if TCXO is used.
*2: Set this bit first when you use TCXO. Even if you set enable (set another register before this bit) during configuration, the other register setting values are not initialized.

0x03[CLK_OUT]

Function: Frequency setting of CLKOUT output
Address: 0x03
Default Value 0x04

Bit	Symbol	Description	Default Value	R/W
7-0	CLK_DIV	Frequency setting of clock output	0000_0100	R/W

[Detailed description]

Frequency of clock output from DMON pin (#17) can be configured by table shown below. It is available when bit4 (CLKOUT_EN) = 0b1 in [CLK_SET] register (B0, 0x02).

Register value	Output frequency
0x00	36 MHz
0x01	18 MHz
0x02	12 MHz (*1)
0x03	9 MHz
0x04	6 MHz (Default Value)
0x05	4.5 MHz
0x06	3.6 MHz
0x07	1.2 MHz
0x08	600 kHz
0x09	246.5 kHz

Following equation will be applied for combination after 0x09.

Output frequency = 36/ (16* register value+2) (MHz)

Example (regsiter value=0x09)
36 / (16 * 9+2) = 0.2465 MHz

[Note]

*1 Duty ratio will be H:L = 1:2 when output frequency is 12MHz.

0x04[RATE_SET1]

Function: Data rate conversion setting 1
Address: 0x04
Initial value: 0x00

Bit	Register Name	Description	Initial value	R/W
7-0	RATE_SET1	Data rate multiplier setting	0000_0000	R/W

[Detail description]

Set any data rate using this register in combination with [RATE_SET2] register (B0 0x05).
Use this function to set 10kbps, 20kbps, 40kbps, or 150kbps. For details on setting registers and setting values, see the explanation about [DATA_SET] register (B0 0x47) bit 2-0. For details on the data rate conversion, see the explanation about [RATE_SET2] register (B0 0x05).

0x05[RATE_SET2]

Function: Data rate conversion setting 2
Address: 0x05
Initial value: 0x00

Bit	Register Name	Description	Initial value	R/W
7-0	RATE_SET2	Data rate divisor setting	0000_0000	R/W

[Detail description]
Set any data rate using this register in combination with [RATE_SET1] register (B0 0x04).
Use this function to set 10kbps, 20kbps, 40kbps, or 150kbps. For details on setting registers and setting values, see the explanation about [DATA_SET] register (B0 0x47) bit 2-0. For details on the data rate conversion, see the explanation about [RATE_SET2] register (B0 0x05).

●Data rate conversion
Use this function to set a data rate that is not supported by [DATA_SET] register (B0 0x47) bit 2-0.

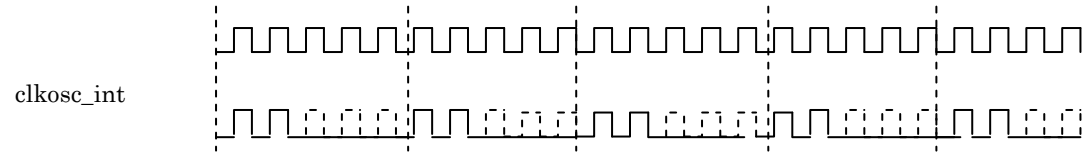
The data rate is calculated with the following formula.

Data rate = (transmission rate set) x (RATE_SET1+1) / (RATE_SET2+1) (RATE_SET2 > RATE_SET1)

[Setting example of 0x04 and 0x05]
When you need 32.768kbps, it is 50kbps multiplied by 40/61.
Setting values = 0x04: 0x27, 0x05: 0x3C
The resulting transmission rate is 32.787kbps (50 x 40 / 61).
The error is 1.00058 (0.058%) (32.787 /32.768).

[Note] Jitter is generated because it is not controlled by PLL. Maximum jitter = RATA_SET2 period - RATE_SET1 period.

[Example of time chart]
RATE_SET1=1
RATE_SET2=4



Place the “RATE_SET2 binary” counter for clock delivery up to the count value of RATE_SET1.

Example:Setting for 150kbps
DATA_SET[2:0]:0x2 (200kbps)
RATE_SET1 :0x02
RATE_SET2 :0x03

Example:Setting for 40kbps
DATA_SET[2:0]:0x2 (200kbps)
RATE_SET1 :0x00
RATE_SET2 :0x04

Example:Setting for 20kbps
DATA_SET[2:0]:0x2 (200kbps)
RATE_SET1 :0x00
RATE_SET2 :0x09

0x08[ADC_CLK_SET]

Function: ADC clock setting for RSSI
Address: 0x08
Default Value 0xC3

Bit	Symbol	Description	Default Value	R/W
7-6	OSC_W_SET	Waiting time for clock stabilization 00: 2ms 01: 1.3ms 10: 1ms 11: 0.6ms	11	R/W
5	Reserved	Reserved	0	
4	ADC_CLK_SET	ADC clock setting for RSSI 0: 1.8 MHz 1: 2.0 MHz	0	R/W
3-0	Reserved	Reserved	0011	R/W

0x0B[OSC_ADJ]

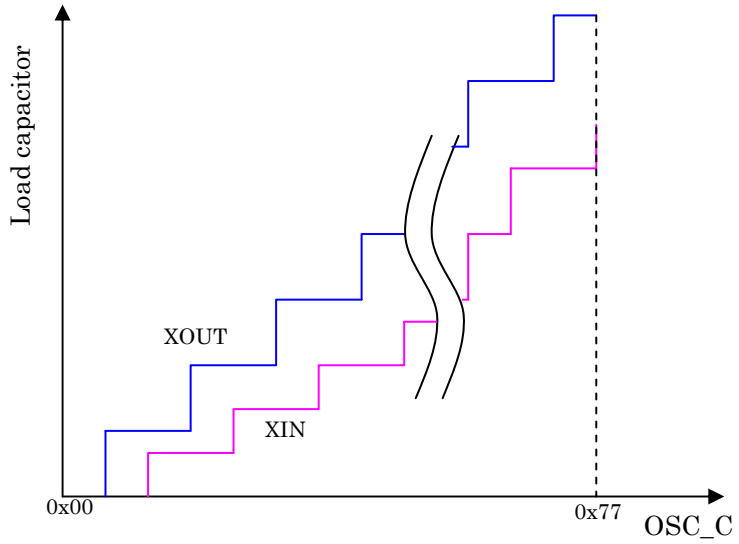
Function: Load capacitor trimming in oscillation circuit
Address: 0x0B
Default Value 0x40

Bit	Symbol	Description	Default Value	R/W
7	Reserved	Reserved	0	R/W
6-0	OSC_C	Load capacitor trimming (*1) (Available range 0x00 - 0x77)	100_000	R/W

[Detailed description]

1. Trimming capacitor will be added to load capacitor at XIN pin (#4) and XOUT pin.

*1 Capacitor value will be varied 0.02pF/2step at XIN pin, 0.03pF/2step at XOUT pin.



0x0C[RF_TEST_MODE]

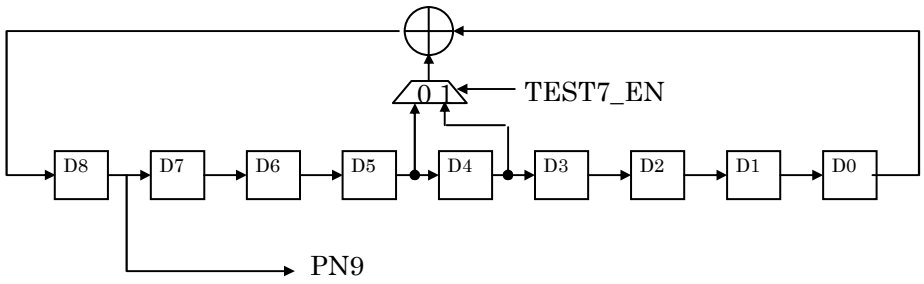
Function: RF TX test pattern configuration
Address: 0x0c
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7	TEST7	See table below	0	R/W
6	TEST6		0	R/W
5	TEST5		0	R/W
4	TEST4		0	R/W
3	TEST3		0	R/W
2	TEST2		0	R/W
1	TEST1		0	R/W
0	TEST_EN	Test mode enable control 0: Test control disabled 1: Test control enable	0	R/W

[Detailed description]

1. All bits in this register have to be 0b0 in normal mode
2. Setting of lowest bit number takes priority when multiple pattern generations are selected.
3. Data rate will be configured in bit 2-0 (RATE[2:0]) in register [DATA_SET] address (B0, 0x47)

*1 PN9 output sequence implemented in most of BER measurement equipment is different from the one defined by IEEE. "BER measurement compatible PN9" refer to following polinomials.



0x0F[PHY_STATE]

Function: PHY state display/Preamble detection status display (for debugging)
Address: 0x0f
Initial value: 0xC0

Bit	Register name	Description	Initial value	R/W
7-6	Reserved	Reserved	11	R/W
5	PB_DET (*1)	Preamble detection status display 0: Not detected 1: Detected	0	R/W
4-0	PHY_STATE (*2)	PHY state display	0_0000	R/W

[Detail description]

1. The preamble detection status is displayed. The preamble detection status shows 1 when it matches or does not match all of the PR[7:0] values set in [PREAMBLE_SET] register (B0 0x39) independent from [SYNC_CONDITION] register (B0 0x44) bit3-0 (PR_SYNC).
2. The status of the PHY state machine is displayed. This bit operates in conjunction with [RF_STATUS] register(B0 0x6c).

PHY_STATE[4:0]	State name	Description	Remarks
0x00	IDLE	Transmission/reception instruction wait state	TRX_OFF takes this state. This state comes after resetting PHY.
0x01	TX_TXD	Transmitted data wait state	
0x02	TX_PB	Preamble transmit state	
0x03	TX_SFD	SFD transmission state	
0x04	TX_LEN	Length transmit state	
0x05	TX_DATA	DATA transmission state	
0x06	TX_CRC	CRC transmission state	
0x07	TX_WAIT	Transmit wait state	This state comes after completing the transmission.
0x08	TX_OFF	Transmission OFF state	
0x09	TX_DIO	DIO transmission state	
0x0B	TX_MOD	Transmission completion wait state	
0x11	RX_RXD	Received SFD detection wait state	
0x14	RX_LEN	Length receive state	
0x15	RX_DATA	DATA receive state	
0x16	RX_CRC	CRC receive state	
0x17	RX_RXD2	Receive wait state	This state comes after completing the reception.
0x18	RX_OFF	Reception OFF state	
0x19	RX_DIO	DIO receive state	
0x1C	RX_DIV1	Diversity search state 1	
0x1D	RX_DIV2	Diversity search state 2	
0x1F	RX_FEC_WAIT	Operation for FEC wait state	

[Note] This register (PHY_STATE) is provided only for debugging. Do not use it for other purposes.
If a PHY_STATE value other than above is read when you use it for debugging, try to read it again.

0x10[FIFO_BANK]

Function: FIFO bank display
Address: 0x10
Initial value: 0x00

Bit	Register name	Description	Initial value	R/W
7-4	Reserved	Reserved	0000	R
3	SPI_TX_B	SPI-FIFO write bank monitor 0: FIFO0 1: FIFO1	0	R
2	SPI_RX_B	SPI-FIFO read bank monitor 0: FIFO0 1: FIFO1	0	R
1	PHY_TX_B	PHY-FIFO write bank monitor 0: FIFO0 1: FIFO1	0	R
0	PHY_RX_B	PHY-FIFO read bank monitor 0: FIFO0 1: FIFO1	0	R

[Detail description]
These bits transit from 0 (FIFO bank0) to 1 (FIFO bank1) or from 1 (FIFO bank1) to 0 (FIFO bank0) under the following conditions. The initial value is always 0 (FIFO bank0).
SPI_TX_B ...When SPI completes writing a Length of data while writing transmitted data to FIFO
SPI_RX_B ...When SPI completes reading a Length of data while reading received data from FIFO
PHY_TX_B ...When PHY completes writing a Length of data while writing received data to FIFO
PHY_RX_B ...When PHY starts reading a Length of data while reading transmitted data from FIFO

0x11[PLL_LOCK_DETECT]

Function: Parameter setting for PLL lock detection
Address: 0x11
Default Value 0x83

Bit	Symbol	Description	Default Value	R/W
7	PLL_LD_EN (*1)	PLL unlock detection control 0: No PLL unlock detection 1: Perform PLL unlock detection	1	R/W
6-0	TIM_PLL_LD[6:0]	PLL unlock judgement time Judgement time = Register value x 8.88 usec + 8.88usec Default Value = 3 x 8.88 + 8.88 = 35.52usec	000_0011	R/W

[Detailed description]
*1: Perform unlock detection. Following action will take place when PLL unlock is detected.
RX mode operation: Generate INT[25] in interrupt group4, continue RX mode operation.
TX mode operation: Generate INT[25] in interrupt group4, move to IDLE state.

[Note]
1. Perform PHY reset in [RST_SET] register (B0, 0x01) by writing 0x88, when operation mode moved to TX mode operation to IDLE state. Register bit1 (INT[25]) in [INT_SOOURCE_GRP4] (B0, 0x27) have to be clear.
2. Wait more than 5us from PLL unlock detect before writing to register when bit7(PLL_LD_EN) gets enable.

0x12[CCA_IGNORE_LEVEL]

Function: ED threshold level to exclude CCA judgement
Address: 0x12
Default Value 0xFE

Bit	Symbol	Description	Default Value	R/W
7-0	IGNORE_LV[7:0]	ED threshold level to exclude CCA judgement.	1111_1110	R/W

[Detailed description]

1. Please refer to “CCA (Clear Channel Assesment)” section for more information.
2. If detected ED value exceed threshold value defined by this register, those values are excluded from averaging process defined by register bit2-0 (ED_AVG[2:0]) in [ED_CNTRL] register (B0, 0x1B). CCA status register bit1-0 (CCA_RST[1:0]) in [CCA_CNTRL] address (B0, 0x15) shows 0b11 (busy)

0x13[CCA_LEVEL]

Function: : Threshold level for CCA operation
Address: : 0x13
Default Value : 0x08

Bit	Symbol	Description	Default Value	R/W
7-0	CCA_TH_LV[7:0]	Thoreshold level for CCA operation (0 to 255)	0000_1000	R/W

[Detailed description]

1. Please refer to “CCA (Clear Channel Assesment)” section for more information.
2. If ED value exceed threshold level given by this register, status bit in [CCA_CNTRL] register (B0, 0x15) bit1-0 (CCA_RSLT) shows 0b01 (carrier found).

0x14[CCA_ABORT]

Function: Time parameter to terminate CCA operation during AUTO_ACK case.
Address: 0x14
Default Value 0xFF

Bit	Symbol	Description	Default Value	R/W
7-0	CCA_ABORT[6:0]	Time parameter to terminate CCA operation (0 to 255)	1111_1111	R/W

[Detail description]

1. Time out parameter in Auto_Ack mode. CCA operation may block Ack packet transmission until it finds clear channel. Please refer to “CCA (Clear Channel Assesment)” section for more information.
2. CCA operation will be maintained for time length given as “register value” x 17.8uS. If IDLE status detected, remaining packet data will be destroyed and RF block goes TRX_OFF state.
   (Note: time length given above is register [ADC_CLK_SET] register (B0, 0x08) is configured as Default Value (1.8MHz). If ADC_CLK is configured 2MHz, time length will be “register value” x 16usec.)

0x15[CCA_CNTRL]

Function: CCA control setting and reporting result
Address: 0x15
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7	CCA_AUTO_EN	Perform CCA operation in AUTO_ACK mode. (‘1’ : perform)	0	R/W
6	CCA_LOOP_STOP	Disable CCA loop (‘1’: disable)	0	R/W
5	CCA_LOOP_START	Perform CCA loop. (‘1’: perform) (*1)	0	R/W
4	CCA_EN	Enable CCA operation (‘1’ : enable) (*2)	0	R/W
3	CCA_IDLE_EN	CCA idle detection control 0: disable idle detection 1: enable idle detection	0	R/W
2	CCA_DONE	CCA complete flag (*4) 0: CCA is busy (or not started) 1: CCA completed	0	R
1-0	CCA_RSLT[1:0]	CCA result flag (*3) CCA_RSLT[1:0] = 11:CCA is busy (out of range detected) 10:CCA in judgement (IDLE detection in progress) 01:Carrier detected 00:No carrier detected	00	R

[Detail description]
1. Please refer to “CCA (Clear Channel Assesment)” section for more information.

*1 CCA operation will be repeated until CCA_LOOP_STOP bit disable it.
*2 CCA_EN bit will be cleared to 0b0 automatically.
*3 CCA_RSLT can be cleared manually when it is written as 0b00.
*4 Bit2 (CCA_DONE) operates in conjunction with [INT_SOURCE_GRP2] register (B0 0x25) bit0. Bit2 transitions to 0b1 (CCA completed) only when bit1-0 is 0b00 or 0b01.

[Note]
1. When you want to write access to the register after enabling bit7 (CCA_AUTO_EN), wait until the RF state setting (RF_STATUS) becomes 0x99 after the CCA detection is completed.

0x16[ED_RSLT]

Function: Readout register for ED (Energy Detection) values
Address: 0x16
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	ED_Value[7:0]	ED value	0000_0000	R

[Detail description]
1. Please refer to “Energy Detection (ED) function” section for more information.
2. ED vlaue will be updated when state move to RX_ON. [RF_STATUS] register (B0, x6C) bit[3:0] (SET_TRX[3:0]) to control RF status.

0x17[IDLE_WAIT_L]

Function: Time parameter to judge as IDLE state during CCA operation. (lower 8bits)
Address: 0x17
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	IDLE_WAIT[7:0]	Maximam wait time for IDLE detection. (lower 8bits)	0000_0000	R/W

[Detail description]

1. Please refer to “CCA (Clear Channel Assesment)” section for more information.
2. Wait for IDLE detection performing CCA operation.
   ED value averaging time (8 x T_{ADC}) + (“register value” x T_{ADC}) [uS]
   T_{ADC} = 17.6 uS (default ADC clock is 1.8MHz), 16.0us (ADC clock is 2.0MHz)
   Number of aceraging process ‘8’ is default.

0x18[IDLE_WAIT_H]

Function: Time parameter to judge as IDLE state during CCA operation (upper 2bits)
Address: 0x18
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-2	Reserved	Reserved	0000_00	R/W
1-0	IDLE_WAIT[9:8]	Maximam wait time for IDLE detection (upper 2bits)	00	R/W

[Detail description]

1. Please refer to “CCA (Clear Channel Assesment)” section for more information.
2. Wait for IDLE detection performing CCA operation.
   ED value averaging time (8 x T_{ADC}) + (“register value” x T_{ADC}) [uS]
   T_{ADC} = 17.6 uS (default ADC clock is 1.8MHz), 16.0us (ADC clock is 2.0MHz)
   Number of aceraging process ‘8’ is default.

0x19[CCA_PROG_L]

Function: Elapsed time as IDLE state during CCA operation (lower 8bits)
Address: 0x19
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	CCA_PROG [7:0]	Elapsed time as IDLE state during CCA operation (lower 8bits)	0000_0000	R

[Detail description]

1. Please refer to “CCA (Clear Channel Assesment)” section for more information.
2. This register shows elapsed time of IDLE detection.
   ED value averaging time (8 x T_{ADC}) + (“register value” x T_{ADC}) [uS]
   T_{ADC} = 17.6 uS (default ADC clock is 1.8MHz), 16.0us (ADC clock is 2.0MHz)
   Number of aceraging process ‘8’ is default.

0x1A[CCA_PROG_H]

Function: Elapsed time as IDLE state during CCA operation (upper 2bits)
Address: 0x1a
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-2	Reserved	Reserved	0000_00	R
1-0	CCA_PROG[9:8]	Elapsed time as IDLE state during CCA operation (upper 2bits)	00	R

[Detail description]

1. Please refer to "CCA (Clear Channel Assesment)" section for more information.
2. This register shows elapsed time of IDLE detection.
   ED value averaging time (8 x T_{ADC}) + ("register value" x T_{ADC}) [uS]
   T_{ADC} = 17.6 uS (default ADC clock is 1.8MHz), 16.0us (ADC clock is 2.0MHz)
   Number of aceraging process '8' is default.

0x1B[ED_CNTRL]

Function: ED (Energy Detection) control
Address: 0x1b
Default Value 0x83

Bit	Symbol	Description	Default Value	R/W
7	ED_CALC_EN	Control of ED value computation 0: ED value is not computed 1: ED value is computed	1	R/W
6-5	Reserved	Reserved	00	R/W
4	ED_DONE	Completion flag for ED value computation 0: Busy 1: Completed	0	R
3	Reserved	Reserved	0	R/W
2-0	ED_AVG[2:0]	Number of averaging process for ED value computation (*1)	011	R/W

[Detail description]

1. Please refer to "Energy Detection (ED) function" section for more information.

*1 Following table shows number of ED value averaging samples

ED_AVG[2:0]	Number of averaging samples
0b000	1
0b001	2
0b010	4
0b011 (Default Value)	8
0b100	15
0b101	16
Otherwise	8

[Note] Set ED_AVG[2:0] while the ED value is not being calculated (in TRX_OFF or TX_ON state or ED_CALC_EN is 0).

0x1C[GAIN_MtoL]

Function: Threshold level to switch from middle gain to low gain
Address: :0x1c

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5-0	GC_TRIM_ML[5:0]	Threshold level for gain control	01_1110	R/W

[Detail description]
1. Please refer to “Energy Detection (ED) value adjustment” section for more information.

[Note]
1. Please do not change this register value given by “Initial register setting” file
2. GC_TRIM_ML has to be greater than GC_TRIM_LM

0x1D[GAIN_LtoM]

Function: Threshold level to switch from low gain to middle gain
Address: :0x1d
Default Value :0x03

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5-0	GC_TRIM_LM[5:0]	Threshold level for gain control	00_0011	R/W

[Detail description]
1. Please refer to “Energy Detection (ED) value adjustment” section for more information.

[Note]
1. Please do not change this register value given by “Initial register setting” file
2. GC_TRIM_ML has to be greater than GC_TRIM_LM

0x1E[GAIN_HtoM]

Function: Gain update setting and threshold level to switch from high gain to middle gain
Address: 0x1e
Default Value 0x9E

Bit	Symbol	Description	Default Value	R/W
7	GC_FIX_EN	Gain control (*1) 0: Always update gain mode 1: Fix gain after synchronization to received signal established in DEMOD block.	1	R/W
6	Reserved	Reserved	00	R/W
5-0	GC_TRIM_HM[5:0]	Threshold level for gain control	1_1110	R/W

[Detail description]
1. Please refer to “Energy Detection (ED) value adjustment” section for more information.

[Note]
1. Please do not change this register value given by “Initial register setting” file
2. GC_TRIM_HM has to be greated than GC_TRIM_MH

*1 GC_FIX_EN has to be 0b0 during BER measurement

0x1F[GAIN_MtoH]

Function: Threshold level to switch from middle gain to high gain
Address: 0x1f
Default Value 0x03

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5-0	GC_TRIM_MH[5:0]	Threshold level for gain control	00_0011	R/W

[Detail description]
1. Please refer to “Energy Detection (ED) value adjustment” section for more information.

[Note]
1. Please do not change this register value given by “Initial register setting” file
2. GC_TRIM_HM has to be greated than GC_TRIM_MH

0x20[RSSI_ADJ_M]

Function: RSSI offset value in middle gain range
Address: 0x20
Default Value 0x19

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5-0	RSSI_OFFSET_M[5:0]	RSSI offset value in middle gain range	01_1001	R/W

[Detail description]
1. Please refer to “Energy Detection (ED) value adjustment” section for more information.

[Note]
1. Please do not change this register value given by “Initial register setting” file

0x21[RSSI_ADJ_L]

Function: RSSI offset value in low gain range
Address: 0x21
Default Value 0x37

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5-0	RSSI_OFFSET_L[5:0]	RSSI offset value in low gain range	11_0111	R/W

[Detail description]
1. Please refer to “Energy Detection (ED) function” section for more information

[Note]
1. Please do not change this register value given by “Initial register setting” file

0x22[RSSI_STABLE_TIME]

Function: Time parameter for RSSI value become stable after gain switch
Address: 0x22
Default Value 0x03

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5-4	AD_MASK_SET[1:0]	RSSI convergence wait setting (*2)	00	R/W
3-0	RSSI_STABLE[3:0]	Settling time of RSSI conversion after gain switch. (1 to 15) (*1)	0011	R/W

[Detail description]
*1 ED value detection will not use RSSI value in this period, as it is settling time for RSSI conversion block. RSSI stabilization time is calculated by Setting value + 1 x A/D conversion zone (17.8us[at 1.8MHz]
*2 or 16us[at 2MHz]. This function can be used with ED value detection and diversity mode, but it will not be available for CCA operation.Wait time for convergence of the RSSI value output from the RSSI circuit, not executing the next gain switching. The wait time from the last gain switching is calculated by (Setting value + 2) x A/D conversion zone (17.8us[at 1.8MHz] or 16us[at 2MHz].

[Note]
1. Do not set 0x00. Please do not change this register value given by “Initial register setting” file

0x23[RSSI_VAL_ADJ]

Function: RSSI scale factor for ED value conversion.
Address: 0x23
Default Value 0x50

Bit	Symbol	Description	Default Value	R/W
7-4	RSSI_VAL_M[3:0]	RSSI scale factor (0 to 15) (Default Value x5)	0101	R/W
3	RSSI_VAL_D3	RSSI scale factor x1/8 (applied when it is '1')	0	R/W
2	RSSI_VAL_D2	RSSI scale factor x1/4 (applied when it is '1')	0	R/W
1	RSSI_VAL_D1	RSSI scale factor x1/2 (applied when it is '1')	0	R/W
0	RSSI_VAL_D0	RSSI scale factor x1/1 (applied when it is '1')	0	R/W

[Note]

1. Please refer to "Energy Detection (ED) value adjustment" section for more information
2. Do not set 0x00. Please do not change this register value given by "Initial register setting" file
3. One of bit3 to bit0 are allowed to active. Bit3 has higher priority than bit2, and so on.
4. 0x00 in this register is equal to x1

Example)
Bit[7:0] = 0b01000010 = x2, bit[7:4]=0b0100= x4, bit[3:0]=0b0010=1/2.

0x24[INT_SOURCE_GRP1]

Function: FIFO clear setting, interrupt status for INT05 to INT00
Address: 0x24
Default Value 0x01

Bit	Symbol	Description	Default Value	R/W
7	FIFO_CLR1	FIFO bank1 clear (*1) 0: No data in FIFO (execute FIFO clear) 1: FIFO has data to clear	0	R/W
6	FIFO_CLR0	FIFO bank0 clear (*2) 0: No data in FIFO (exectute FIFO clear) 1: FIFO has data to clear	0	R/W
5	INT[05]	Interrupt by FIFO_FULL (*3) 0: No interrupt 1: Interrupt taken place	0	R/W
4	INT[04]	Interrupt by FIFO_EMPTY (*4) 0: No interrupt 1: Interrupt taken place	0	R/W
3	INT[03]	Interrupt by packet abort completion in address filtering function (*5) 0: No interupt 1: Interrupt taken place	0	R/W
2	INT[02]	Interrupt by VCO calibration complete 0: No interrupt 1: Interrupt taken place	0	R/W
1	INT[01]	Reserved	0	R/W
0	INT[00]	Interrupt by CLK stabilization complete 0: No interrupt 1: Interrupt taken place	1	R/W

[Detail description]

*1 FIFO bank1 will be cleared when FIFO clear function is executed. Received data will be written into FIFO bank1, and it will be available to read by SPI. If SPI read started, this bit become '1'. By writing '0', it will be cleared.

*2 FIFO bank0 will be cleared when FIFO clear function is executed. Received data will be written into FIFO bank0, and it will be available to read by SPI. If SPI read started, this bit become '1'. By writing '0', it will be cleared.

*3 Interrupt will be taken place when TX or RX FIFO remaining size is larget than threshold level given by [TX_ALARM_LH] or [RX_ALARM_LH] register (B0, 0x35 or 0x37)

*4 Interrupt will be taken place when TX or RX FIFO remaining size is smaller than threshold level given by [TX_ALARM_HL] or [RX_ALARM_HL] register (B0, 0x36 or 0x38)

*5 Interrupt will be taken place when Received packet abort completed by Address filtering function.

[Note]

1. Those registers are active independent from [INT_EN_GRP1] register (B0, 0x2a). Writing 0b0 to each bit is available, no action taken place if writing 0b1.
2. bit7(FIFO_CLR1) and bit6(FIFO_CLR0) are independent from [INT_EN_GRP1] register. No interrupt reporting function.
3. Do not clear FIFO if FIFO read completed properly.
4. If an unmasked interrupt source has been taken place, SINTN (Pin #10) continues to output Low.

0x25[INT_SOURCE_GRP2]

Function: Interrupt status for INT15 to INT8
Address: 0x25
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7	INT[15]	Interrupt by TX FIFO access error (*1) 0: No interrupt 1: Interupt taken place	0	R/W
6	INT[14]	Interrupt by RX FIFO access error (*2) 0: No interrupt 1: Interrupt taken place	0	R/W
5	INT[13]	Interrupt by TX Length error (*3) 0: No interrupt 1: Interrupt taken place	0	R/W
4	INT[12]	Interrupt by RX Length error (*4) 0: No interrupt 1: Intrrupt taken place	0	R/W
3	INT[11]	Interupt by SFD detection (*5) 0: No interrupt 1: Interrupt taken place	0	R/W
2	INT[10]	Interrupt by RF state transition complete (*6) 0: No interrupt 1: Interrupt taken place	0	R/W
1	INT[09]	Interrupt by diversity detection complete 0: No interrupt 1: Interrupt taken place	0	R/W
0	INT[08]	Interrupt by CCA detection complete 0: No interrupt 1: Interrupt taken place	0	R/W

[Detail description]

*1 If writing transmit packet data which has larger size than 2banks of buffer size, and TX FIFO has no more space to write, intrrupt will take place when third packet (packet length shorter than 256byte) or FIFO has no moredata.

*2 If writing received packet data which has larger size than 2banks of buffer size, and RX FIFO has no more space to write, interrupt will take place.

*3 This interrupt will be valid only if [PACKET_MODE_SET] register (B0, 0x45) bit1 (IEEE_MODE) is 0b0（IEEE802．15．4d）. If value grater than 129byte is written in TX Length field , interrupt will take place.

*4 This interrupt will be valid only if [PACKET_MODE_SET] register (B0, 0x45) bit1 (IEEE_MODE) is 0b0（IEEE802．15．4d）. If value grater than 129byte is written in RX Length field, interrupt will take place.

*5 In preamble data and SFD field detecion, nterrupt will take place when data include smaller amount of error bits defined in [SYNC_CONDITION] register (B0, 0x44).

*6 Interrupt will take place when state transition which is configured in [RF_STATUS] register (B0, 0x6c) bit[2:0] (SET_TRX[2:0]), are completed.

[Note]

1. Those registers are active independent from [INT_EN_GRP2] register (B0, 0x2a). Writing 0b0 to each bit is available, no action taken place if writing 0b1.

0x26[INT_SOURCE_GRP3]

Function: Interrupt status for INT23 to INT16
Address: 0x26
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7	INT[23]	Interrupt by FIFO1 data TX REQ accepted (*1) 0: No interrupt 1: Interrupt taken place	0	R/W
6	INT[22]	Interrupt by FIFO0 data TX REQ accepted (*2) 0: No interrupt 1: Interrupt taken place	0	R/W
5	INT[21]	Interrupt by CRC error detected in RX FIFO1 data (*3) 0: No interrupt 1: Interrupt taken place	0	R/W
4	INT[20]	Interrupt by CRC error deteced in RX FIFO0 data (*4) 0: No interrupt 1: Interrupt taken place	0	R/W
3	INT[19]	Inerrupt by FIFO1 data reception completed (*5) 0: No interrupt 1: Interrupt taken place	0	R/W
2	INT[18]	Interrupt by FIFO0 data reception completed (*6) 0: No interrupt 1: Interrupt taken place	0	R/W
1	INT[17]	Interrupt by FIFO1 data transmission completed (*7) 0: No interrupt 1: Interrupt taken place	0	R/W
0	INT[16]	Interrupt by FOFO0 data transmission completed (*8) 0: No interrupt 1: Interrupt taken place	0	R/W

[Detail description]

*1 Interrupt occurs when a specified Length of transmitted data is stored to FIFO1.
If 0b0 is written to [PD_DATA_REQ] register bit5 (PD_DATA_REQ1) for clearance, this bit is also cleared.

*2 Interrupt occurs when a specified Length of transmitted data is stored to FIFO1.
If 0b0 is written to [PD_DATA_REQ] register bit1 (PD_DATA_REQ1) for clearance, this bit is also cleared.

*3 Interrupt will take place when received data written in FIFO1 results with CRC error.
If [PD_DATA_IND] register (B0, 0x29) bit4 (CRC_RSLT1) is cleard by 0b0, this bit will be cleared.
If data cannot be received during reception after SFD due to drastic change of radio wave intensity and so on, it is notified of by this interrupt.

*4 Interrupt will take place when received data written in FIFO0 results with CRC error.
If [PD_DATA_IND] register (B0, 0x29) bit0 (CRC_RSLT0) is cleared by 0b0, this bit will be cleared.
If data cannot be received during reception after SFD due to drastic change of radio wave intensity and so on, it is notified of by this interrupt.

*5 Interrupt will take place when receiving data into FIFO1 completed.
If [PD_DATA_IND] register (B0, x29) bit5 (PD_DATA_IND1) is cleared by 0b0, this bit will be cleared.

*6 Interrupt will take place when receiveing data into FIFO0 completed.
If [PD_DATA_IND] register (B0, x29) bit1 (PD_DATA_IND0) is cleared by 0b0, this bit will be cleared.

*7 Interrupt will take place when transmission of data in FIFO1 completed.
If [PD_DATA_REQ] register (B0, x29) bit4 (PD_DATA_CFM1) is cleared by 0b0, this bit will be cleard.

*8 Interrupt will take place when transmission of data in FIFO0 completed.
If [PD_DATA_REQ] register (B0, x29) bit0 (PD_DATA_CFM0) is cleared by 0b0, this bit will be cleared.

[Note]

1. Those registers are active independent from [INT_EN_GRP3] register (B0, 0x2c). Writing 0b0 to each bit is available, no action taken place if writing 0b1.

0x27[INT_SOURCE_GRP4]

Function: Interrupt status for INT25 to INT24
Address: 0x27
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-2	Reserved	Reserved	0000_00	R/W
1	INT[25]	Interrupt by PLL unlock detection (*1) 0: No interrupt 1: Interrupt taken place	0	R/W
0	INT[24]	Interrupt by Auto_Ack ready (*2) 0: No interrupt 1: Interrupt taken place	0	R/W

[Detail description]
*1 Interrupt will take place when PLL unlock is detected while TRX status.
*2 This bit will be valid when [AUTO_ACK_SET] register (B0, 0x55) bit4 (AUTO_ACK_EN) is written as 0b1,and Auto_Ack is configured. While receiving Ack request packet, and when TX Ack packet become ready to send and TX_ON is activated.

[Note]
1. Those registers are active independent from [INT_EN_GRP4] register (B0, 0x2d). Writing 0b0 to each bit is available, no action taken place if writing 0b1.

0x28[PD_DATA_REQ]

Function: Data transmission request
Address: 0x28
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5	PD_DATA_REQ1	Data transmission request from FIFO1 (1: TX reqested) (*1)	0	R/W
4	PD_DATA_CFM1	Status data transmission from FIFO1 0: Not transmitted yet or under transmitting 1: Transmission completed	0	R/W
3-2	Reserved	Reserved	00	R/W
1	PD_DATA_REQ0	Data transmission request from FIFO0 (1: TX requested) (*1)	0	R/W
0	PD_DATA_CFM0	Stauts data transmission from FIFO0 0: Not transmitted yet or under transmitting 1: Transmission completed	0	R/W

[Note]
*1 PD_DATA_REQ bits will be automatically set to 0b1 when writing to TX data into FIFO is completed.

Only 0 can be written to each bit of this register.

0x29[PD_DATA_IND]

Function: Data reception reporting
Address: 0x29
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5	PD_DATA_IND1	Data reception to FIFO1 completed *1 0: Under receiving or no received data 1: Receive completed	0	R/W
4	CRC_RSLT1	CRC result status received data in FIFO1 *2 0: CRC error 1: CRC is OK	0	R/W
3-2	Reserved	Reserved	00	R/W
1	PD_DATA_IND0	Data reception to FIFO0 completed *1 0: Under receiving or no received data 1: Receive completed	0	R/W
0	CRC_RSLT0	CRC results for received data in FIFO0 *2 0: CRC error 1: CRC is OK	0	R/W

[Note]
1. This register will be available to access if [CLK_SET] register (B0, 0x02) bit0 (CLK0_EN) is 0b1.

*1 This bit will not be cleared automatically even reading all received data are read out from FIFO by MCU.This bit will be cleared by writting 0b0. Writing 0b1 cause no action.
*2 CRC_RSLT bits will not be cleared automatically. CRC computation results by next received data overwrite those bits. This bit will be cleared by writing 0b0. Writing 0b1 cause no action.
If 0b0 is written to this bit, CRC error interrupt display in [INT_SOURCE_GRP3] register (B0 0x26) bit5-4 is retained. Clear the CRC error interrupt display in [INT_SOURCE_dGRP3] register.

0x2A[INT_EN_GRP1]

Function: Interrupt mask for INT03 to INT00
Address: 0x2a
Default Value 0xFF

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	11	R/W
5-0	INT_EN [05:00]	Interrupt mask for INT05 to INT00 0: No interrupt reporting 1: Interrupt enabled	11_1111	R/W

[Detail description]
1. Detail of interrupt source is described in [INT_SOURCE_GRP1] register (B0, 0x24)

0x2B[INT_EN_GRP2]

Function: Interrupt mask for INT15 to INT08
Address: 0x2b
Default Value 0xFF

Bit	Symbol	Description	Default Value	R/W
7-0	INT_EN[15:08]	Interrupt mask for INT15 to INT08 0: No interrupt reporting 1: Interrupt enabled	1111_1111	R/W

[Detail description]

1. Detail of interrupt source is described in [INT_SOURCE_GRP2] register (B0, 0x25)

0x2C[INT_EN_GRP3]

Function: Interrupt mask for INT23 to INT16
Address: 0x2c
Default Value 0xFF

Bit	Symbol	Description	Default Value	R/W
7-0	INT_EN[23:16]	Interrupt mask for INT15 to INT08 0: No interrupt reporting 1: Interrupt enabled	1111_1111	R/W

[Detail description]

1. Detail of interrupt source is described in [INT_SOURCE_GRP3] register (B0, 0x26)

0x2D[INT_EN_GRP4]

Function: Interrupt mask for INT25 and INT24.
Address: 0x2d
Default Value 0x03

Bit	Symbol	Description	Default Value	R/W
7-2	Reservef	Reserved	0000_00	R/W
1	INT_EN[25]	Interrupt mask for INT25 0: No interrupt reporting 1: Interrupt enabled	1	R/W
0	INT_EN[24]	Interrupt mask for INT24 0: No interrupt reporting 1: Interrupt enabled	1	R/W

[Detail description]

1. Detail of interrupt source is described in [INT_SOURCE_GRP4] register (B0, 0x27)

0x2E[CH_EN_L]

Function: Channel enable setting for lower 8ch.
Address: 0x2e
Default Value 0xFF

Bit	Symbol	Description	Default Value	R/W
7	CH7_EN	Channel 7 enable (1: enabled)	1	R/W
6	CH6_EN	Channel 6 enable (1: enabled)	1	R/W
5	CH5_EN	Channel 5 enable (1: enabled)	1	R/W
4	CH4_EN	Channel 4 enable (1: enabled)	1	R/W
3	CH3_EN	Channel 3 enable (1: enabled)	1	R/W
2	CH2_EN	Channel 2 enable (1: enabled)	1	R/W
1	CH1_EN	Channel 1 enable (1: enabled)	1	R/W
0	CH0_EN	Channel 0 enable (1: enabled)	1	R/W

[Detail description]

1. See section “Programming Channel frequency”
2. [CH_SET] register (B0, 0x6b) configure channel used in TX/RX.

0x2F[CH_EN_H]

Function: Channel enable setting for upper 8ch.
Address: 0x2f
Default Value 0xFF

Bit	Symbol	Description	Default Value	R/W
7	CH15_EN	Channel 15 enable (1: enabled)	1	R/W
6	CH14_EN	Channel 14 enable (1: enabled)	1	R/W
5	CH13_EN	Channel 13 enable (1: enabled)	1	R/W
4	CH12_EN	Channel 12 enable (1: enabled)	1	R/W
3	CH11_EN	Channel 11 enable (1: enabled)	1	R/W
2	CH10_EN	Channel 10 enable (1: enabled)	1	R/W
1	CH9_EN	Channel 9 enable (1: enabled)	1	R/W
0	CH8_EN	Channel 8 enable (1: enabled)	1	R/W

[Detail description]

1. See section “Programming Channel frequency”
2. [CH_SET] register (B0, 0x6b) configure channel used in TX/RX.

0x30[IF_FREQ_AFC_H]

Function: :IF frequency setting in AFC mode. (upper 8bits)
Address: :0x30
Default Value :0x1C

Bit	Symbol	Description	Default Value	R/W
7-0	IF_FREQ_AFC[15:8]	IF frequency setting in AFC mode (bit15 to bit8)	0001_1100	R/W

[Detail description]
1. This register will be valid only if [AFC_CNTRL] register (B0 0x34) bit0 (AFC_EN) is 0b1
2. It configures IF frequency while AFC function is active. Afer AFC function finished, IF frequencies defined by [IF_FREQ_H] and [IF_FREQ_L] (B1, 0x0a and 0x0b) will be used.
3. Adjustment of IF frequency depending on data rate in use will be updated automatically. Data rate is configured in [DATA_SET] register (B0, 0x47) bit2-0(RATE[2:0])

[Note]
1. See section “IF frequency setting”.

0x31[IF_FREQ_AFC_L]

Function: IF frequency setting in AFC mode (lower 8bits)
Address: 0x31
Default Value 0x71

Bit	Symbol	Description	Default Value	R/W
7-0	IF_FREQ_AFC[7:0]	IF frequency setting in AFC mode (bit7 to bit0)	0111_0001	R/W

[Detail description]
1. This register will be valid only if [AFC_CNTRL] register (B0 0x34) bit0 (AFC_EN) is 0b1.
2. It configures IF frequency while AFC function is active. Afer AFC function finished, IF frequencies defined by [IF_FREQ_H] and [IF_FREQ_L] (B1, 0x0a and 0x0b) will be used.
3. Adjustment of IF frequency depending on data rate in use will be updated automatically. Data rate is configured in [DATA_SET] register (B0, 0x47) bit2-0(RATE[2:0])

[Note]
1. See section “IF frequency setting”.

0x32[BPF_AFC_ADJ_H]

Function: Capacitor trimming of bandpass filter in AFC mode operation (upper 2bits)
Address: 0x32
Default Value 0x01

Bit	Symbol	Description	Default Value	R/W
7-2	Reserved	Reserved	0000_00	R/W
1-0	BPF_C_AFC[9:8]	Capacitor trimming of bandpass filter in AFC mode operation (bit9, bit8)	01	R/W

[Detail description]
1. This register will be valid only if [AFC_CNTRL] register (B0 0x34) bit0 (AFC_EN) is 0b1.
2. It adjust bandwidth of BPF while AFC function is active. Afer AFC function finished, bandwidth of BPF defined by [BPF_ADJ_H] and [BPF_ADJ_L] (B1, 0x0e and 0x0f) will be used.

[Note]
1. See section “BPF_ADJ adjustment method”

0x33[BPF_AFC_ADJ_L]

Function: Capacitor trimming of bandpass filter in AFC mode operation (lower 8bits)
Address: 0x33
Default Value 0x9c

Bit	Symbol	Description	Default Value	R/W
7-0	BPF_C_AFC[7:0]	Capacitor trimming of bandpass filter in AFC mode operation (bit7 to bit0)	1001_1100	R/W

[Detail description]
1. This register will be valid only if [AFC_CNTRL] register (B0 0x34) bit0 (AFC_EN) is 0b1.
2. It adjust bandwidth of BPF while AFC function is active. Afer AFC function finished, bandwidth of BPF defined by [BPF_ADJ_H] and [BPF_ADJ_L] (B1, 0x0e and 0x0f) will be used.

[Note]
1. See section “BPF_ADJ adjustment method”

0x34[AFC_CNTRL]

Function: AFC mode configuration
Address: 0x34
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7	Reserved	Reserved	0	R/W
6	AFC_UPDATE_EN	AFC update 0: No AFC update 1: AFC update enabled	0	R/W
5-4	UPDATE_TERM[1:0]	Interval of AFC update (*1) UPDATE_TERM[1:0] = 00: 8 symbols 01: 16 symbols 10: 32 symbols 11: 64 symbols	00	R/W
3-1	Reserved	Reserved	000	R/W
0	AFC_EN	AFC mode control 0: AFC mode disabled 1: AFC mode enabled	0	R/W

[Detail description]
*1 Update timing will be varied depending on data rate given by [DATA_SET] register (B0 0x47).

[Note]
1. For this register, set a value specified in "Initial setting registers" and do not change it for adjustment.

0x35[TX_ALARM_LH]

Function: Alert level setting for remaining size of TX FIFO (alerm for FIFO full)
Address: 0x35
Default Value 0xF0

Bit	Symbol	Description	Default Value	R/W
7-0	TX_ALARM_LH[7:0]	Alert level setting for remaining size of TX FIFO (alerm for FIFO full) Range 0-255 byte (Default Value 240 bytes)	1111_0000	R/W

[Detail description]

1. See section “Managing TX FIFO remaining size”
2. If amount of data remaining in TX FIFO is bigger than level given by this register, INT[5] in interrupt group1 will be generated and asser SINTN (#10pin) to low.

0x36[TX_ALARM_HL]

Function: Alert level setting for remaining size of TX FIFO (alerm for TX empty)
Address: 0x36
Default Value 0x0F

Bit	Symbol	Description	Default Value	R/W
7-0	TX_ALARM_HL[7:0]	Alert level setting for remaining size of TX FIFO (alerm for FIFO empty) Range 0-255 byte. (Default Value 31bytes)	0000_1111	R/W

[Detail description]

1. See section “Managing TX FIFO remaining size”
2. If amount of data remaining in TX FIFO is smaler than given by this register, INT[4] in interrupt group1 will be generated and assert SINTN (#10pin) to low.

0x37[RX_ALARM_LH]

Function: Alert level setting for remaing size of RX FIFO (alerm for RX full)
Address: 0x37
Default Value 0x05

Bit	Symbol	Description	Default Value	R/W
7-0	RX_ALARM_LH[7:0]	Alert level setting for remaining size of RX FIFO (alerm for FIFO full) Range 0-255 byte (Default Value 5 bytes)	000_0101	R/W

[Detail description]

1. See section “Managing RX FIFO remaining size”
2. If amount of data remaining in RX FIFO is bigger than level given by this register, INT[5] in interrupt group1 will be generated and asser SINTN (#10pin) to low.

0x38[RX_ALARM_HL]

Function: Alert level setting for remaing size of RX FIFO (alerm for RX empty)
Address: 0x38
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	RX_ALARM_HL[6:0]	Alert level setting for remaining size of RX FIFO (alerm for FIFO empty) Range 0-255 byte. (Default Value 0byte)	000_0000	R/W

[Detail description]

1. See section “Managing RX FIFO remaining size”
2. If amount of data remaining in RX FIFO is smaler than given by this register, INT[4] in interrupt group1 will be generated and assert SINTN (#10pin) to low.

0x39[PREAMBLE_SET]

Function: Preamble pattern setting for TX/RX operation
Address: 0x39
Default Value 0x55

Bit	Symbol	Description	Default Value	R/W
7-0	PR[7:0]	Preamble pattern (1st byte fixed) setting	0101_0101	R/W

[Detail description]

1. Preamble pattern has to be repetitive pattern which can be used for radio synchronization. Either 0xAA or 0x55 are ued. If it is used in IEEE802.15.4d/g, 0xAA needs to be set.
2. LSB first
3. Length of frame synchronization pattern during TX mode is configured in [TX_PR_LEN] register (B0, 0x42). Comparison length of frame synchronization pattern durin RX mode is configured in [RX_PR_LEN/SFD_LEN] register (B0 0x43).

0x3A[SFD1_SET1]

Function: Frame synchronization pattern (max 4bytes) of 1st byte of 1st pattern
SFD: Start of Frame Delimiter
Address: 0x3a
Default Value 0xA7

Bit	Symbol	Description	Default Value	R/W
7-0	SFD1[7:0]	Frame synchronization pattern (max 4bytes) of 1st byte of 1st pattern	1010_0111	R/W

[Detail description]

1. See section “SFD detection function”
2. 1st pattern of SFD is valid if [PACKET_MODE_SET] register (B0, 0x45) bit6 (MRFSKFSD) is 0b0.
3. LSB first
4. Valid length of SFD field is configured in [RX_PR_LEN/SFD_LEN] register (B0, 0x43).

0x3B[SFD1_SET2]

Function: Frame synchronization pattern (max 4byte) of 2nd byte of 1st pattern
Address: 0x3b
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	SFD1[15:8]	Frame synchronization pattern (max 4bytes) of 2nd byte of 1st pattern	0000_0000	R/W

[Detail description]

1. See section “SFD detection function”
2. 1st pattern of SFD is valid if [PACKET_MODE_SET] register (B0, 0x45) bit6 (MRFSKFSD) is 0b0.
3. LSB first
4. Valid length of SFD field is configured in [RX_PR_LEN/SFD_LEN] register (B0, 0x43).

0x3C[SFD1_SET3]

Function: Frame synchronization pattern (max 4byte) of 3rd byte of 1st pattern
Address: 0x3c
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	SFD1[23:16]	Frame synchronization pattern (max 4bytes) of 3rd byte of 1st pattern	0000_0000	R/W

[Detail description]

1. See section “SFD detection function”
2. 1st pattern of SFD is valid if [PACKET_MODE_SET] register (B0, 0x45) bit6 (MRFSKFSD) is 0b0.
3. LSB first
4. Valid length of SFD field is configured in [RX_PR_LEN/SFD_LEN] register (B0, 0x43).

0x3D[SFD1_SET4]

Function: Frame synchronization pattern (max 4byte) of 4th byte of 1st pattern
Address: 0x3d
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	SFD1[31:24]	Frame synchronization pattern (max 4bytes) of 4th byte of 1st pattern	0000_0000	R/W

[Detail description]

1. See section “SFD detection function”
2. 1st pattern of SFD is valid if [PACKET_MODE_SET] register (B0, 0x45) bit6 (MRFSKFSD) is 0b0.
3. LSB first
4. Valid length of SFD field is configured in [RX_PR_LEN/SFD_LEN] register (B0, 0x43).

0x3E[SFD2_SET1]

Function: Frame synchronization pattern (max 4byte) of 1st byte of 2nd pattern
SFD: Start of Frame Delimiter
Address: 0x3e
Default Value 0xA7

Bit	Symbol	Description	Default Value	R/W
7-0	SFD2[7:0]	Frame synchronization pattern (max 4bytes) of 1st byte of 2nd pattern	1010_0111	R/W

[Detail description]
1. See section “SFD detection function”
2. 1st pattern of SFD is valid if [PACKET_MODE_SET] register (B0, 0x45) bit6 (MRFSKFSD) is 0b1.
3. LSB first
4. Valid length of SFD field is configured in [RX_PR_LEN/SFD_LEN] register (B0, 0x43).

0x3F[SFD2_SET2]

Function: Frame synchronization pattern (max 4byte) of 2nd byte of 2nd pattern
Address: 0x3f
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	SFD2[15:8]	Frame synchronization pattern (max 4bytes) of 2nd byte of 2nd pattern	0000_0000	R/W

[Detail description]
1. See section “SFD detection function”
2. 1st pattern of SFD is valid if [PACKET_MODE_SET] register (B0, 0x45) bit6 (MRFSKFSD) is 0b1.
3. LSB first
4. Valid length of SFD field is configured in [RX_PR_LEN/SFD_LEN] register (B0, 0x43).

0x40[SFD2_SET3]

Function: Frame synchronization pattern (max 4byte) of 3rd byte of 2nd pattern
Address: 0x40
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	SFD2[23:16]	Frame synchronization pattern (max 4bytes) of 3rd byte of 2nd pattern	0000_0000	R/W

[Detail description]
1. See section “SFD detection function”
2. 1st pattern of SFD is valid if [PACKET_MODE_SET] register (B0, 0x45) bit6 (MRFSKFSD) is 0b1.
3. LSB first
4. Valid length of SFD field is configured in [RX_PR_LEN/SFD_LEN] register (B0, 0x43).

0x41[SFD2_SET4]

Function: Frame synchronization pattern (max 4byte) of 4th byte of 2nd pattern
Address: 0x41
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	SFD2[31:24]	Frame synchronization pattern (max 4bytes) of 4th byte of 2nd pattern	0000_0000	R/W

[Detail description]

1. See section “SFD detection function”
2. 1st pattern of SFD is valid if [PACKET_MODE_SET] register (B0, 0x45) bit6 (MRFSKFSD) is 0b1.
3. LSB first
4. Valid length of SFD field is configured in [RX_PR_LEN/SFD_LEN] register (B0, 0x43).

0x42[TX_PR_LEN]

Function: TX preamble length (max 255 byte)
Address: 0x42
Default Value 0x04

Bit	Symbol	Description	Default Value	R/W
7-0	TXPR_LEN[7:0]	Preamble length in TX mode. (Max 255 bytes) Range 0-255 bytes (Default Value 4bytes)	0000_0100	R/W

[Note]

IEEE 802.15.4g standard defines “phyFSKPreambleRepetitions” parameter from 4. It is recommended not to use value below 4.

This setting value needs to be changed according to the data rate setting when the diversity is used. For details on the setting value supported for the data rate, refer to "Initial setting registers."

0x43[RX_PR_LEN / SFD_LEN]

Function: RX preamble comparison length (max 15byte) and SFD length setting
Address: 0x43
Default Value 0x02

Bit	Symbol	Description	Default Value	R/W
7-4	RX_PR_LEN[3:0]	Preamble comarison length in RX mode. [Setting value] byte is set. (The initial value 0b0000 is handled as 1-byte length. 0b0101 or larger values are handled as 4-byte length.)	0000	R/W
3	RX_PB_DISABLE (*2)	Received preamble two banks wait setting bit 0: Use the pattern set in [PREAMBLE_SET] register (B0 0x39) for SFD detection 1: Use either 0xAA or 0x55 pattern for SFD detection	0	R/W
2-0	SFD_LEN[2:0] (*1)	SFD field length in TX mode (LSB first) 0b001: SFD[7:0] will be used 0b010: SFD[15:0] will be used (default) 0b011: SFD[23:0] will be used 0b100: SFD[31:0] will be used	010	R/W

[Note]
*1 SFD comparison function is invalid if other combination of SFD_LEN is configured.
*2 When this bit is set to two banks wait, the number of allowable error bits for preamble detection in [SYNC_CONDITION] register (B0 0x44) bit3-0 (PB_SYNC[3:0]) is disabled and it is assumed as 0. When you enable this bit, set RX_PR_LEN[3:0] to 2 bytes or less.

0x44[SYNC_CONDITION]

Function: Tolerance of error bit in RX preamble detection and SFD detection (max 15bits)
Address: :0x44
Default Value :0x00

Bit	Symbol	Description	Default Value	R/W
7	SFD_SYNC[3]	Allowable error bits in SFD detection Range 0 to 15bits	0	R/W
6	SFD_SYNC[2]		0	R/W
5	SFD_SYNC[1]		0	R/W
4	SFD_SYNC[0]		0	R/W
3	PR_SYNC[3]	Allowable error bits in preamble detection Range 0 to 15bits	0	R/W
2	PR_SYNC[2]		0	R/W
1	PR_SYNC[1]		0	R/W
0	PR_SYNC[0]		0	R/W

[Note]
1. This function is not available when Manchester coding is used.

0x45[PACKET_MODE_SET]

Function: Configuration for Packet mode (FIFO in use)
Address: 0x45
Default Value 0x1B

Bit	Symbol	Description	Default Value	R/W
7	FIFO_ADR_EN	FIFO address status (*1) 0: Disable address status 1: Enable address status	0	R/W
6	MRFSKSFD	MR-FSK SFD group (*2) 0: Select SFD1 1: Select SFD2	0	R/W
5	ADDFIL_NG_SET	Operation after NG judgement in address filtering function. 0: Abort data immediately. 1: Abort data when RX completed	0	R/W
4	WHITENING	Whitening control (*7) 0: Whitening disabled 1: Whitening enabled	1	R/W
3	ED_NOTICE	ED value attach in RX mode (*4) 0: ED value is not attached to RX packet 1: ED value is attached to RX packet	1	R/W
2	AUTO_TX	Auto TX function control (*5) 0: Auto TX disabled 1: Auto TX enabled.	0	R/W
1	IEEE_MODE	IEEE 802.15.4 packet mode control (*6) 0: use IEE802.15.4d packet format 1: use IEEE802.15.4g packet format	1	R/W
0	ADDFIL_IDLE_DET	IDLE detection after NG judgement in address filtering function. (*3) 0: After data abort, issue interrupt without IDLE detection 1: After data abort, issue interrupt IDLE detected.	1	R/W

[Detail description]

*1 Address status is shown in [RD_FIFO_LAST] register (B0, 0x7c)

*2 See “SFD detection function”.

*3 See “Address filtering function”.

*4 Attach ED value to received packet

*5 Automatic TX operation without setting [RF_STATUS] register (B0, 0x6c) bit[3:0] (SET_TRX) to 0b1001(TX_ON). TX operation will be started automatically in following cases.
1/ Writing transmission data completed amount given by Length field.
2/ Amount of written transmission data is reached to [FAST_TX_SET] register trigger setting.
(Amount of transmission data include Length field)
To switch the RF state to RX_ON or TRX_OFF immediately after the transmission, the following two method can be used.
①Issue the RX_ON or TRX_OFF instruction and set 0 for this bit (AUTO_TX_EN) during the transmission.
②Set 1 for this bit (AUTO_TX_EN) and 1 for TX_DONE_RX ([ACK_TIMER_EN] register (B0 0x52) bit5) or TX_DONE_OFF ([ACK_TIMER_EN] register (B0 0x52) bit4). For TX_DONE_RX/TX_DONE_OFF, see [ACK_TIMER_EN] register (B0 0x52).

*6 Valid only packet mode (FIFO mode) is selected. Packet mode is selected by register [PLL_MON/DIO_SEL] (B0, x69)

*7 Data Whitening will be applied following case.
1/ In IEEE802.15.4d mode (bit1=0), Whitening function is activated by this register.
2/ In IEEE802.15.4g mode (bit1=1), Whitening function is activated by this register and Whitening bit in PHR data is 1.
If FEC and this bit are enabled concurrently, the data whitening is performed only at data reception regardless of the whitening bit in PHR data

[Note]

1. When you want to write access to the register after enabling bit2 (AUTO_TX), wait for 150us or longer after the FIFO write operation is completed.

0x46[FEC/CRC_SET]

Function: FEC and CRC configuration in TX packet.
Address: 0x46
Default Value 0x03

Bit	Symbol	Description	Default Value	R/W
7	INTLV_EN	Interleave control (*1) 0: Ineterleave disabled 1: Interleave enabled	0	R/W
6	FEC_EN	FEC control 0: FEC disabled 1: FEC enabled	0	R/W
5	FEC_SCHEME	FEC scheme 0: NRNSC 1: RSC	0	R/W
4	CRC_INIT	CRC initial state 0: All “0” 1: All “1”	0	R/W
3	CRC_EN	CRC scheme information source (*3) 0: Use information from FCS Length Field 1: Use information from CRC_MODE[1:0] register	0	R/W
2-1	CRC_MODE[1:0]	CRC scheme (*2) 00: 8bitCRC 01: 16bitCRC (Default Value) 10: 32bitCRC 11: 16bitCRC (CRC-IBM)	01	R/W
0	CRC_DONE	CRC control (1: Perform CRC computation)	1	R/W

[Detail description]

1. If [PACKET_MODE_SET] register (B0, 0x45) bit1(IEEE_MODE)=0b1, IEEE802.15.4g mode is selected.
   CRC computation will use CRC scheme defined by bit[2:1](CRC_MODE) register in TX mode.
   In RX mode, it can be selected by bit3(CRC_EN) register, if it is 0b0, CRC scheme information provided by FCS Length information in Frame Control Field will be used. If it is CRC_EN=0b1, CRC scheme defined by bit[2:1](CRC_MODE) will be used.
2. If [PACKET_MODE_SET] register (B0, x45) bit1(IEEE_MODE)=0b0, IEEE802.15.4d mode is selected, CRC scheme defined by bit[2:1](CRC_MODE) will be used.

Polynomials for each CRC scheme are shown.

CRC8 $= X^8 + X^2 + X^1 + 1$
CRC16 $= X^{16} + X^{12} + X^5 + 1$
CRC16-IBM $= X^{16} + X^{12} + X^2 + 1$
CRC32 $= X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

The following table shows the CRC settings.

IEEE802.15.4 Mode Setting (PACKET_MODE_SET Bit1)	CRC_SET [0]	CRC_SET [3]	CRC_SET [2:1]	Description of CRC Operation
0 (4g Mode)	1	0	00/01/10/11	The CRC calculation is performed using CRC setting information for PHR. CRC setting information for PHR = 0...CRC32 CRC setting information for PHR = 1...CRC16
		1	00/01/10/11	The CRC calculation is performed according to CRC_SET[2:1].
	0	0/1	00/01/10/11	The CRC calculation is not performed, and CRC is not added to packets.
1 (4d Mode)	1	0/1	00/01/10/11	The CRC calculation is performed according to CRC_SET[2:1].
	0	0/1	00/01/10/11	The CRC calculation is not performed, and CRC is not added to packets.

[Note]

*1 This bit is enabled only when bit6(FEC_EN) is 0b1 and enabled.

*2 When [AUTO_ACK_SET] register (B0 0x55) bit4 (AUTO_ACK_EN) is set 0b1, and the AutoAck function is enabled, please set 1b1 for this register bit3 (CRC_EN) and bit0(CRC_DONE) and set the CRC length with bit2-1(CRC_MODE[1:0]) before transmitting the Ack packet.

*3 If **CRC_EN is 0 and the CRC calculation is performed using the CRC setting information for the packet**, the CRC setting for transmission/reception is enabled only in the cases below. If CRC_EN is 1, ignore the following description

Transmit:

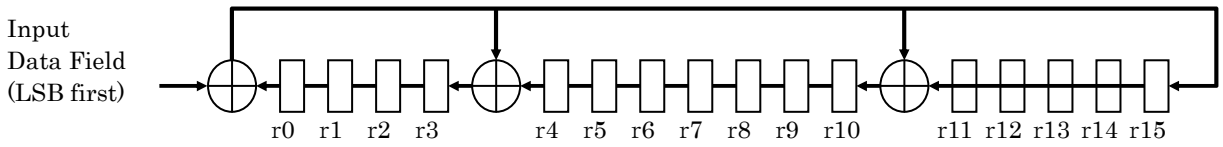
The CRC setting for transmitted data is enabled only when SET_TRX ([RF_STATUS] register (B0 0x6c) bit3-0) is other than 0x6. Therefore, in receiving state, ①write the transmitted data to FIFO after issuing TRX_OFF/Force_TRX_OFF, or ②write the transmitted data to FIFO after issuing TX_ON. If the data is transmitted automatically before a Length of data is written to FIFO using the FAST_TX_TRG ([FAST_TX_SET] register (B0 0x6a)), this operation is not necessary.

Receive:

The CRC setting for received data is enabled only when SET_TRX ([RF_STATUS] register (B0 0x6c) bit3-0) is 0x6. Therefore, read all received data from FIFO in receiving state (before issuing the TRX_OFF/Force_TRX_OFF instruction). When you want to read the received data after issuing the TRX_OFF/Force_TRX_OFF instruction, configure the CRC setting with CRC_EN = 1 and CRC_MODE[1:0] to read it.

*4 When 32-bit CRC is set, the minimum Length is 4 bytes. If FCS (CRC) is set 32-bit for IEEE802.15.4g packet transmission/reception, the Ack packet cannot be received. For the Ack packet, set 16-bit for FCS (CRC) or disable the CRC check.

Example: CRC16 scheme



In TX mode, CRC scheme will be selected by CRC_MODE[1:0] register. It computes Length and PSDU area automatically, 1st byte in FIFO will be updated.

In RX mode, CRC scheme have two choices as described, CRC computation will be applied to Length and PSDU field, then check CRC computation results with attached CRC data. The result will be stored in [PD_DATA_IND] register (B0, 0x29) bit4 (CRC_RSLT1) and bit0 (CRC_RSLT0).

0x47[DATA_SET]

Function: Configuration of TX and RX data
Address: 0x47
Default Value 0x11

Bit	Symbol	Description	Default Value	R/W
7	NBO_SEL	Bandwidth control (*1) 0: Normal bandwidth mode 1: Narrow bandwidth mode (optional function)	0	R/W
6	TX_POL	TX data polarity 0: “1” = +ÄF 1: “1” = -ÄF	0	R/W
5	RX_POL	RX data polarity 0: “1” = +ÄF 1: “1” = -ÄF	0	R/W
4	GFSK_EN	Gaussian Filter control 0: disabled (FSK) 1: enabled (GFSK)	1	R/W
3	FORMAT	Coding scheme 0: NRZ code 1: Manchester code (*2)	0	R/W
2-0	RATE[2:0]	Data rate control 000: 50 kbps 001: 100 kbps (Default Value) 010: 200 kbps 011: 400 kbps Others: Reserved	001	R/W

[Note]

*1. In IEEE802.15.4g standard, channel spacing is defined as 400 kHz in case of data transmission rate is100kbps. So called “Narrow bandwidth mode” is apply 200kHz of channel spacing in case of 100kbps data transmission rate. In order to use “Narrow bandwidth mode”, following registers have to be configured.
- [IF_FREQ_AFC_H] and [IF_FREQ_AFC_L] register (B0, x30 and x31)
- [IF_FREQ_H] and [IF_FREQ_L] register (B1 x0a, 0b)
- [IF_FREQ_CCA_H] and [IF_FRE_CCA_L] register (B1, x0c and 0d)
- [BPF_AFC_ADJ_H] and [BPF_AFC_ADJ_L] register (B0, x32 and 33)
- [BPF_ADJ_H] and [BPF_AFC_ADJ_L] register (B1, x0e and 0f)
- [BPF_CCA_ADJ_H] and [BPF_CCA_ADJ_L] register (B1, x10 and 11)
- [RSSI_LPF_ADJ] register (B1, x12)

Channel occupied bandwidth in each data transmission rate is shown in table below.

NBO_SEL	50 kbps	100 kbps	150 kbps	200 kbps	400 kbps
“0”	200 kHz	400 kHz (Default Value)	400 kHz (Initial value)	600 kHz	800 kHz
“1”	200 kHz	200 kHz	-	400 kHz	600 kHz

Set the following registers for 150kbps.

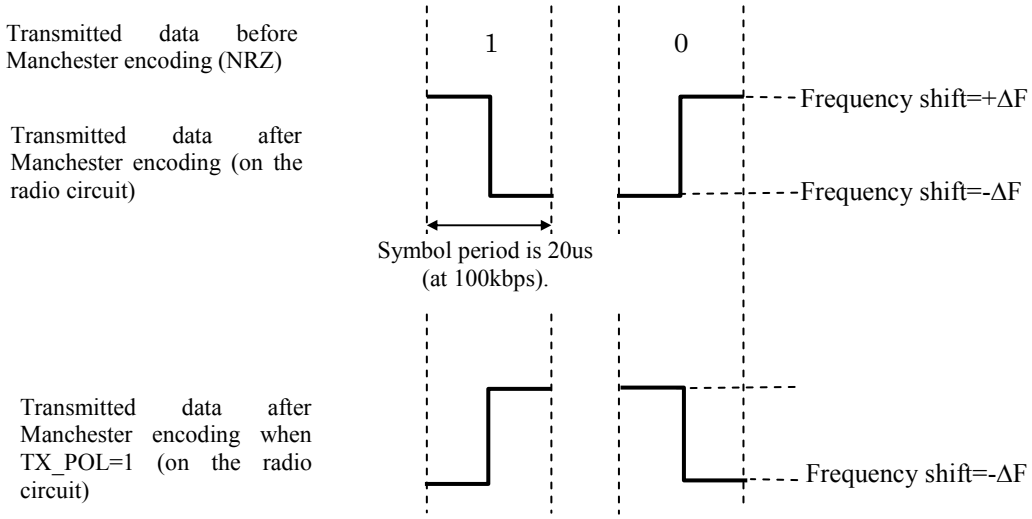
Register	Setting value
RATE_SET1(B0 0x04)	0x02
RATE_SET2(B0 0x05)	0x03
DATA_SET(B0 0x47 bit2-0 RMODE)	0x2

For 10kbps/20kbps/40kbps, see "Initial setting register."

*2. Manchester encoding is performed for the data after the preamble (SFD/Length/user data/CRC area). For details, see section "Packet Format." For details on the Manchester encoding, see "About Manchester encoding" described later. The Manchester code is not applied to the ACK packet during AutoAck. The FEC function does not support the Manchester code.

About Manchester encoding

Here is the correspondence between the transmitted data and the Manchester encoded data transmitted on the radio circuit when MFMT is 1 (Manchester format setting is ON). The transmission rate on the radio circuit is half of the specified transmission rate (RATE) when FORMAT is 1. For 100kbps (RATE = 001), the transmission rate on the radio circuit is 50kbps. When you want to identify the polarity of the Manchester encoded data, set TX_POL (bit 6) to 1 for the sender or RX_POL (bit 5) to 1 for the receiver to invert the polarity.



0x48[CH0_FL]

Function: Frequency parameter for ch0 (lower 8bits)
Address: 0x48
Default Value 0x44
923.100MHz (Xtal frequency: 36MHz)

Bit	Symbol	Description	Default Value	R/W
7-0	CH0_F[7:0]	Frequency parameter for Channel 0 (bit7 to bit0)	0100_0100	R/W

[Detail description]

1. See section “Programming Channel#0 Frequency parameter”

0x49[CH0_FM]

Function: Frequency parameter for ch0 (middle 8bits)
Address: 0x49
Default Value 0x44
923.100MHz (Xtal frequency: 36MHz)

Bit	Symbol	Description	Default Value	R/W
7-0	CH0_F[15:8]	Frequency parameter for Channel 0 (bit15 to bit8)	0100_0100	R/W

[Detail description]

1. See section “Programming Channel#0 Frequency parameter”

0x4A[CH0_FH]

Function: : Frequency parameter for ch0 (upper 4bits)
Address: : 0x4a
Default Value : 0x0A
923.100MHz (Xtal frequency: 36MHz)

Bit	Symbol	Description	Default Value	R/W
7-4	Reserved	Reserved	0000	R/W
3-0	CH0_F[19:16]	Frequency parameter for Channel 0 (bit19 to bit16)	1010	R/W

[Detail description]
1. See section “Programming Channel#0 Frequency parameter”

0x4B[CH0_NA]

Function: N counter and A counter avlue for ch0
Address: 0x4b
Default Value 0x61
923.100MHz (Xtal frequency: 36MHz)

Bit	Symbol	Description	Default Value	R/W
7-4	CH0_N[3:0]	N-counter	0110	R/W
3-2	Reserved	Reserved	00	R/W
1-0	Ch0_A[1:0]	A-counter	01	R/W

[Detail description]
1. See section “Programming Channel#0 Frequency parameter”

0x4C[CH_SPACE_L]

Function: Frequency spacing setting to next channel (lower 8bits)
Address: 0x4c
Default Value 0x82 (Channel spacing = 400kHz)

Bit	Symbol	Description	Default Value	R/W
7-0	CH_SP_F[7:0]	Channel spacing parameter (bit7 to bit0)	1000_0010	R/W

[Detail description]
1. See section “Programming Channel spacing”

0x4D[CH_SPACE_H]

Function: Frequency spacing setting to next channel (upper 8bits)
Address: 0x4d
Default Value 0x2D (Channel spacing = 400kHz)

Bit	Symbol	Description	Default Value	R/W
7-0	CH_SP_F[15:8]	Channel spacing parameter (bit15 to bit8)	0010_1101	R/W

[Detail description]
1. See section “Programming Channel spacing”

0x4E[F_DEV_L]

Function: Frequency deviation setting for GFSK modulation (lower 8bits)
Address: 0x4e
Default Value 0xB0 (Fdev=50 kHz)

Bit	Symbol	Description	Default Value	R/W
7-0	F_DEV[7:0]	Frequency deviation in TX mode (lower 8bits)	1011_0000	R/W

[Detail description]
1. See section “Programming Frequency deviation”

[Note]
1. Frequency deviation of FSK modulation is decided by register values of [FSK_FDEV1] to [FSK_FDEV4].

0x4F[F_DEV_H]

Function: Frequency deviation setting for GFSK modulation (upper 8bits)
Address: 0x4f
Default Value 0x05 (Fdev=50 kHz)

Bit	Symbol	Description	Default Value	R/W
7-0	F_DEV[15:8]	Frequency deviation in TX mode (upper 8bits)	0000_0101	R/W

[Detail description]
1. See section “Programming Frequency deviation”

[Note]
1. Frequency deviation in FSK modulation will be configured by [FSK_FDEV1] to [FSK_FDEV4] register.
2. For 400kbps, 100kbps ([DATA_SET] register (B0 0x47) bit7 NBO_SEL=1), and 200kbps (NBO_SEL=1), set the modulation index to 0.6 or less.

0x50[ACK_TIMER_L]

Function: Ack timer setting for Auto_Ack operation (lower 8bits)
Address: 0x50
Default Value 0x08

Bit	Symbol	Description	Default Value	R/W
7-0	ACK_TIMER[7:0]	Ack timer setting (lower 8bits)	0000_1000	R/W

0x51[ACK_TIMER_H]

Function: Ack timer setting for Auto_Ack operation (upper 8bits)
Address: 0x51
Default Value 0x07

Bit	Symbol	Description	Default Value	R/W
7-0	ACK_TIMER[15:8]	Ack timer setting (upper 8bits)	0000_0111	R/W

[Detail description]

1. See section “AUTO_ACK function”.
2. [ACK_TIMER_L/H] registers are valid if [ACK_TIMER_EN] register bit0 (ACK_TIMER_EN)=0b1.
3. Timer clock will be different depending on data transmission rate.

Data transmission rate	Timer clock
10kbps	0.18 MHz
20kbps	0.36 MHz
40kbps	0.72 MHz
50kbps	0.9 MHz
100kbps	1.8 MHz
150kbps	2.7 MHz
200kbps	3.6 MHz
400kbps	7.2 MHz

Example: If ACK_TIMER[15:0]= 0x708 (Default, d1800) in case of 100kbps.
Timer duration : 1800 / 1.8MHz = 1msec

0x52[ACK_TIMER_EN]

Function: Ack timrer configuration
Address: 0x52
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5	TX_DONE_RX	RX setting after the transmit completion enable 0:Disable 1: Enable When this bit is set 1, the state automatically transitions to RX_ON after the transmit completion.	0	R/W
4	TX_DONE_OFF	TRX_OFF setting after the transmit completion enable 0:Disable 1: Enable When this bit is set 1, the state automatically transitions to TRX_OFF after the transmit completion.	0	R/W
3-1	Reserved	Reserved	000	R/W
0	ACK_TIMER_EN	Ack timer control 0: Ack timer disabled 1: Ack timer enabled	0	R/W

[Detail description]

1. See section “AUTO_ACK function”.
2. ACK packet will be transmitted automatically after Ack timer expired, if [AUTO_ACK_SET] register (B0, x55) bit4 (AUTO_ACK_EN)=0b1, and ACK_TIMER_EN is valid.

[Note]

1. Both bit5 (TX_DONE_RX) and bit4 (TX_DONE_OFF) are set to 0b1, the bit5 setting takes priority.
2. The following table shows the operation and priority for a combination of bit5 (RX setting enable after the transmit completion), bit4 (TRX_OFF setting enable after the transmit completion), and RF state setting command ([RF_STATUS] register (B0 0x6c) bit3-0 SET_TRX) issued during the transmission. The RF state setting command (RF_STATUS) is valid after the transmit completion interrupt takes place and an RF state transition is completed by bit5 or bit4.

   Priority : Force_TRX_OFF > TRX_DONE_RX > TX_DONE_OFF > (TRX_OFF/TX_ON/RX_ON)

TX_DONE_RX	TX_DONE_OFF	SET_TRX (RF_STATUS)	Operation after the transmit completion
0	1	Force_TRX_OFF	TRX_OFF immediately after Force_TRX_OFF command is issued.
		TRX_OFF	TRX_OFF.
		TX_ON	TRX_OFF.
		RX_ON	TRX_OFF.
1	0	Force_TRX_OFF	TRX_OFF immediately after Force_TRX_OFF command is issued.
		TRX_OFF	RX_ON.
		TX_ON	RX_ON.
		RX_ON	RX_ON.
1	1	Force_TRX_OFF	TRX_OFF immediately after Force_TRX_OFF command is issued.
		TRX_OFF	RX_ON.
		TX_ON	RX_ON.
		RX_ON	RX_ON.

3. When bit5 (TX_DONE_RX) is enabled, wait until the RF state setting (RF_STATUS) becomes 0x66 after the transmit completion before write accessing to the register.
4. When bit4 (TX_DONE_OFF) is enabled, wait until the RF state setting (RF_STATUS) becomes 0x88 after the transmit completion before write accessing to the register.

0x53[ACK_FRAME1]

Function: Frame Control Field (2bytes) setting in Ack packet (lower byte)
Address: 0x53
Default Value 0x02

Bit	Symbol	Description	Default Value	R/W
7-0	ACK_FRAME[7:0]	Frame Control Field (lower byte)	0000_0010	R/W

0x54[ACK_FRAME2]

Function: :Frame Control Field (2bytes) setting in Ack packet (upper byte)
Address: :0x54
Default Value :0x00

Bit	Symbol	Description	Default Value	R/W
7-0	ACK_FRAME[15:8]	Frame Control Field 設定 (upper byte)	0000_0000	R/W

[Detail description]
1. See section “AUTO_ACK function”.
2. Please refer to IEEE 802.15.4i for detail of Ack packet.
3. LSB first

The following table shows the correspondence between the ACK frame (FrameControl) and the register.

Register	Bit	Ack frame
ACK_FRAME2	7-6	Source Addressing Mode
	5-4	Frame Version
	3-2	Dest Addressing Mode
	1-0	Reserved
ACK_FRAME1	7	Reserved
	6	PAN ID Compression
	5	Ack Request
	4	Frame Pending
	3	Security Enabled
	2-0	Frame Type

※In the Ack transmit frame, this register setting value is applied to the FrameControl field (2byte), the obtained data is applied to the SequenceNumber field (1byte), and FCS(2byte) is calculated automatically.

0x55[AUTO_ACK_SET]

Function: Configuration of Auto_Ack function
Address: 0x55
Default Value :0x00

Bit	Symbol	Description	Default Value	R/W
7	RX_ACK_CANCEL	ACK packet abort (*4) 0: Do not abort received ACK packet 1: Abort received ACK packet	0	R/W
6	AUTO_RX_EN	ACK automatic reception control (*1) 0: Automatic reception disabled 1: Automatic reception enabled	0	R/W
5	Reserved	Reserved	0	R/W
4	AUTO_ACK_EN	ACK Function control (*2) 0: Auto_Ack disabled 1: Auto_Ack enabled	0	R/W
3-2	Reserved	Reserved	00	R/W
1	ACK_SEND	Perform ACK packet transmission (1: transmit) (*3)	0	R/W
0	ACK_STOP	Ack packet abort/receive stop (1: stop) (*3)	0	R/W

[Detail description]

1. See section “AUTO_ACK function”.

*1 The function that enable RX_ON immediately after transmitting Ack request packet to check Ack status.
*2 The function that execute TX_ON for Ack packet transmission preparation.
*3 ACK_SEND or ACK_STOP perform following operations shown below.
If ACK_SEND=0b1
Transmit ACK packet.
If ACK_STOP=0b1
TX mode: Prepared ACK packet will not be transmitted, packet destroyed and RF_STATUS maintained.
RX mode: Stop receiving operation. RF_STATUS move to TRX_OFF.
*4 This bit will valid if one of bit in [ADDFIL_CNTRL] register (B2, 0x60) bit[4:0] is 0b1, Address Filtering Function is enabled. In case of Bit6 (AUTO_RX_EN)=0b1, it received ACK packet which is just after ACK request packet is transmitted.

[Note]

1. Either bit1(ACK_SEND) or bit0 (ACK_STOP) should be 0b1. ACK_STOP has higher priority if both bits are 0b1.
2. When bit6 (AUTO_RX_EN) is enabled, wait until the RF state setting (RF_STATUS) becomes 0x66 after the transmit completion before write accessing to the register.
3. When bit4 (AUTO_ACK_EN) is enabled, wait until the RF state setting (RF_STATUS) becomes 0x99 after the receive completion before write accessing to the register.
4. When bit4 (AUTO_ACK_EN) is enabled, [TX_ALARM_LH] register (B0 0x35) bit[7:0] has to be 8’h00 before ACK packet is transmitted

0x59[GFIL00/FSK_FDEV1]

Function: Gaussian filter parametre 0 / 1st set of frequency deviation parameter for FSK modulation
Address: 0x59
Default Value 0x00 (GFSK Modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL001[7:0] FSK_FDEV1[7:0]	Gaussian Filter parameter 0 1st frequency deviation parameter in FSK modulation [register value x 33.4 x 2 (Hz)]	0000_0000	R/W

[Detail description]

1. If [DATA_SET] register (B0, 0x47) bit4 (GFSK_EN)=0b1, GFSK modulation scheme will be used, otherwise FSK modulation scheme will be used.
   See section “Gaussian Filter configuration” in GFSK modulation scheme.
2. In FSK modulation scheme, this register represent amount of frequency offset from centre frequency.
   See section “FSK modulation”.

0x5A[GFIL01/FSK_FDEV2]

Function: Gaussian filter parameter 1 / 2nd set of frequency deviation parameter for FSK modulation
Address: 0x5a
Default Value 0x00 (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL01[7:0] FSK_FDEV2[7:0]	Gaussian Filter parameter 1 2nd frequency deviation parameter in FSK modulation (*2) [registrer value x 33.4 x 2 (Hz)]	0000_0000	R/W

[Detail description]

1. If [DATA_SET] register (B0, 0x47) bit4 (GFSK_EN)=0b1, GFSK modulation scheme will be used, otherwise FSK modulation scheme will be used.
   See section “Gaussian Filter configuration” in GFSK modulation scheme.
2. In FSK modulation scheme, this register represent amount of frequency offset from 1st frequency deviation.
   See section “FSK modulation”.

0x5B[GFIL02/FSK_FDEV3]

Function: Gaussian filter parameter 2 / 3rd set of frequency deviation parameter for FSK modulation
Address: 0x5b
Default Value 0x10 (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL02[7:0] FSK_FDEV3[7:0]	Gaussian Filter parameter 2 3rd frequency deviation parameter in FSK modulation *2 [registrer value x 33.4 x 2 (Hz)]	0001_0000	R/W

[Detail description]

1. If [DATA_SET] register (B0, 0x47) bit4 (GFSK_EN)=0b1, GFSK modulation scheme will be used, otherwise FSK modulation scheme will be used.
   See section “Gaussian Filter configuration” in GFSK modulation scheme.
2. In FSK modulation scheme, this register represent amount of frequency offset from 2nd frequency deviation.
   See section “FSK modulation”.

0x5C[GFIL03/FSK_FDEV4]

Function: Gaussian filter parameter 3 / 4th set of frequency deviation parameter for FSK modulation
Address: 0x5c
Default Value 0x01 (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL03[7:0] F_DEV3[7:0]	Gaussian Filter parameter 3 4th frequency deviation parameter in FSK modulation *2 [registrer value x 33.4 x 2 (Hz)]	0000_0001	R/W

[Detail description]

1. If [DATA_SET] register (B0, 0x47) bit4 (GFSK_EN)=0b1, GFSK modulation scheme will be used, otherwise FSK modulation scheme will be used.
   See section “Gaussian Filter configuration” in GFSK modulation scheme.
2. In FSK modulation scheme, this register represent amount of frequency offset from 3rd frequency deviation.
   See section “FSK modulation”.

0x5D[GFIL04]

Function: : Gaussigan filter parameter 4
Address: 0x5d
Default Value 0x03 (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL04[7:0]	Gaussian Filter parameter 4	0000_0011	R/W

[Detail description]

1. If [DATA_SET] register (B0, 0x47) bit4 (GFSK_EN)=0b1, GFSK modulation scheme will be used, otherwise FSK modulation scheme will be used..
2. See section “Gaussian Filter configuration” in GFSK modulation scheme.

0x5E[GFIL05]

Function: Gaussian filter parameter 5
Address: 0x5e
Default Value 0x05 (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL05[7:0]	Gaussian Filter parameter 5	0000_0101	R/W

[Detail description]

1. If [DATA_SET] register (B0, 0x47) bit4 (GFSK_EN)=0b1, GFSK modulation scheme will be used, otherwise FSK modulation scheme will be used..
2. See section “Gaussian Filter configuration” in GFSK modulation scheme.

0x5F[GFIL06]

Function: Gaussian filter parameter 6
Address: 0x5f
Default Value 0x09 (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL06[7:0]	Gaussian Filter parameter 6	0000_1001	R/W

[Detail description]

1. If [DATA_SET] register (B0, 0x47) bit4 (GFSK_EN)=0b1, GFSK modulation scheme will be used, otherwise FSK modulation scheme will be used..
2. See section “Gaussian Filter configuration” in GFSK modulation scheme.

0x60[GFIL07]

Function: Gaussian filter parameter 7
Address: 0x60
Default Value 0x0F (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL07[7:0]	Gaussian Filter parameter 7	0000_1111	R/W

[Detail description]

1. If [DATA_SET] register (B0, 0x47) bit4 (GFSK_EN)=0b1, GFSK modulation scheme will be used, otherwise FSK modulation scheme will be used..
2. See section “Gaussian Filter configuration” in GFSK modulation scheme.

0x61[GFIL08]

Function: Gaussian filter parameter 8
Address: 0x61
Default Value 0x15 (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL08[7:0]	Gaussian Filter parameter 8	0001_0101	R/W

[Detail description]

1. If [DATA_SET] register (B0, 0x47) bit4 (GFSK_EN)=0b1, GFSK modulation scheme will be used, otherwise FSK modulation scheme will be used..
2. See section “Gaussian Filter configuration” in GFSK modulation scheme.

0x62[GFIL09]

Function: Gaussian filter parameter 9
Address: 0x62
Default Value 0x1A (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL09[7:0]	Gaussian Filter parameter 9	0001_1010	R/W

[Detail description]

1. If [DATA_SET] register (B0, 0x47) bit4 (GFSK_EN)=0b1, GFSK modulation scheme will be used, otherwise FSK modulation scheme will be used..
2. See section “Gaussian Filter configuration” in GFSK modulation scheme.

0x63[GFIL10]

Function: Gaussian filter parameter 10
Address: 0x63
Default Value 0x1F (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL10[7:0]	Gaussian Filter parameter 10	0001_1111	R/W

[Detail description]

1. If [DATA_SET] register (B0, 0x47) bit4 (GFSK_EN)=0b1, GFSK modulation scheme will be used, otherwise FSK modulation scheme will be used..
2. See section “Gaussian Filter configuration” in GFSK modulation scheme.

0x64[GFIL11]

Function: Gaussian filter parameter 11
Address: 0x64
Default Value 0x20 (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL11[7:0]	Gaussian Filter parameter 11	0010_0000	R/W

[Detail description]

1. If [DATA_SET] register (B0, 0x47) bit4 (GFSK_EN)=0b1, GFSK modulation scheme will be used, otherwise FSK modulation scheme will be used.
2. See section “Gaussian Filter configuration” in GFSK modulation scheme.

0x65[FSK_TIME1]

Function: Timing parameter for Frequency deviation in FSK modulation (FDEV3)
Address: 0x65
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	FDEV_TIME1[7:0]	Timing parameter for Frequency deviation in FSK modulation (FDEV3) [register value x clk (4MHz)]	0000_0000	R/W

[Detail description]

1. Frequency deviation defined by [FSK_FDEV3] register (B0, 0x5b) will be mainted for time duration defined in this register.
2. See section “FSK modulation”.

0x66[FSK_TIME2]

Function: Timing parameter for Frequency deviation in FSK modulation (FDEV2)
Address: 0x66
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	FDEV_TIME2[7:0]	Timing parameter for Frequency deviation in FSK modulation (FDEV2) [register value x clk (4MHz)]	0000_0000	R/W

[Detail description]

1. Frequency deviation defined by [FSK_FDEV2] register (B0, 0x5a) will be mainted for time duration defined in this register.
2. See section “FSK modulation”.

0x67[FSK_TIME3]

Function: Timing parameter for Frequency deviation in FSK modulation (FDEV1)
Address: 0x67
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	FDEV_TIME3[7:0]	Timing parameter for Frequency deviation in FSK modulation (FDEV1) [register value x clk (4MHz)]	0000_0000	R/W

[Detail description]

1. Frequency deviation defined by [FSK_FDEV2] register (B0, 0x59) will be mainted for time duration defined in this register.
2. See section “FSK modulation”.

0x68[FSK_TIME4]

Function: Timing parameter for Frequency deviation in FSK modulation (FDEV0)
Address: 0x68
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	FDEV_TIME4[7:0]	Timing parameter for unmodulated (carrier frequency) time period [register value x clk (4MHz)]	0000_0000	R/W

[Detail description]

1. Define time period for unmodulatied signal transmission
2. See section “FSK modulation”.

0x69[PLL_MON/DIO_SEL]

Function: Output configutation of PLL lock detection and DIO mode configuration
Address: 0x69
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7	Reserved	Reserved	000	R/W
6	INT_TIM_CTRL	Interrupt notification timing switch 0: The interrupt is notified at the same timing as ML7396. 1: The interrupt is notified at the same timing as defined in ML7396B.	0	R/W
5	Reserved	Reserved	0	R/W
4	PLL_LD	Output configuration of PLL lock status signal from DMON pin. (*1) 0: Output disabled 1: Output enabled	0	R/W
3-2	Reserved	Reserved	00	R/W
1	DIO_EN	DIO mode setting (*2) 0: Use in packet mode (FIFO mode) 1: Use in DIO mode	0	R/W
0	RX_FIFO_MON	RX data bit monitoring (*3) 0: Output disabled 1: Output enabled	0	R/W

[Detail description]

*1 In case of output PLL lock signal from DMON pin (#17 pin), it has to be [CLK_SET] register (B0, x02) bit4 (CLKOUT_EN)=0b0.

*2 DIO is operating mode that will use DIO interface (DCLK and DIO) to have data interface with HOST MCUwithout TX/RX FIFO. DIO input and output is combined with [PREAMBLE_SET] and [SFD1_SETx] registers. Data input and output will be synchronized to DCLK pin.
Dummy write to FIFO is required in order to output DCLK at transmission. For details, refer to "Flow chart at transmission (When DIO used)."
When this bit is disabled, FIFO operation is performed. Only in this case, IEEE mode setting ([PACKET_MODE_SET] register (B0 0x45) bit1) is enabled.

*3 If you want to output demodulated received data from DIO interface independent from configured preamble or SFD, enable this bit. If you enable this bit when DIO_EN = Ob1, it is output from the data section of packet after SFD detection.
During BER measurement, set DIO_EN = 0b0 and RX_FIFO_MON = 0b1.

*4 For details on the interrupt timing, see "Address filtering function."

0x6A[FAST_TX_SET]

Function: : Trigger timing for start of transmission in FAST_TX mode
Address: : 0x6a
Default Value : 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	FAST_TX_TRG[7:0]	TX start trigger in FAST_TX mode [7]=0b1: 128byte [6]=0b1: 64byte [5]=0b1: 32byte [4]=0b1: 16byte [3]=0b1: 8byte [2]=0b1: 4byte [1]=0b1: 2byte [0]=0b1: 1byte 0x00: No FAST_TX mode	0000_0000	R/W

[Detail description]

1. FAST_TX mode is operating mode that will start transmission before FIFO is filled by amount of data given by Lnegth field. It will start transmission if FIFO is filled by amount of data given by register.
2. This function will be available if [PACKET_MODE_SET] register (B0, 0x45) bit2 (AUTO_TX)=0b1. Otherwise, [RF_STATUS] register (B0, 0x6c) bit[3] (SET_TRX)=0b1001 (TX_ON) to start transmission.

[Note]

1. If amount of transmission data is greater than 256 bytes, [PACKET_MODE_SET] register bit2 (AUTO_TX) has to be 0b1, it enables AUTO_TX mode(or set TX_ON in advance), and this register has to be value other than 0x00.
2. Writing to FIFO has to be faster than data transmission speed in order to avoid FIFO empty.
3. Amount of data to write include Length field.
4. When multiple bits are set for this register, the most significant bit is used.

0x6B[CH_SET]

Function: TX/RX channel setting
Address: 0x6b
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-4	Reserved	Reserved	0000	R/W
3-0	RF_CH[3:0]	TX/RX channel setting It can be selected from 0 to 15CH	0000	R/W

[Note]

1. Those channels enabled by register [CH_EN_L] and [CH_EN_H] have to be selected.

0x6C[RF_STATUS]

Function: RF status register
Address: 0x6c
Default Value 0x88

Bit	Symbol	Description	Default Value	R/W
7-4	GET_TRX[3:0]	Operating status of RF block 0110: RX_ON (receiving) 1000: TRX_OFF (RF block is OFF) 1001: TX_ON (transmitting) Others: Reserved	1000	R
3-0	SET_TRX[3:0]	Configure RF block status 0011: Force_TRX_OFF (Force RF block OFF) 0110: RX_ON (Enable RX) (*1) 1000: TRX_OFF (Disable RF block) (*2) 1001: TX_ON (Enable TX) (*3) Others: Forbidden, nothing responded.	1000	R/W

[Detail description]

*1 You can set the reception during transmitting a packet. In this case, the state transitions to RX_ON after the transmit completion.

*2 If TRX_OFF executed, RF block will be OFF after TX or RX completed.
Force_TRX_OFF will stop TX or RX immediately and disable RF block.

*3 You can set the transmission during receiving a packet. In this case, the state transitions to TX_ON after the receive completion.
When using the auto-transmit setting, see also the description of AUTO_TX ([PACKET_MODE_SET] register (B0 0x45) bit2).

[Note]

1. If SFD is detected during TRX_OFF state transition, RX_ON is retained automatically.

0x6D[2DIV_ED_AVG]

Function: The number of averaging process in ED computation for 2 diversity mode.
Address: 0x6d
Default Value 0x01

Bit	Symbol	Description	Default Value	R/W
7-3	Reserved	Reserved	0000_0	R/W
2-0	2DIV_ED_AVG[2:0]	Number of values to be averaged for calculating the ED value in 2 diversity mode (*1)	001	R/W

[Detail description]

*1 Number of averaging sample is shown in table below

2DIV_ED_AVG[2:0]	Averaging samples
0b000	1
0b001 (Default Value)	2
0b010	4
0b011	8
0b100	15
0b101	16
others	8

0x6E[2DIV_GAIN_CNTRL]

Function: Gain control mode setting
Address: 0x6e
Default Value 0x02

Bit	Symbol	Description	Default Value	R/W
7-2	TIM_TX_OFF2	Lamp down timing adjustment when transitioning to RX_ON following TX_ON (*2) (Setting value + 1) x 2.22usec	0000_00	R/W
1-0	2DIV_GAIN[1:0]	Gain control mode setting (*1) 00: Fix H gain mode 01: Enable H <-> M gain transition 10: Enable H <-> M <-> L gain transition 11: Fix H gain mode	10	R/W

[Detail description]

*1 Threshold level for each gain mode are defined by register [GAIN_MtoL], [GAIN_LtoM], [GAIN_HtoM] and [GAIN_MtoH] register (B0, 0x1c to 0x1f).
For this register, set a value specified in "Initial setting registers" and do not change it for adjustment.

*2 It is enabled when [RAMP_CNTRL] register (B2 0x2C) bit4 (TXOFF_RAMP_EN) is set 0b1.
For details, see "Lamp control function"

0x6F[2DIV_SEARCH]

Function: Timing parameter in 2 diversity mode.
Address: 0x6f
Default Value 0x20

Bit	Symbol	Description	Default Value	R/W
7	SEARCH_MODE	Serach mode setting in 2 diversity mode. (*1) 0: Normal serach 1: FAST search	0	R/W
6-0	SEARCH_TIME[6:0]	Time parameter for 2 diversity serach (*2) Search for preamble duration of [(register value+1) x 1bit]	010_0000	R/W

[Detail description]

*1 In normal serach, ED value detecion will be performed for 2 antennas and select one of an antenna which has better ED value.
In FAST search mode, if first antenna has larger ED value than [2DIV_FAST_LV] register, antenna searching will be terminated.

*2 As default it will be 0x20 (=0d32) which is corresponding to 330usec in 100kbp. This setting value needs to be changed according to the data rate setting when the diversity is used. For details on the setting value supported for the data rate, refer to "Initial setting registers."

[Note]

*1 SEARCH_TIME[6:0] has to be greater than 0x18(22 bit). Preamble length in TX side has minimum 12bits (In 100kbps mode for both). See secion “Antenna diversity function”.

0x70[2DIV_FAST_LV]

Function: Threshold value setting in 2 diversity mode.
Address: 0x70
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	2DIV_FAST_LV[7:0]	Threshold level in FSST seacrch mode. (0 to 255)	0000_0000	R/W

[Detail description]

1. This register will be valid if [2DIV_SERCH] register bit7 (SEARCH_MODE)=0b1.
2. Detected ED value is greater than value in this register, opposite blanch of antenna is not measured.

0x71[2DIV_CNTRL]

Function: Miscellaneous function in 2 diversity mode.
Address: 0x71
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5	ANT_CNTRL	ANT control bit1	0	R/W
4	ANT_CTRL0	ANT control bit0	0	R/W
3	INV_ANT_SW	ANT_SW polarity 0: positive logic 1: negative logic	0	R/W
2	INV_TRX_SW	TRX_SW polarity 0: positive logic 1: negative logic	0	R/W
1	2PORT_SW	ANT_SW configuration 0: use SPDT SW 1: use DPDT DW	0	R/W
0	2DIV_EN	2 diversity control 0: diversity disabled 1: diversity enabled	0	R/W

[Detail description]

1. See secion “Antenna diversity function”.

The following table shows the output control for TRX_SW and ANT_SW.

INV_TRX_SW	2PORT_SW	TX/RX 0:Receive 1:Transmit	When TX_ANT_EN = 0 * 1		When TX_ANT_EN = 1 * 1	
			TRX_SW pin	ANT_SW pin	TRX_SW pin	ANT_SW pin
0	0 (SPDT)	0 (during CCA)	0	2DIV_RSLT ※3	0	TX_ANT ※2
		0 (not during CCA)				2DiverRSLT ※3
		1	1		1	
	1 (DPDT)	0 (during CCA)	ANT_SW inverted	2DIV_RSLT ※3	ANT_SW inverted	TX_ANT ※2
		0 (not during CCA)				2DIV_RSLT ※3
		1		2DIV_RSLT inverted		2DIV_RSLT inverted
1	0 (SPDT)	0 (during CCA)	1	2DIV_RSLT ※3	1	TX_ANT ※2
		0 (not during CCA)				2DIV_RSLT ※3
		1	0		0	
	1 (DPDT)	0 (during CCA)	ANT_SW inverted	2DIV_RSLT inverted	ANT_SW inverted	TX_ANT ※2
		0 (not during CCA)				2DIV_RSLT inverted
		1		2DIV_RSLT ※3		2DIV_RSLT ※3

* 1: See [2DIV_RSLT] register (B0 0x72) bit5.
* 2: See [2DIV_RSLT] register (B0 0x72) bit4.
* 3: See [2DIV_RSLT] register (B0 0x72) bit1-0.

The antenna specified by diversity is cleared when one of the following condition is satisfied.
①Receive completion interrupt (both of INT[18] and INT[19]) is cleared after the packet reception
②Diversity completion interrupt is cleared
③Diversity is completed, but it is considered as error, and diversity search is restarted
Therefore, when the diversity search is enabled, clear the receive completion interrupt and the diversity search completion interrupt after the packet reception is completed. If you want to read the diversity search result, it must be done before you clear the receive completion interrupt and the diversity detection completion interrupt. If you disable the diversity search (2DIV_EN = 0) before clearing the receive completion interrupt, the antenna by the diversity search is retained. Issuing the TRX_OFF instruction restores the default antenna (antenna setting when the diversity search is disabled).

The ANT_SW, TRX_SW, and DCNT pin functions are switched by the bit 5-3 settings as shown below.

ANT_CTRL[0]	DCNT pin
0	External PA control signal (default function)
1	ANT control signal (ant_sw internal signal)

ANT_CTRL[1]	TRX_SW pin	ANT_SW pin
0	Default function (see the above table)	Default function (see the above table)
1	ANT control signal (exclusive OR of internal signals trx_sw and ant_sw)	ANT control signal (ant_sw internal signal)

For details, see "Antenna switch control."

[Note]
If you enable this bit and set RX_ON, wait until the SFD detection interrupt ([INT_SOURCE_GRP2] register bit3 (INT[11])) occurs before write accessing to the register.

0x72[2DIV_RSLT]

Function: Status register for 2 divresity mode
Address: 0x72
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7	2DIV_DONE	Completion flag for 2 diversity search 0: Busy (Not started yet) 1: Completed	0	R
6	Reserved	Reserved	0	R/W
5	TX_ANT_EN	CCA/transmission antenna setting enable (*1) 0:Disable 1: Enable	0	R/W
4	TX_ANT	CCA/transmission antenna setting (*1) 0:Antenna1 1: Antenna2	0	R/W
3-2	Reserved	Reserved	00	R/W
1	2DIV_RSLT2	Antenna2 selected (*2) 1: selected	0	R/W
0	2DIV_RSLT1	Anternna1 selected (*2) 1: selected	0	R/W

[Note]

*1 When TX_ANT_EN is set to 0b1, the antenna is fixed with this bit for TX_ON or when running CCA. This antenna fix function is valid only for TX_ON or when CCA runs by CCA_EN (CCA_CNTRL) and invalid for AutoAck or when CCA runs automatically after the address filtering. It is also invalid for TX_ON set by the AutoAck function. It becomes valid when Ackstop (AUTO_ACK_EN) is issued.It can be cleared by writing 0b1 to this register bit.

*2 See secion “Antenna diversity function”.

About 2DIV_RSLT[2-1]

This displays the antenna status (Read only) or specifies the antenna (Write only) during diversity search. When any value is written to this bit, the ANT_SW pin is set to the specified antenna (Forced setting). For details on the forced setting, see "About forced ANT_SW and TRX_SW pin setting." Note that if the antenna is specified forcibly by this register, its setting value cannot be read.
The following table "Antenna display for each operation status" shows the antenna status when it is not set forcibly.

Antenna display for each operation status

2DIV_EN (B0 0x71)	TX_ANT_EN	Operation status	Display content
0	0	Reception (not during CCA)	Receiving antenna (Default: 01)
		Reception (during CCA)	Receiving antenna (Default: 01)
		Transmit	Transmitting antenna (Default: 01)
	1	Reception (not during CCA)	Receiving antenna (Default: 01)
		Reception (during CCA)	Antenna set by TX_ANT
		Transmit	Antenna set by TX_ANT
1	0	Reception (not during CCA)	Antenna during or after the search
		Reception (during CCA)	Antenna during or after the search
		Transmit	Transmitting antenna (Default: 01)
	1	Reception (not during CCA)	During search : Antenna during the search
		Reception (during CCA)	Antenna set by TX_ANT
		Transmit	Antenna set by TX_ANT

For ANT1 or ANT2 in 2DIV_RSLT[2-1], the following antenna switch truth-value lists (with [2DIV_CNTRL] register (B0 0x71) bit2 (INV_TRX_SW) = 0b0, bit3 (INV_ANT_SW) = 0b0, and bit5 (ANT_CTRL1) = 0b0) are assumed.

SPDT switch

ANT_SW pin	Antenna
0	ANT1
1	ANT2

DPDT switch

TRX_SW Pin	ANT_SW Pin	ANT1⇔ LNA_P	ANT1⇔ PA_OUT	ANT2⇔ LNA_P	ANT2⇔ PA_OUT	Transmitting and receiving antenna
0	1	ON	OFF	OFF	ON	Receive: ANT1 Transmit: ANT2
1	0	OFF	ON	ON	OFF	Receive: ANT2 Transmit: ANT1

About forced ANT_SW and TRX_SW pin setting

To control the ANT_SW and TRX_SW pins forcibly, set [2DIV_CNTRL] register (B0 0x71) bit0 (2DIV_EN) to 0b0, and turn off the diversity search. Then, set bit1 (2PORT_SW) to 0b0 regardless of the used RF_SW type. Also, set [INT_SOURCE_GRP2] register (B0 0x25) bit1 (INT[09]) to 0b0. Otherwise, the forced setting does not function.

The ANT_SW pin output can be set by bit5 (TX_ANT_EN) and bit1 (2DIV_RSLT2) as shown in the following table.

Forced ANT_SW setting (with 2DIV_EN = 0b0, 2PORT_SW = 0b0, and INT[09] = 0b0)

TX_ANT_EN	2DIV_RSLT2 (*1)	ANT_SW pin (Pin#20)
0	0b0	L
	0b1	H
1	0b0	L/ bit4 setting value (TX_ANT) (at transmission or when CCA is running)
	0b1	H/ bit4 setting value (TX_ANT) (at transmission or when CCA is running)

(* 1) Any value written to 2DIV_RSLT1 does not affect this setting.

The TRX_SW pin output can be set by [2DIV_CNTRL] register (B0 0x71) bit2 (INV_TRX_SW) as shown in the following table.

Forced TRX_SW setting (with 2DIV_EN = 0b0, 2PORT_SW = 0b0, and INT[09] = 0b0)

INV_TRX_SW (B0 0x71)	TRX_SW pin (Pin #21)
0	L
1	H

[RF_CNTRL_SET] register (B0 0x75) can be used for forced setting. However, the forced setting function is disabled if [2DIV_CNTRL] register (B0 0x71) bit1 (2PORT_SW) is set to 0b1. Here is the priority of the forced settings.

RF_CNTRL_SET(B0 0x75) > INV_TRX_SW(B0 0x71) > TX_ANT_EN/TX_ANT (during CCA or transmission) > 2DIV_RSLT2

[Note]

0b0 can be written to 2DIV_RSLT[2-1]. Note that, if it is written during reception (after the diversity search), the antenna specified by this diversity search is changed. Avoid writing to 2DIV_RSLT[2-1] during reception.

0x73[ANT1_ED]

Function: ED value register for ANT1
Address: 0x73
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	ED_ANT1[7:0]	ED value register for ANT1	0000_0000	R

[Detail description]

1. [2DIV_CONTL] register (B0, 0x71) 2DIV_EN bit has to be 0b1
2. This register is cleared when the diversity detection completion interrupt is cleared or when the diversity is restarted automatically.

0x74[ANT2_ED]

Function: ED value register for ANT2
Address: 0x74
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	ED_ANT1[7:0]	ED value register for ANT2	0000_0000	R

[Detail description]

1. [2DIV_CONTL] register (B0, 0x71) 2DIV_EN bit has to be 0b1
2. This register is cleared when the diversity detection completion interrupt is cleared or when the diversity is restarted automatically.

0x75[RF_CNTRL_SET]

Function: Configuration of RF control pin (ANT_SW, TRX_SW, DCNT)
Address: 0x75
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7	Reserve	Reserved	0	R/W
6	DCNT_SET	Programmable output at DCNT pin. 0: Output “L” 1: Output ”H”	0	R/W
5	ANT_SW_SET	Progtammable output at ANT_SW pin. 0: Output “L” 1: Output ”H”	0	R/W
4	TRX_SW_SET	Programmable output at TRX_SW pin 0: Output “L” 1: Output ”H”	0	R/W
3	Reserve	Reserved	0	R/W
2	DCNT_EN	Access to programmable port at DCNT (1: programmable)	0	R/W
1	ANT_SW_EN	Access to programmable port at ANT_SW (1: programmable)	0	R/W
0	TRX_SW_EN	Access to programmable port at TRX_SW (1: programmable)	0	R/W

[Note]

1. This register enable to have programmability to ANT_SW (#20 pin), TRX_SW (#21 pin) and DCNT pin(#22 pin). This register will override internal block function.
2. [PA_CNTRL] register (B1, 0x07) bit5 (EXT_PA_OIT) has to be 0b0 (CMOS output: Default Value) to use DCNT pin as programmable pin.
3. [SW_OUT/RAMP_ADJ] register (B1, 0x08) bit6 (ANTSW_OUT) has to be 0b0 (CMOS output: Default Value) to use ANT_SW pin as programmable pin.
4. [SW_OUT/RAMP_ADJ] register (B1, 0x08) bit6 (TRXSW_OUT) has to be 0b0 (CMOS output: Default Value) to use TRX_SW pin as programmable pin.

0x77[CRC_AREA/FIFO_TRG]

Function: CRC computation area and FIFO trigger setting
Address: 0x77
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-2	Reserve	Reserved	0000_00	R/W
1	CRC_AREA	CRC computation field (*1) 0: bit sequence after Length field (PHR excluded) 1: bit sequence after SFD field (PHR included)	0	R/W
0	FIFO_TRG_EN	Output monitor of FIFO trigger from DMON pin. 0: Output disabled 1: Out put enabled	0	R/W

[Note]

*1 It has to be 0b1 in case of IEEE802.15.4d mode.
*2 [CLK_SET] register bit4 (CLKOUT_EN) has to be 0b0 to monitor FIFO trigger from DMON (#17 pin)

0x78[RSSI_MON]

Function: RSSI data output
Address: 0x78
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R
5-0	RSSI[5:0]	A/D conversion result of Received signal (RSSI)	00_0000	R

[Note]
1. As ADC is shared with the temperature acquisition, this register value is undefined while the temperature information is being acquired.
2. Update period of A/D conversion is 17.8uS if ADC clock is configured by [ADC_CLK_SET] register (B0, 0x08) is default value of 1.8MHz. It will be 16.0uS if ADC clock become 2MHz.

0x79[TEMP_MON]

Function: Temperature data output
Address: 0x79
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
-0	TEMP[7:0]	A/D conversion result of temperature measurement	0000_0000	R

[Note]
1. In case of measuring temperature, 75kÙof load resistance has to be attached to A_MON pin, and [RSSI/TEMP_OUT] register（B1, 0x03）bit5 (TEMP_ADC_OUT) has to be 0b1.
2. Temperature measurement result can be detected all operating state except for sleep mode.

0x7A[PN9_SET_L]

Function: Initial root value for PN9 hardware used for Whitening process (lower 8bits)
Address: 0x7a
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	PN9[7:0]	Initial root value of PN9 generator (bit7 to bit0)	0000_0000	R/W

[Detail description]
1. See the [PN9_SET_H] register (B0 0x7b).[]

0x7B[PN9_SET_H]

Function: Default Value for PN9 hardware used for Whitening process (upper 1bit) and enable control
Address: 0x7b
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7	PN9_EN	PN9 enable control 0: stop PN9 generation 1: execute PN9 generation	0	R/W
6-1	Reserved	Reserved	000_000	R
0	PN9[8]	Initial root value of PN9 generator (bit8) (*1)	0	R/W

[Detail description]

1. If PN9_EN is set to 0b1, PN9 continues to operate synchronizing with CLK0_EN (enabled when [CLK_SET] register (B0 0x02) bit0 is set to 1).
2. The PN9 operation starts from the initial value (= 9'h1FF). Run the burst read when reading PN9_SET_L/PN9_SET_H.

[Note]

*1 This function shares the PN9 circuit with the Whitening function. Use this function while the Whitening function is not running and set PN9_EN = 1.

0x7C[RD_FIFO_LAST]

Function: FIFO remaining size or address of FIFO
Address: 0x7c
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	FIFO_LAST[7:0]	FIFO remaining size (up to 255) or address of FIFO	0000_0000	R

[Detail description]

1. If [PACKET_MODE_SET] register (B0, 0x45) bit7 (FIFO_ADR_EN)=0b1, this register will show address of FIFO.
2. Packet length (2bytes) can be read and writ via FIFO, it will be stored separated from data FIFO (256bytes), remaining size of FIFO will not count Length field size.
3. Address of FIFO shows next address to write in TX, and next address to read in RX.
4. Remaining size of TX FIFO is only available during data transmission is active. Similarly, remaining size of RX FIFO is only available during data reception is active.

[Note]

1. If a portion of the FIFO is read while receiving data, FIFO_LAST must be controled to more than 8'01.

0x7E[WR_TX_FIFO]

Function: TX FIFO data
Address: 0x7e
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	TX_FIFO[7:0]	TX FIFO (bit7 to bit0)	0000_0000	W

[Note]

1. This LSI has 2 banks of 256byte FIFO. However valid size of FIFO is defined by register [PACKET_MODE_SET] (B0, 0x45) bit1 (IEEE_MODE). If it is 0b0, IEEE 802.15.4d mode is selected and the size will be 128 byte.
2. FIFO0 will be filled by data first. This LSI will manage which bank will be available to write.
3. Maximam 2packets of data will be stored independe from packet length. If both banks stores the data, FIFO is overwritten by the next write operation, and the transmit FIFO access error interrupt (INT[15]) occurs. If an access error occurs, discard the FIFO data.
4. If data is written while receiving data, data will be written in other bank of FIFO.

0x7F[RD_RX_FIFO]

Function: RX FIFO data
Address: 0x7f
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	RX_FIFO[7:0]	RX FIFO (bit7 to bit0)	0000_0000	R

[Note]

1. This LSI has 2 banks of 256byte FIFO. However valid size of FIFO is defined by register [PACKET_MODE_SET] (B0, x45) bit1 (IEEE_MODE). If it is 0b0, IEEE 802.15.4d mode is selected and the size will be 128 byte.
2. FIFO0 will be filled by data first. This LSI will manage which bank will be available to write.
3. Maximam 2packets of data will be stored independe from packet length. If both banks stores the data, FIFO is overwritten by the next write operation (to store the received data), and the receive FIFO access error interrupt (INT[14]) occurs. If an access error occurs, discard the FIFO data.

●Register BANK1

0x00[BANK_SEL]

Function: Register access destination (BANK) select
Address: 0x00
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7	TST_ACEN	Test register access enable (*2) 0: Access forbidden 1: Access permitted	0	R/W
6-2	Reserved	Reserved	000_00	R/W
1-0	BANK[1:0]	BANK select BANK[1:0]＝x00: Access to BANK0 x01: Access to BANK1 x10: Access to BANK2 x11: Forbidden (*1)	00	R/W

[Notes]
*1 Writing x11 to this field is forbbiden.
*2 This bit will affect permission of register access, see “register map” section.

0x01[DEMOD_SET]

Function: Demodulator setting
Address: 0x01
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7	BER_MODE_ON	BER measurement mode enable 0: Normal reception mode 1: BER measurement mode	0	R/W
6-4	Reserved	Reserved	000	R/W
3	STR_HOLD_ON	Symbol timming recovery control 0: Maintain symbol timing after SFD detected. 1: Continue symbol timing tracking	0	R/W
2	AFC_LIM_OFF	AFC limitter control 0: AFC limitter enabled 1: AFC limitter disabled	0	R/W
1	AFC_HOLD_ON	AFC mode setting 0: Maintain AFC after SFD detected 1: Continue AFC tracking	0	R/W
0	AFC_OFF	AFC control 0: AFC_OFF disabled (*1) 1: AFC_OFF enabled	0	R/W

[Note]
*1 If AFC is disabled, AFC value will be relevant to frequency offset is zero.

0x02[RSSI_ADJ]

Function: RSSI data adjustment
Address: 0x02
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7	RSSI_ADD	RSSI adjustment 0: set as - 1: set as +	0	R/W
6-5	Reserved	Reserved	00	R/W
4-0	RSSI_ADJ[4:0]	RSSI adjustment value	0_0000	R/W

[Detail description]
1. Please refer to “Energy Detection (ED) value adjustment” section for more information.

0x03[RSSI/TEMP_OUT]

Function: Output setting for RSSI and Temperature data
Address: 0x03
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5	TEMP_ADC_OUT	Digital output setting for temperature data (*1) 0: Digital output disabled 1:Digital output enabled	0	R/W
4	TEMP_OUT	Analog output setting for temperature data (*2) 0: Analog output disabled 1: Analog output enabled	0	R/W
3-1	Reserved	Reserved	000	R/W
0	RSSI_OUT	Output control of RSSI signal to A_MON pin (*2) 0: Output disabled. 1: Output enabled.	0	R/W

[Detail description]
*1 Output value can be read from [TEMP_MON] register (B0, 0x79)
*2 Signal can be monitored at A_MON pin (#24 pin)

[Note]
1. Do not put 0b1 at same time, correct value will not be output.

0x04[PA_ADJ1]

Function:PA adjustment register1
Address: 0x04
Default Value 0x77

Bit	Symbol	Description	Default Value	R/W
7-4	PA_ADJ1_H[4:0]	Adjustment value for 20mW output PA.	0111	R/W
3-0	PA_ADJ1_L[4:0]	Adjustment value for 1mW output PA	0111	R/W

[Detail description]
1. See section “PA adjustment”
2. This register will be valid if [PA_CNTRL] register (B1, 0x07) bit1-0(PA_ADJ_SEL[1:0])=0b01.
3. With this register, output power can be adjusted 0.1dB to 0.7dB per step and 2.5 to 3.5 dB in total in 20mW output PA. Similarly power can be adjusted 0.3 to 1.2dB per step and 10dB in total range. Approx. 0.5dB step of adjustment can be done by [PA_REG_ADJ1] register (B1, 0x33) and 0.1dB step of fine tuning is also available by [PA_REG_FINE_ADJ] register (B1, 0x013).
4. Adjustment range will be depended by supply voltage setting [PA_REG_ADJ1] register.

0x05[PA_ADJ2]

Function: PA adjustment register2
Address: 0x05
Default Value 0x77

Bit	Symbol	Description	Default Value	R/W
7-4	PA_ADJ2_H[4:0]	Adjustment value for 20mW output PA.	0111	R/W
3-0	PA_ADJ2_L[4:0]	Adjustment value for 1mW output PA	0111	R/W

[Detail description]

1. See section “PA adjustment”
2. This register will be valid if [PA_CNTRL] register (B1, 0x07) bit1-0(PA_ADJ_SEL[1:0])=0b10.
3. With this register, output power can be adjusted 0.1dB to 0.7dB per step and 2.5 to 3.5 dB in total in 20mW output PA. Similarly power can be adjusted 0.3 to 1.2dB per step and 10dB in total range. Approx. 0.5dB step of adjustment can be done by [PA_REG_ADJ2] register (B1, 0x34) and 0.1dB step of fine tuning is also available by [PA_REG_FINE_ADJ] register (B1, 0x013).
4. Adjustment range will be depended by supply voltage setting [PA_REG_ADJ2] register.

0x06[PA_ADJ3]

Function: PA adjustment register3
Address: 0x06
Default Value 0x77

Bit	Symbol	Description	Default Value	R/W
7-4	PA_ADJ3_H[4:0]	Adjustment value for 20mW output PA.	0111	R/W
3-0	PA_ADJ3_L[4:0]	Adjustment value for 1mW output PA	0111	R/W

[Detail description]

1. See section “PA adjustment”
2. This register will be valid if [PA_CNTRL] register (B1, 0x07) bit1-0(PA_ADJ_SEL[1:0])=0b11.
3. With this register, output power can be adjusted 0.1dB to 0.7dB per step and 2.5 to 3.5 dB in total in 20mW output PA. Similarly power can be adjusted 0.3 to 1.2dB per step and 10dB in total range. Approx. 0.5dB step of adjustment can be done by [PA_REG_ADJ2] register (B1, 0x35) and 0.1dB step of fine tuning is also available by [PA_REG_FINE_ADJ] register (B1, 0x013).
4. Adjustment range will be depended by supply voltage setting [PA_REG_ADJ3] register.

0x07[PA_CNTRL]

Function: External PA control and PA mode setting
Address: 0x07
Default Value 0x13

Bit	Symbol	Description	Default Value	R/W
7	EXT_PA_CNT	Output timing of DCNT signal 0: Synchronized to PA_ON timing 1: Synchronized to TX_ON timing	0	R/W
6	EXT_PA_INV	DCNT output polarity (*1) 0: postive logic 1: negative logic	0	R/W
5	EXT_PA_OUT	Output type of DCNT pin 0: CMOS logic output 1: Open Drain output	0	R/W
4	PA_SEL	Select PA circuit (*2) 0: Select 1mW output PA 1: Select 20mWoutput PA	1	R/W
3-2	Reserves	Reserved	00	R/W
1-0	PA_ADJ_SEL[1:0]	PA adjustment register set (*1) 00: Prohibited 01: Select PA_ADJ1 register 10: Select PA_ADJ2 register 11: Select PA_ADJ3 register	11	R/W

[Detail description]

1. External PA control signal will output from DCNT pin (#22 pin)

*1 This register bit will be applied to logical signal controlled by [SW_OUT/RAMP_ADJ] register (B1, 0x08) bit4 (EXT_PA_EN).
*2 see section “PA adjustment”

0x08[SW_OUT/RAMP_ADJ]

Function: Timing parameter for ANT_SW/TRX_SW signal control
Address: 0x08
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7	ANTSW_OUT	Output type of ANT_SW pin 0: CMOS output 1:Open Drain output	0	R/W
6	TRXSW_OUT	Output type of TRX_SW 0: CMOS output 1:Open Drain output	0	R/W
5	Reserved	Reserved	0	R/W
4	EXT_PA_EN	DCNT pin control 0: fixed to ”L” 1: Control as EXT_PA Ouput “H” in TX operation, otherwise output “L”	0	R/W
3-0	RAMP_ADJ[3:0]	Time adjustment of PA ramping up (*1) 0b0000: OFF (9usec) 0b0001: +10.1 usec : : 0b1111: +25.1 usec	0000	R/W

[Detail description]
Rump Up time for PA is adjusted (approximately 1.1us/step).

[Note]
*1 Default timing parameter for rampin up and ramping down will be used. By increasing register value, ramping time will be extended.

0x09[PLL_CP_ADJ]

Function: Current adjustment for PLL charge pump
Address: 0x09
Default Value 0x44

Bit	Symbol	Description	Default Value	R/W
7	Reserved	Reserved	0	R/W
6-4	PLL_CP_TX[2:0]	PLL charge pump current during TX mode	100	R/W
3	Reserved	Reserved	0	R/W
2-0	PLL_CP_RX[2:0]	PLL chage pump current during RX mode	100	R/W

0x0A[IF_FREQ_H]

Function: IF frequency setting (upper 8bits)
Address: 0x0a
Default Value 0x14 (IF frequency: 178.22kHz)

Bit	Symbol	Description	Default Value	R/W
7-0	IF_FREQ[15:8]	IF frequency setting (bit15 to bit8)	0001_0100	R/W

[Detail description]
1. IF frequency will be changed depending on data rate defined by [DATA_SET] register (B0, 0x47) bit2-0 (RATE[2:0]).

[Note]
2. See section “IF frequency setting”

0x0B[IF_FREQ_L]

Function: IF frequency setting (lower 8bits)
Address: 0x0b
Default Value 0x47 (IF Frequency:178.22kHz)

Bit	Symbol	Description	Default Value	R/W
7-0	IF_FREQ[7:0]	IF frequency setting (bit7 to bit0)	0100_0111	R/W

[Detail description]
1. IF frequency will be changed depending on data rate defined by [DATA_SET] register (B0, 0x47) bit2-0 (RATE[2:0]).

[Note]
1. See section “IF frequency setting”

0x0C[IF_FREQ_CCA _H]

Function: IF frequency setting during CCA operation (upper 8bits)
Address: 0x0c
Default Value 0x14

Bit	Symbol	Description	Default Value	R/W
7-0	IF_FREQ_CCA[15:8]	IF frequency setting in CCA operation (bit15 to bit8)	0001_0100	R/W

[Detail description]
1. IF frequency will be changed depending on data rate defined by [DATA_SET] register (B0, 0x47) bit2-0 (RATE[2:0]).

[Note]
1. See section “IF frequency setting”

0x0D[IF_FREQ_CCA_L]

Function: IF frequency setting during CCA operation (lower 8bits)
Address: 0x0d
Default Value 0x47

Bit	Symbol	Description	Default Value	R/W
7-0	IF_FREQ_CCA[7:0]	IF frequency setting in CCA operation (bit7 to bit0)	0100_0111	R/W

[Note]
1. See section “IF frequency setting”

0x0E[BPF_ADJ_H]

Function: Bandwidth adjustment in Band-Pass-Filter (upper 2bits)
Address: 0x0e
Default Value 0x02

Bit	Symbol	Description	Default Value	R/W
7-2	Reserved	Reserved	0000_00	R/W
1-0	BPF_C[9:8]	Bandwidth adjustment in Band-Pass-Filter (bit9,bit8)	10	R/W

[Note]
1. See section “Band-Pass-Filter setting”

0x0F[BPF_ADJ_L]

Function: Bandwidth adjustment in Band-Pass-Filter (lower 8bits)
Address: 0x0f
Default Value 0x04

Bit	Symbol	Description	Default Value	R/W
7-0	BPF_C[7:0]	Bandwidth adjustment in Band-Pass-Filter (bit7 to bit0)	0000_0100	R/W

[Note]
1. See section “Band-Pass-Filter setting”
2. NBO_SEL = 1 cannot be set in rates other than 50kbps/100kbps/200kbps.

0x10[BPF_CCA_ADJ_H]

Function: Bandwidth adjustment in Band-Pass-Filter during CCA operation (upper 2bits)
Address: 0x10
Default Value 0x01

Bit	Symbol	Description	Default Value	R/W
7-2	Reserved	Reserved	0000_00	R/W
1-0	BPF_C_CCA[9:8]	Bandwidth adjustment in Band-Pass-Filter during CCA operation (bit9, bit8)	01	R/W

[Note]
1. See section “Band-Pass-Filter setting”

0x11[BPF_CCA_ADJ_L]

Function: Bandwidth adjustment in Band-Pass-Filter during CCA operation (lower 8bits)
Address: 0x11
Default Value 0x10

Bit	Symbol	Description	Default Value	R/W
7-0	BPF_C_CCA[7:0]	Bandwidth adjustment in Band-Pass-Filter during CCA operation (bit7 to bit0)	0001_0000	R/W

[Note]
1. See section “Band-Pass-Filter setting”
2. NBO_SEL = 1 cannot be set in rates other than 50kbps/100kbps/200kbps.

0x12[RSSI_LPF_ADJ]

Function: Time constant adjustment for RSSI output
Address: 0x12
Default Value 0x1F

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5-0	RSSI_LPF_R[5:0]	Time constant adjustment for RSSI output	01_1111	R/W

0x13[PA_REG_FINE_ADJ]

Function: Trimming adjustment for PA regulator
Address: 0x13
Default Value 0x10

Bit	Symbol	Description	Default Value	R/W
7-5	Reserved	Reserved	0	R/W
4-0	PA_REG_ADJ[4:0]	Output voltage fine trimming in PA regulator	001_0000	R/W

[Detail description]
1. It is possible to adjust output voltage of PA regurater in 0.1dB step. Fine trimming function cancel device variation with high accuracy.
2. 1step is correspond to approximately 14mV.

0x14[IQ_MAG_ADJ]

Function: Amplitude balance adjustment for IF I/Q signals
Address: 0x14
Default Value 0x08

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5	IQ_CAL_LNA_EN	Calibration test pattern generator control for IQ signal in LNA block. 0: Disabled 1: Enabled	0	R/W
4	IQ_CAL_MIX_EN	Calibration test pattern generator control for IQ signal in Mixer block 0: Disabled 1: Enabled	0	R/W
3-0	MAG_TRM[4:0]	Amplitude balance adjustment for IQ signal in Mixer block	1000	R/W

[Note]
1. Image rejection ratio can be improved by this register. See section “I/Q signal adjustment”

0x15[IQ_PHASE_ADJ]

Function: Phase balance adjustment for IF I/Q signals
Address: 0x15
Default Value 0x20

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5-0	IF_Q[5:0]	Phase balance adjustment for IF BPF IQ signals	10_0000	R/W

[Note]
1. Image rejection ratio can be improved by this register. See section “I/Q signal adjustment”

0x16[VCO_CAL_MIN_FL]

Function: VCO minimam operating frequency (lower 8bits)
Address: 0x16
Default Value 0x55

Bit	Symbol	Description	Default Value	R/W
7-0	VCO_CAL_MIN_F[7:0]	VCO minimam operating frequency (bit7 to bit0)	0101_0101	R/W

0x17[VCO_CAL_MIN_FM]

Function: VCO minimam operating frequency (middle 8bits)
Address: 0x17
Default Value 0x55

Bit	Symbol	Description	Default Value	R/W
7-0	VCO_CAL_MIN_F[15:8]	VCO minimam operating frequency (bit15 to bit8)	0101_0101	R/W

0x18[VCO_CAL_MIN_FH]

Function: VCO minimam operating frequency (upper 4bits)
Address: 0x18
Default Value 0x09

Bit	Symbol	Description	Default Value	R/W
7-4	Reserved	Reserved	0000	R/W
3-0	VCO_CAL_MIN_F[19:16]	VCO minimam operating frequency (bit19 to bit16)	1001	R/W

[Detail description]

1. See section “VCO_CAL operation”
2. See also setction“setting VCO minimam operating frequency”

[Note]

1. Please configure lower frequency limit to 2MHz lower than actual operating frequency.

0x19[VCO_CAL_MAX_N]

Function: VCO maximam operating frequency
Address: :0x19
Default Value :0x07

Bit	Symbol	Description	Default Value	R/W
7-5	Reserved	Reserved	000	R/W
4-0	VCO_CAL_MAX_N[4:0]	VCO maximam operating frequency (⊿F) (*1)	0_0111	R/W

[Detail description]
1. See section “Adjusting VCO”

[Note]
*1. Operating frequency has be with in range upto upper frequency limit.
*2. It can be used only when VCO_CAL_MIN_FL (B1 0x16), VCO_CAL_MIN_FM(B1 0x17), and VCO_CAL_MIN_FH(B1 0x18) are set to all "0x00" (36MHz x n).

0x1A[VCO_CAL_MIN]

Function: Status register for lower side of VCO caliburation result
Address: 0x1A
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7	Reserved	Reserved	0	R/W
6-0	VCO_CAL_MIN[6:0]	Status register for lower side of VCO calibration result	000_0000	R/W

[Detail description]
1. See section “Adjusting VCO”
2. Calibratio operation will be performed by register [VCO_CAL_EN] (B1, 0x1d) and result will be stored in this register.

0x1B[VCO_CAL_MAX]

Function: Stauts register for upper side of VCO caliburation result
Address: 0x1b
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7	Reserved	Reserved	0	R/W
6-0	VCO_CAL_MAX[6:0]	Status register for upper side of VCO calibration result	000_0000	R/W

[Detail description]
1. See section “Adjusting VCO”
2. Calibratio operation will be performed by register [VCO_CAL_EN] (B1, 0x1d) and result will be stored in this register.

0x1C[VCO_CAL]

Function: Stauts register for current VCO caliburation value
Address: 0x1c
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7	CAL_WR_EN	Enable overwite of calibration register 0: Auto Caliburation mode 1: Overwrite mode	0	R/W
6-0	VCO_CAL[6:0]	Current VCO calibration result	000_0000	R/W

[Detail description]

1. See section “Adjusting VCO”
2. VCO_CAL[6:0] register will be applied during calibration operation
   In Auto Calibration mode, VCO calibration value which is currently used is stored.
   If Overwrite mode (CAL_WR_EN=1b1), the value in VCO_CAL[6:0] will be overwritten to current value.
3. VCO_CAL[6:0] will be updated each time TX_ON or RX_ON is activated.

0x1D[VCO_CAL_START]

Function: VCO caliburation control
Address: 0x1d
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-1	Reserved	Reserved	0000_000	R/W
0	VCO_CAL_START	Enable VCO calibration 0: Operation completed 1: Perform calibration operation	0	R/W

[Detail description]

1. See section “Adjusting VCO”

0x1E[BPF_ADJ_OFFSET]

Function: Offset data for BPF adjustment
Address: 0x1e
Default Value 0xxx

Bit	Symbol	Description	Default Value	R/W
7-0	BPF_OFFSET_POL	Polarity of BPF adjustment offset 0: set as - 1: set as +	x	R
6:0	BPF_OFFSET[6:0]	BPF adjustment offset absolute value	xxx_xxxx	R

[Detail description]

1. BPF adjustment offset value can be read by this register, its value will have device variation.
2. See section “BPF_ADJ correction”

0x2B[ID_CODE]

Function: ID code
Address: 0x2b
Default Value 0x11

Bit	Symbol	Description	Default Value	R/W
7-0	LSI_ID[7:0]	ID code of LSI version 0x11: ML7396 0x12: ML7396B, ML7396A, or ML7396E	0001_0001	R

0x33[PA_REG_ADJ1]

Function: PA regulator adjustment register1
Address: 0x33
Default Value 0x07

Bit	Symbol	Description	Default Value	R/W
7-3	Reserved	Reserved	0000_0	R/W
2-0	PA_REG_ADJ1 [2:0]	PA regulator adjustment register 1	111	R/W

[Detail description]

1. See section “PA adjustment”
2. It is possible to adjust PA output at 0.5dB step
3. 1 step will correspond to approximately 0.1V

[Note]

If the voltage is too high, the transmitter power output decreases with decreasing supply voltage.

0x34[PA_REG_ADJ2]

Function: PA regulator adjustment register2
Address: 0x34
Default Value 0x07

Bit	Symbol	Description	Default Value	R/W
7-3	Reserved	Reserved	0000_0	R/W
2-0	PA_REG_ADJ2 [2:0]	PA regulator adjustment register 2	111	R/W

[Detail description]

1. See section “PA adjustment”
2. It is possible to adjust PA output at 0.5dB step
3. 1 step will correspond to approximately 0.1V

[Note]

If the voltage is too high, the transmitter power output decreases with decreasing supply voltage.

0x35[PA_REG_ADJ3]

Function: PA regulator adjustment register 3
Address: 0x35
Default Value 0x07

Bit	Symbol	Description	Default Value	R/W
7-3	Reserved	Reserved	0000_0	R/W
2-0	PA_REG_ADJ3 [2:0]	PA regulator adjustment register 3	111	R/W

[Detail description]

1. See section “PA adjustment”
2. It is possible to adjust PA output at 0.5dB step
3. 1 step will correspond to approximately 0.1V

[Note]

If the voltage is too high, the transmitter power output decreases with decreasing supply voltage.

0x3A[PLL_CTRL]

Function: RF adjustment
Address: 0x3A
Initial value: 0x9F

Bit	Register Name	Description	Initial value	R/W
7-5	Reserved	Reserved	100	R/W
4	PLL_SD_PS	Frequency setting load timing switch for PLL	1	R/W
3-0	Reserved	Reserved	1111	R/W

[Detail description]

Set the frequency setting load timing switch for PLL.

1: Rising edge for VCO dividing output

0: Falling edge for VCO dividing output

When using one unit channel specified in ARIB STD-T108, set 0b0 in order to improve the ACP characteristics. When using two unit channels, both 0b0 and 0b1 can be set.

0x3F[RX_ON_ADJ2]

Function: RX_ON adjustment register 2 setting
Address: 0x3F
Initial value: 0x02

Bit	Register Name	Description	Initial value	R/W
7	Reserved	Reserved	0	R/W
6-4	TIM_RX_ON2[2:0]	Receive switching timing adjustment when transitioning to RX_ON following TX_ON (Setting value + 1) x 8.88usec	000	R/W
3-0	Reserved	Reserved	0010	R/W

[Detail description]
It is enabled when [RAMP_CNTRL] register (B2 0x2C) bit4 (TXOFF_RAMP_EN) is set 0b1.
For details, see "Lamp control function."
[Note]
1. For this register, set a value specified in "Initial setting registers" and do not change it for adjustment.

0x49[LNA_GAIN_ADJ_M]

Function: LNA gain adjustment in middle gain operation
Address: 0x49
Default Value 0x0E

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5-0	LNA_MGAIN[5:0]	LNA gain adjustment in middle gain operation	00_1110	R/W

[Note]
1. Appropriate value are given by ”Initial setting for register”, do not change to other value

0x4A[LNA_GAIN_ADJ_L]

Function: LNA gain adjustment in lower gain opration
Address: 0x4a
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5-0	LNA_LGAIN[5:0]	LNA gain adjustment in lower gain operation	00_0000	R/W

[Note]
1. Appropriate value are given by ”Initial setting for register”, do not change to other value

0x4D[MIX_GAIN_ADJ_H]

Function: Mixer gain adjustment for large gain
Address: 0x4E
Initial value: 0xFF

Bit	Register Name	Description	Initial value	R/W
7-0	MIX_HGAIN[7:0]	Mixer gain adjustment for large gain	1111_1111	R/W

[Note]
1. For this register, set a value specified in "Initial setting registers" and do not change it for adjustment.

0x4E[MIX_GAIN_ADJ_M]

Function: Mixer gain adjustment in middle gain operation
Address: 0x4E
Default Value 0xFF

Bit	Symbol	Description	Default Value	R/W
7-0	MIX_MGAIN[7:0]	Mixer gain adjustment in middle gain operation	1111_1111	R/W

[Note]
1. Appropriate value are given by ”Initial setting for register”, do not change to other value

0x4F[MIX_GAIN_ADJ_L]

Function: Mixer gain adjustment in lower gain operation
Address: 0x4F
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	MIX_LGAIN[7:0]	Mixer gain adjustment in lower gain operation	0000_0000	R/W

[Note]
1. Appropriate value are given by ”Initial setting for register”, do not change to other value

0x55[TX_OFF_ADJ1]

Function: TX_OFF adjustment register 1 setting
Address: 0x55
Initial value: 0x00

Bit	Register Name	Description	Initial value	R/W
7-0	TIM_TX_OFF1[7:0]	Lamp down timing adjustment when transitioning from TX_ON to TX_OFF (Setting value + 1) x 2.22usec	0000_0000	R/W

[Detail description]
It is enabled when [RAMP_CNTRL] register (B2 0x2C) bit4 (TXOFF_RAMP_EN) is set 0b1.
For details, see ″Lamp control function.″
[Note]
1. For this register, set a value specified in "Initial setting registers" and do not change it for adjustment.

0x5A[RSSI_SLOPE_ADJ]

Function: RSSI slope adjustment
Address: 0x5A
Default Value 0x07

Bit	Symbol	Description	Default Value	R/W
7-4	Reserved	Reserved	0000	R/W
3-0	RSSI_SLOPE[3:0]	RSSI slope adjustment	0111	R/W

[Note]
1. Appropriate value are given by ”Initial setting for register”, do not change to other value

●Register BANK2

0x00[BANK_SEL]

Function: Register access destination (BANK) select
Address: 0x00
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7	TST_ACEN	Test register access enable (*2) 0: Access forbidden 1: Access permitted	0	R/W
6-2	Reserved	Reserved	000_00	R/W
1-0	BANK[1:0]	BANK select BANK[1:0]＝x00: Access to BANK0 x01: Access to BANK1 x10: Access to BANK2 x11: Forbidden (*1)	00	R/W

[Notes]
*1 Writing x11 to this field is forbbiden.
*2 This bit will affect permission of register access, see “register map” section.

0x12[SYNC_MODE]

Function: Mode setting for bit synchronization
Address: 0x12
Default Value 0x04

Bit	Symbol	Description	Default Value	R/W
7-3	Reserved	Reserved	0000_0	R/W
2	SYNC_MODE	Mode setting for bit synchronization *1 0: For BER measurement 1: For normal operation	1	R/W
1-0	Reserved	Reserved	00	R/W

[Detail description]
*1 PN9 data for BER does not include enough preamble length to detect, alternative algorithm will be used during BER measurement.
You need to set 0b0 for SYNC_MODE when measuring BER.
If you set 0b0 for SYNC_MODE when diversity search is not used, this LSI internally and automatically switches it to 0b1.

0x1E[PA_ON_ADJ]

Function: Timing adjustment for PA_ON signal
Address: 0x1E
Default Value 0x0A

Bit	Symbol	Description	Default Value	R/W
7-0	PA_ON_ADJ[7:0]	Timing adjustment for PA_ON signal (register value +1) x 8.88uS	0000_1010	R/W

[Note]
1. Appropriate value are given by ”Initial setting for register”, do not change to other value

0x1F[DAT_IN_ADJ]

Function: DATA Input timing adjustment
Address: 0x1F
Initial value: 0x1A

Bit	Register Name	Description	Initial value	R/W
7-0	DAT_IN_ADJ[7:0]	Data Input timing adjustment (Setting value + 1) x 1.11usec	0001_1010	R/W

[Note]
1. For this register, set a value specified in "Initial setting registers" and do not change it for adjustment. This setting is necessary only for 400kbps.

0x22[RX_ON_ADJ]

Function: Timing adjustment for RX_ON signal
Address: 0x22
Default Value 0x01

Bit	Symbol	Description	Default Value	R/W
7-0	RX_ON_ADJ[7:0]	Timing adjustment for RX_ON signal (register value+1) x 8.88uS	0000_0001	R/W

[Note]
1. Appropriate value are given by ”Initial setting for register”, do not change to other value

0x24[RXD_ADJ]

Function: Timing adjustment for RXD signal
Address: 0x24
Default Value 0x59

Bit	Symbol	Description	Default Value	R/W
7-0	RXD_ADJ[7:0]	Timing adjustment for RXD signal (register value+1) x1.11uS	0101_1001	R/W

[Note]
1. Appropriate value are given by ”Initial setting for register”, do not change to other value

0x2A[RATE_ADJ1]

Function: Reception adjustment at rate other than 50/100/200/400kbps (lower 8 bits)
Address: 0x2A
Initial value: 0x01

Bit	Register Name	Description	Initial value	R/W
7-0	RATE_ADJ[7:0]	Reception adjustment at rate other than 50/100/200/400kbps (lower 8 bits)	0000_0001	R/W

[Detail description]
It is enabled when [RATE_ADJ2] register (B2 0x2B) bit4 (RATE_ADJ_EN) is set 0b1.Set as follows for 150kbps.

Receiving state	RATE_ADJ[9:0]
Not during CCA	0x2BE
During CCA	0x17C

[Note]
1. For this register, set a value specified in "Initial setting registers" and do not change it for adjustment.
2. For 10kbps/20kbps/40kbps, see "Initial setting register."

0x2B[RATE_ADJ2]

Function: Reception adjustment enable/adjustment at rate other than 50/100/200/400kbps (higher 2 bits)
Address: 0x2B
Initial value: 0x01

Bit	Register Name	Description	Initial value	R/W
7-5	Reserved	Reserved	000	R/W
4	RATE_ADJ_EN	Reception adjustment enable at rate other than 50/100/200/400kbps	0	R/W
3-2	Reserved	Reserved	11	R/W
1-0	RATE_ADJ[9:8]	Reception adjustment at rate other than 50/100/200/400kbps (higher 2 bits)	11	R/W

[Detail description]
This register bit1-0 is enabled when bit4 (RATE_ADJ_EN) is set 0b1. For 150kbps, see details on [RATE_ADJ1] register.

[Note]
1. For this register, set a value specified in "Initial setting registers" and do not change it for adjustment.
2. For 10kbps/20kbps/40kbps, see "Initial setting register."

0x2C[RAMP_CNTRL]

Function: Lamp control/FEC control setting
Address: 0x2c
Initial value: 0x00

Bit	Register Name	Description	Initial value	R/W
7-6	Reserved	Reserved	00	R/W
5	Reserved	Reserved	0	R/W
4	TXOFF_RAMP_EN	Lamp control enable 0:Disable 1: Enable	0	R/W
3-0	Reserved	Reserved	0000	R/W

[Detail description]
When bit4 (TXOFF_RAMP_EN) is set to 0b1, the lamp down timing after the transmission is set to the one specified by [GAIN_CNTRL] register (B0 0x6e) bit7-2 (TX_OFFADJ2), [RX_ON_ADJ2] register (B1 0x3f) bit6-4 (RX_ON_ADJ2), and [TX_OFF_ADJ1] register (B1 0x55).

0x60[ADDFIL_CNTRL]

Function: Address filtering function control
Address: 0x60
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-5	MASK_SET[2:0]	Byte mask configuration in 64bit address mode (*1) Lower side of [register value] bytes are does not taken into account.	000	R/W
4	SHT_ADD1_EN	Short address1 detection (*2) 0: Disabled 1: Enabled	0	R/W
3	SHT_ADD0_EN	Short address 0 detection (*3) 0: Disabled 1: Enabled	0	R/W
2	EXT_ADD_EN	64bit address detection (*4) 0: Disabled 1: Enabled	0	R/W
1	PANID_EN	PANID detection (*5) 0: Disabled 1: Enabled	0	R/W
0	IGB_EN	I/Gbit detection (*6) 0: Disabled 1: Enabled	0	R/W

[Detail description]
1. See section"Address Filtering Function"

*1 MASK_SET[2:0] will be valid only with 64bit address detection mode. Lower side of bytes are not taken into account in address detection.
*2 Address filtering use address values given by [SHT_ADDR1_0] and [SHT_ADDR1_1], (B2, 0x6d and 0x6e).
*3 Address filtering use address values given by [SHT_ADD0_0] and [SHT_ADDR0_1], (B2, 0x6b and 0x6c).
*4 Address filtering use 64bit address given by [64ADDR1] to [64ADDR8] (B2, 0x63 to 0x6a).
*5 It is valid with SHT_ADD0_EN or SHT_ADD1_EN. Address filtering uses address values given by [PANID0] and [PANID1], (B2, 0x61 and 0x62)
(Note: If PANID=xFFFF (Broadcasting), all packets are received)
*6 It is valid with 0b1(64bit address detection) at EXT_ADD_EN, receive data that set 0b1(multicast) at I/G bit.

[Remarks]
For more detail about I/Gbit, please refere to IEEE802.3 standard. I/G: Individula/Group
I/Gbit is allocated in bit0 of 1st octet of OUI of MAC address.(57th bits in 64bit address). It will represent following MAC address is for unicast or multicast.

0x61[PANID_L]

Function: PANID setting for address filtering function (lower 8bits)
Address: 0x61
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	PANID[7:0]	PANID setting (bit7～bit0)	0000_0000	R/W

[Detail description]

1. See section “Address Filter Function”
2. It is valid if [ADDFIL_CNTRL], (b2, 0x60) bit1(PANID_EN)=0b1.
   Lower octet of PANID

0x62[PANID_H]

Function: PANID setting for address filtering function (upper 8bits)
Address: :0x62
Default Value :0x00

Bit	Symbol	Description	Default Value	R/W
7-0	PANID[7:0]	PANID setting (bit15 to bit8)	0000_0000	R/W

[Detail description]

1. See section “Address Filter Function”
2. It is valid if [ADDFIL_CNTRL], (b2, 0x60) bit1(PANID_EN)=0b1.
   Upper octet of PANID

0x63[64ADDR1]

Function: 64bit address setting for address filtering function (1st byte lowest byte)
Address: 0x63
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	64ADDR[7:0]	64 bitAddress setting (bit7 to bit0)	0000_0000	R/W

[Detail description]

1. See section “Address Filter Function”
2. It is valid if [ADDFIL_CNTRL], (b2, 0x60) bit2(EXT_ADD_EN)=0b1
   1st octet of 64bit address

0x64[64ADDR2]

Function: 64bit address setting for address filtering function (2nd byte)
Address: 0x64
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	64ADDR[15:8]	64 bitAddress setting (bit15 to bit8)	0000_0000	R/W

[Detail description]

1. See section “Address Filter Function”
2. It is valid if [ADDFIL_CNTRL], (b2, 0x60) bit2(EXT_ADD_EN)=0b1
   2nd octet of 64bit address

0x65[64ADDR3]

Function: 64bit address setting for address filtering function (3rd byte)
Address: 0x65
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	64ADDR[23:16]	64 bitAddress setting (bit23 to bit16)	0000_0000	R/W

[Detail description]

1. See section “Address Filter Function”
2. It is valid if [ADDFIL_CNTRL], (b2, 0x60) bit2(EXT_ADD_EN)=0b1
   3rd octet of 64bit address

0x66[64ADDR4]

Function: 64bit address setting for address filtering function (4th byte)
Address: 0x66
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	64ADDR[31:24]	64 bitAddress setting (bit31 to bit24)	0000_0000	R/W

[Detail description]

1. See section “Address Filter Function”
2. It is valid if [ADDFIL_CNTRL], (b2, 0x60) bit2(EXT_ADD_EN)=0b1
   4th octet of 64bit address

0x67[64ADDR5]

Function: 64bit address setting for address filtering function (5th byte)
Address: 0x67
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	64ADDR[39:32]	64 bit address setting (bit39 to bit33)	0000_0000	R/W

[Detail description]

1. See section “Address Filter Function”
2. It is valid if [ADDFIL_CNTRL], (b2, 0x60) bit2(EXT_ADD_EN)=0b1
   5th octet of 64bit address

0x68[64ADDR6]

Function: 64bit address setting for address filtering function (6th byte)
Address: 0x68
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	64ADDR[47:40]	664 bit address setting (bit47 to bit40)	0000_0000	R/W

[Detail description]

1. See section “Address Filter Function”
2. It is valid if [ADDFIL_CNTRL], (b2, 0x60) bit2(EXT_ADD_EN)=0b1
   6th octet of 64bit address

0x69[64ADDR7]

Function: 64bit address setting for address filtering function (7th byte)
Address: 0x69
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	64ADDR[55:47]	64 bit address setting (bit55 to bit48)	0000_0000	R/W

[Detail description]

1. See section “Address Filter Function”
2. It is valid if [ADDFIL_CNTRL], (b2, 0x60) bit2(EXT_ADD_EN)=0b1
   7th octet of 64bit address

0x6A[64ADDR8]

Function: 64bit address setting for address filtering function (8th byte, upper byte)
Address: 0x6A
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	64ADDR[63:56]	64 bit address setting (bit63 to bit54)	0000_0000	R/W

[Detail description]

1. See section “Address Filter Function”
2. It is valid if [ADDFIL_CNTRL], (b2, 0x60) bit2(EXT_ADD_EN)=0b1
   8th octet of 64bit address

0x6B[SHT_ADDR0_L]

Function: Short address0 (16bits) setting for address filtering function (lower 8bits)
Address: 0x6b
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	SHT_ADDR0[7:0]	Short address0 setting (bit7 to bit0)	0000_0000	R/W

[Detail description]

1. See section “Address Filter Function”
2. It is valid if [ADDFIL_CNTRL], (b2, 0x60) bit3(SHT_ADD1_EN) or bit4(SHT_ADD0_EN)=0b1.lower octet of short address0

0x6C[SHT_ADDR0_H]

Function: Short address0 (16bits) setting for address filtering function (upper 8bits)
Address: 0x6c
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	SHT_ADDR0[15:8]	Short address0 setting (bit15 to bit8)	0000_0000	R/W

[Detail description]

1. See section “Address Filter Function”
2. It is valid if [ADDFIL_CNTRL], (b2, 0x60) bit3(SHT_ADD1_EN) or bit4(SHT_ADD0_EN)=0b1.upper octet of short address0

0x6D[SHT_ADDR1_L]

Function: Short address1 (16bits) setting for address filtering function (lower 8bits)
Address: 0x6d
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	SHT_ADDR1[7:0]	Short address1 setting (bit7 to bit0)	0000_0000	R/W

[Detail description]

1. See section “Address Filter Function”
2. It is valid if [ADDFIL_CNTRL], (b2, 0x60) bit3(SHT_ADD1_EN) or bit4(SHT_ADD0_EN)=0b1.lower octet of short address1

0x6E[SHT_ADDR1_H]

Function: Short address1 (16bits) setting for address filtering function (upper 8bits)
Address: 0x6e
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	SHT_ADDR1[15:8]	Short address1 setting (bit15 to bit8)	0000_0000	R/W

[Detail description]

1. See section “Address Filter Function”
2. It is valid if [ADDFIL_CNTRL], (b2, 0x60) bit3(SHT_ADD1_EN) or bit4(SHT_ADD0_EN)=0b1.upper octet of short address1

0x6F[DISCARD_COUNT_L]

Function: Number of discarded packet in address filtering function (lower 8bits)
Address: 0x6f
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	DISCARD[7:0]	Number of discarded packet in address filtering function (bit7 to bit0)	0000_0000	R

[Detail description]

1. See section “Address Filter Function”
2. It is possible to count up to 1023 in maximam.
   Set [RST_SET], (b0, 0x01) RST_3 (PHY reset) to clear this register.
   When the address filter is disabled, this register is cleared to 0.

0x70[DISCARD_COUNT_H]

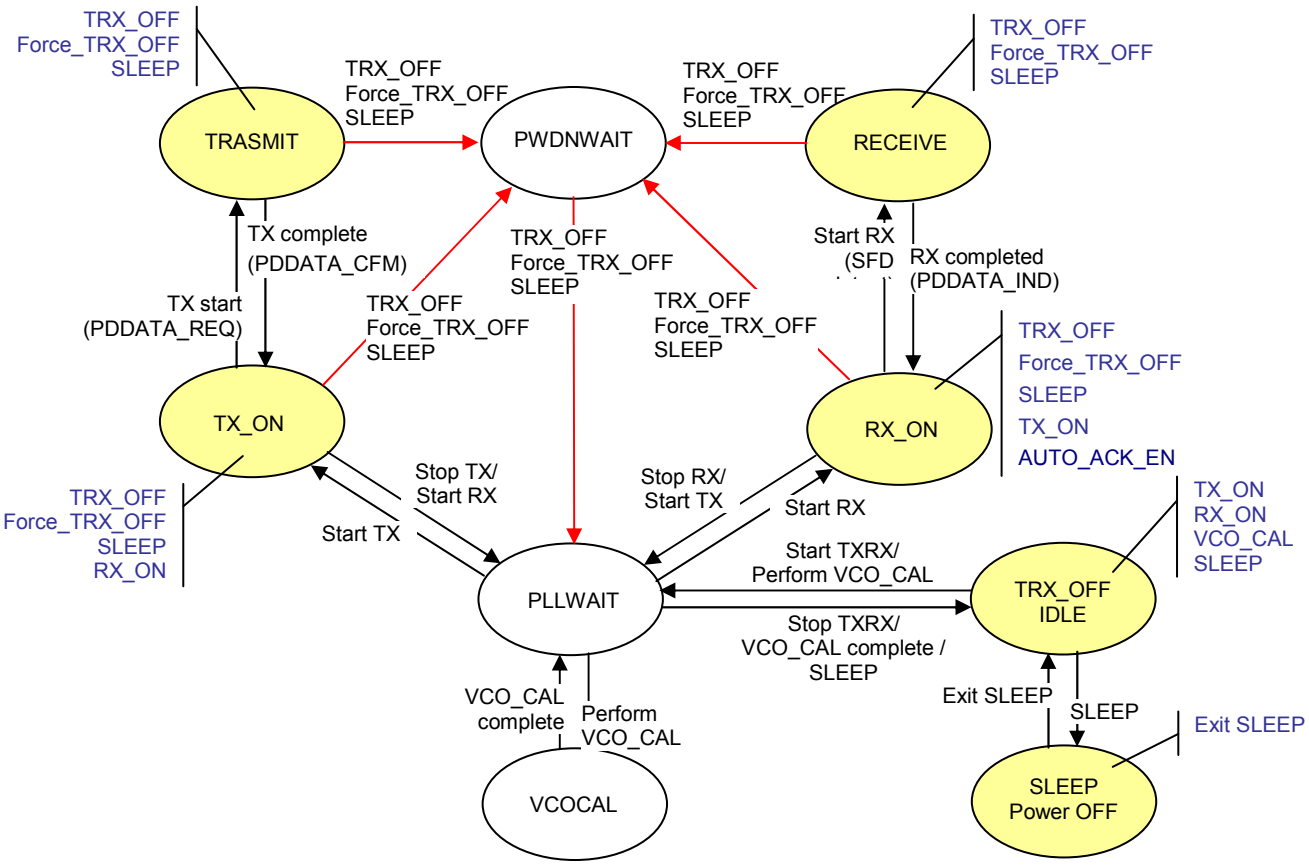
Function: Number of discarded packets in address filtering function (upper 8bits)
Address: 0x6f
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	DISCARD[15:8]	Number of discarded packets in address filtering function (bit15 to bit8)	0000_0000	R

[Detail description]

1. See section “Address Filter Function”
2. It is possible to count up to 1023 in maximam.
   Set [RST_SET], (b0, 0x01) RST_3 (PHY reset) to clear this register.
   When the address filter is disabled, this register is cleared to 0.

■STATE DIAGRAM



[State]

SLEEP/Power OFF	:SLEEP
TRX_OFF/IDLE	:IDLE（Waiting for TXRX start up）
PLL_WAIT	:PLL settling time
TX_ON	:Ready for TX (Wait for TX data)
TRANSMIT	:TX in process
RX_ON	:Ready for RX (Wait for RX data)
RECEIVE	:RX in process
VCO_CAL	:VCO calibration in process
PWDNWAIT	:Power down

State Transition instruction

Normal sequence
（State transition）

Illegal sequence
（State transition）

Control from upper layer

ML7396 self controlled state transition

■FUNCTION: DESCRIPTION

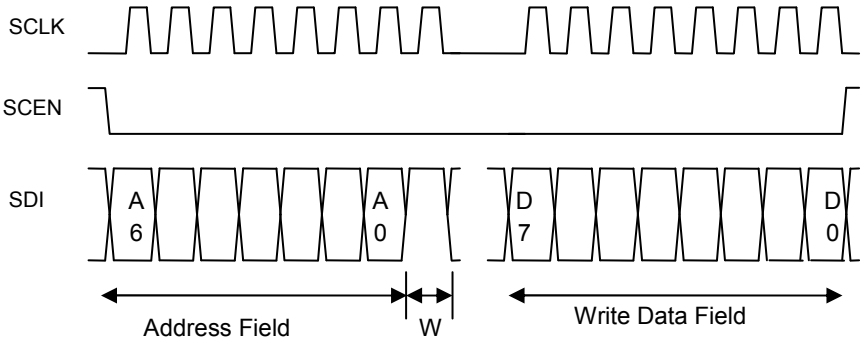
●SPI

Serial Peripheral Interface (SPI) is supported.
It is possible to commnucate with other MCU or peripheral devices.

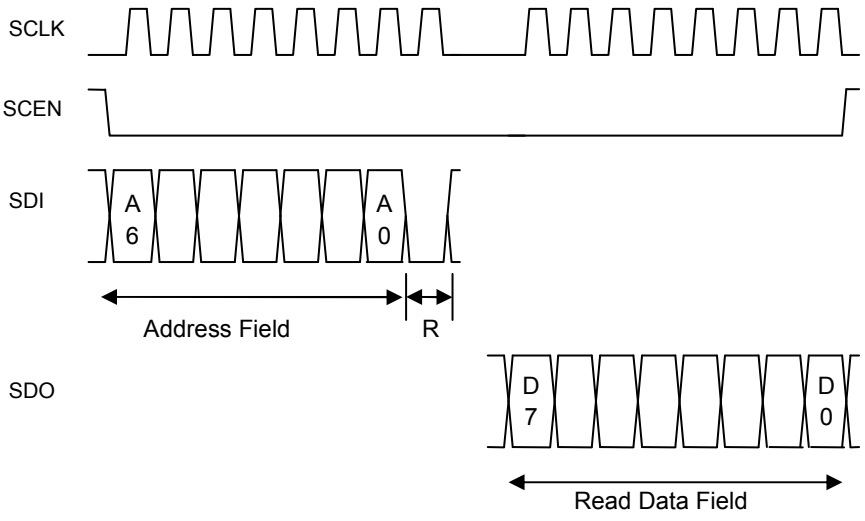
- Half Duplex data transmission
- Slave mode only
- Support Burst access, Single access
- Two banks of TX/RX FIFO（256Byte x 2）

[Single Access Mode]

Write



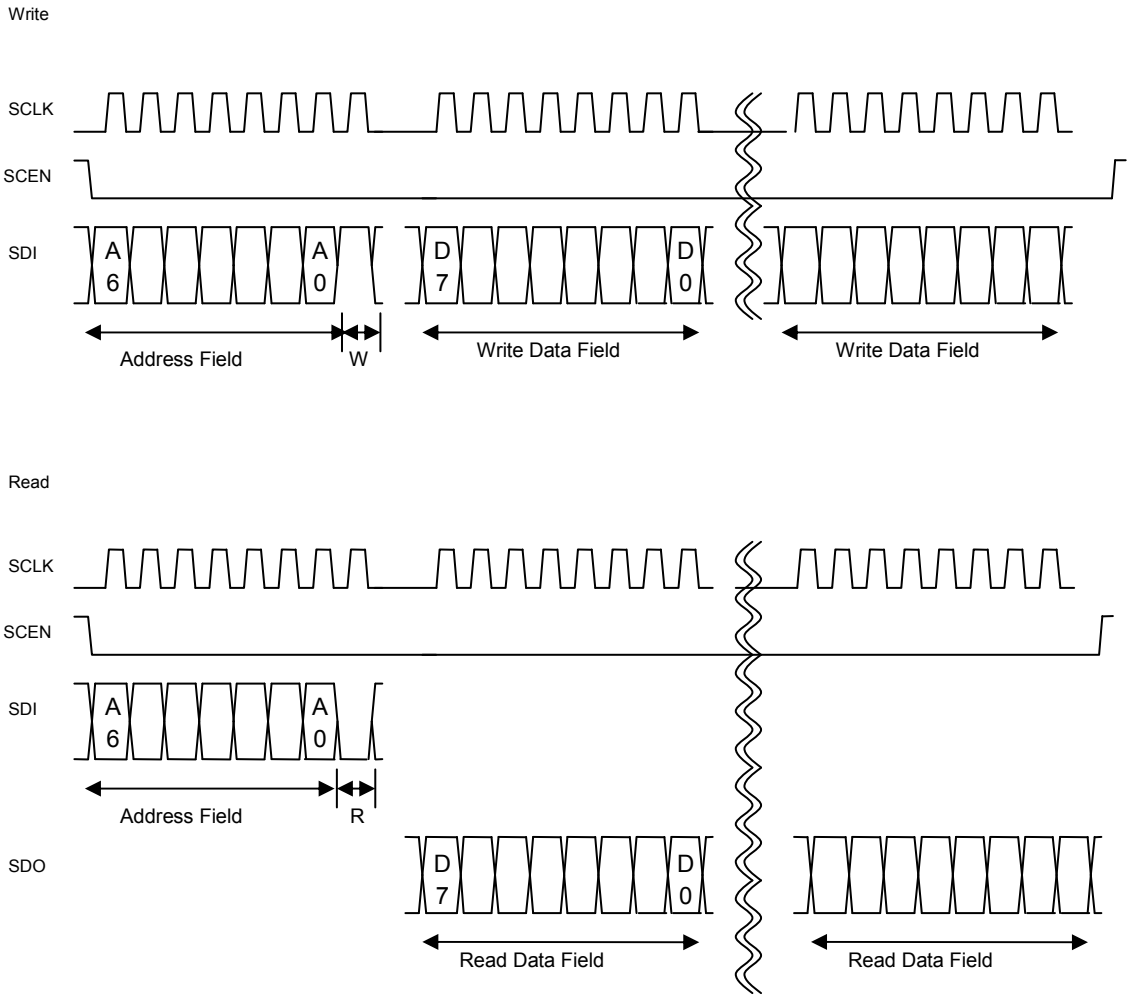
Read



When in write operation, by rising edge of clock which is capturing D0 data, data will be stored into internal blocks.
Control block will be reset by SCEN become H.（Address information will be cleared to 0）

[Note]
You need to read Length + 1 bytes only when reading from FIFO in the IEEE802.15.4d mode (the last one byte is invalid data. It is needed to switch the FIFO banks correctly).

[Burst Access Mode]



By maintaining SCEN as L, Burst Access Mode will be active.
Exiting from Burst Access Mode will be done by SCEN to H.
During Burst Access Mode, address will be automatically incremented.
When SCEN become H before Clock for D0 is input, data transaction will be aborted.
If destination for Burst Access Mode is FIFO（PHYSET108、PHYSET109）, address increment will not be done and same address will be used.

[Note]
You need to read Length + 1 bytes only when reading from FIFO in the IEEE802.15.4d mode (the last one byte is invalid data. It is needed to switch the FIFO banks correctly).

●AFC Function

This LSI has AFC function during RX mode. Frequency difference (max +/- 20ppm) between pier device and local clock will be corrected. AFC function can be activated register [AFC_CNTRL] (B0, 0x34) bit0(AFC_EN)=0b1
This is not supported for data rate settings other than 50/100/150/200/400kbps. Set bit0 (AFC_EN) of [AFC_CNTRL] register (B0 0x34) to 0b0.

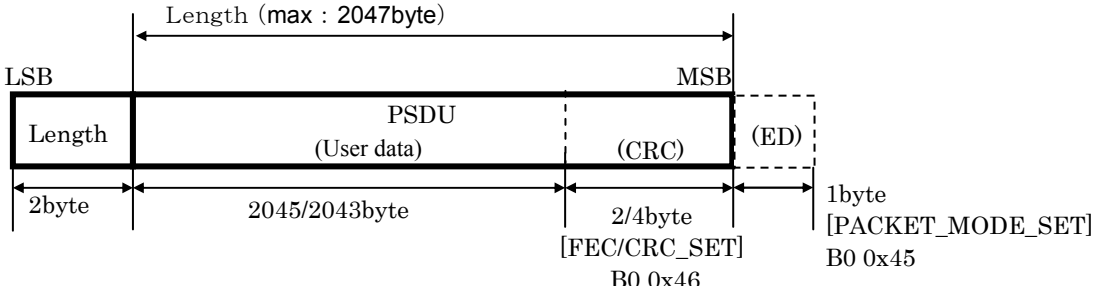
●FIFO

There are two bank of FIFO 256byte each for TX and RX buffer purposes. However, one packet can only use one bank of FIFO (one packet cannot use both banks of FIFO).
While RX_ON, received data from RF block will be stored, and read out by host MCU via SPI. While TX_ON, received data from host MCU will be stored in byte format, transmitted to air via RF.

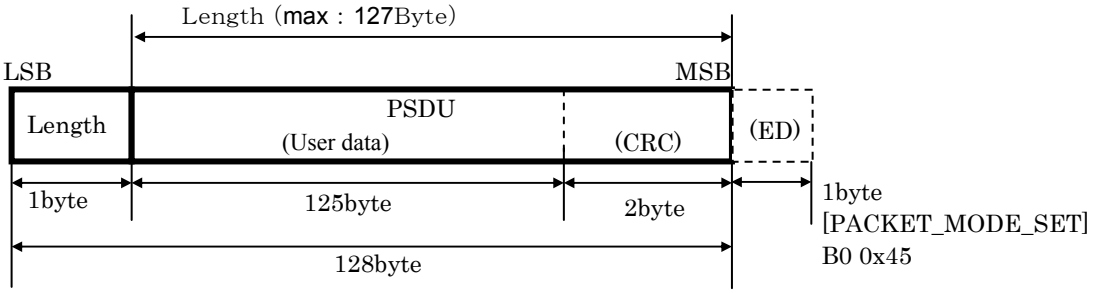
Followings are data format stored in FIFO.

As described below, input data for FIFO is different depending on operation mode.（Mind that neither preamble nor SFD bits are not stored in FIFO in any operation mode）

[IEEE802.15.4g mode（PHYSET51[1]=1）]



[IEEE802.15.4d mode（PHYSET51[1]=0）]



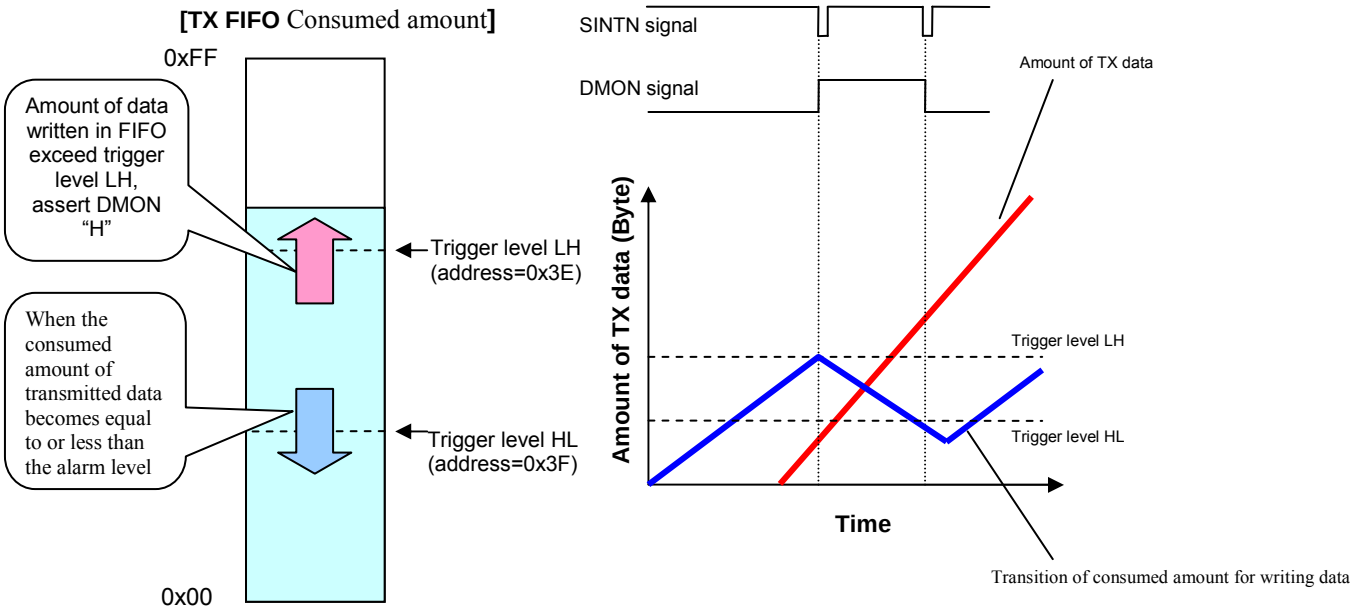
Access to FIFO will be done by SPI burst access. By Writing or Reading data to/from FIFO address (write address 0x7E PHYSET108, read address 0x7F PHYSET109) consecutively, internal address of FIFO will be incremented automatically. If burst access is suspended during reading or writing, address will be kept until packet process will be completed.

Two banks FIFO (bank0, bank1) will be accessed one by another. If in case TX data is required during RX mode operation, RX FIFO will use only single FIFO. Control of using bank number will be done by LSI internally, it is possible to check FIFO status by accessing address 0x28 and 0x29（PHYSET22、PHYSET23）.

[Remarks]Length information must be PSDU length which includes CRC bits. However writing data to FIFO is bits excepts for CRC (2 or 4bytes). Read from FIFO during RX mode includes bits for CRC.

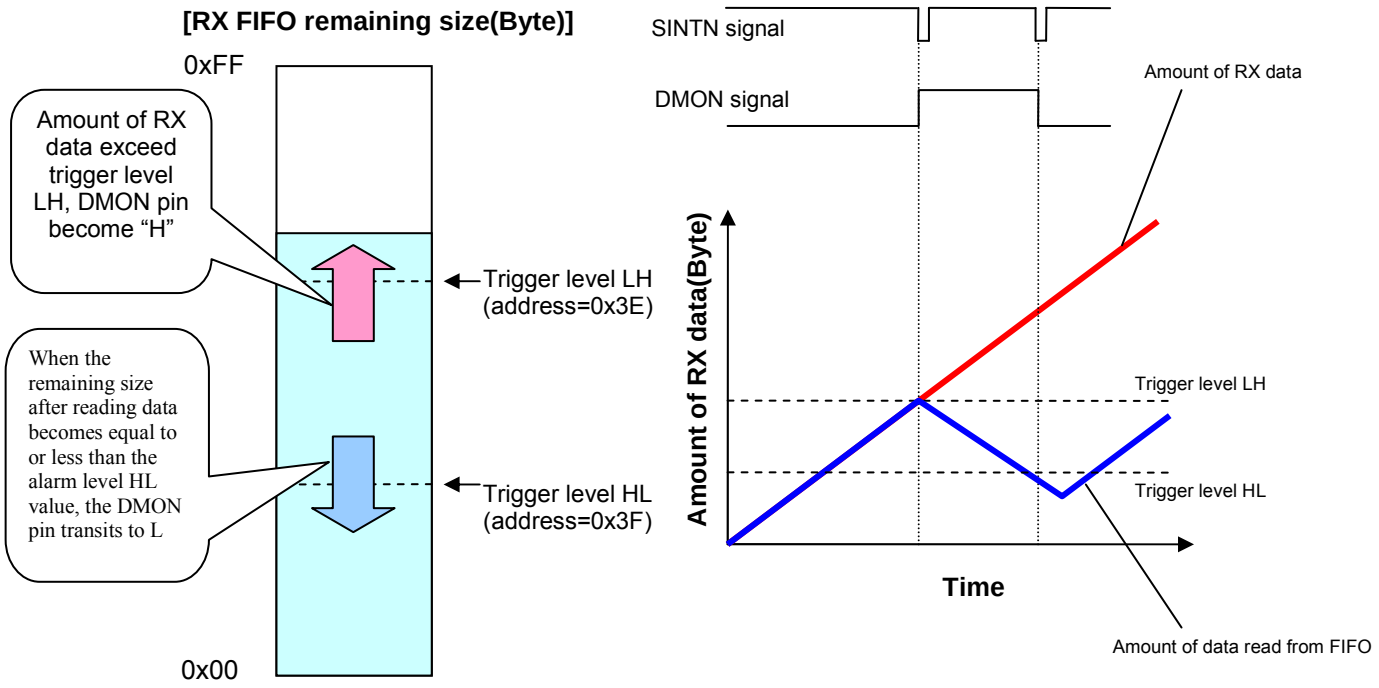
○Reporting TX FIFO Consumed amount

This function is reporting Consumed amount of TX FIFO to host MCU via SINTN (interrupt pin) or DMON pin. If the consumed amount of TX FIFO exceeds the threshold level specified by PHYSET35 (TX_TRG_LH[7:0]), SINTN will be asserted to "L" (or DMON pin become "H"). And if the consumed amount is equal to or less than threshold level specified by PHYSET36 (TX_TRG_HL[7:0]), SINTN will be asserted again (or DMON pin become "L").



○Reporting RX FIFO remaining size

This function is reporting remaining size of RX FIFO to host MCU via SINTN (interrupt pin) or DMON pin. If remaining size of RX FIFO (unread part) exceeds the threshold level specified by PHYSET37 (TRG_LVL_LH[7:0]), SINTN will be asserted to "L" (or DMON pin become "H"). And if remaining size becomes equal to or less than the threshold level specified by PHYSET38 (TRG_LVL_HL[7:0]), SINTN will be asserted again (or DMON pin become "L"), DMON pin will be forced to "L" when RX mode completed.



[Note]

1. If a portion of the FIFO is read while receiving data, FIFO_LAST must be controled to more than 8'h01.

○FIFO control method when FIFO address status is used

(1) At transmission (when bit2 (AUTO_TX) of [PACKET_MODE_SET] register (B0 0x45)=0b1 / FIFO is accessed in units of 128 bits)

①Set bit7 (FIFO_ADR_EN) of [FAST_TX_SET] register (B0 0x6A) and [PACKET_MODE_SET] register (B0 0x45).

②Write data (256 bytes) to [WR_TX_FIFO] register (B0 0x7E) from SPI.

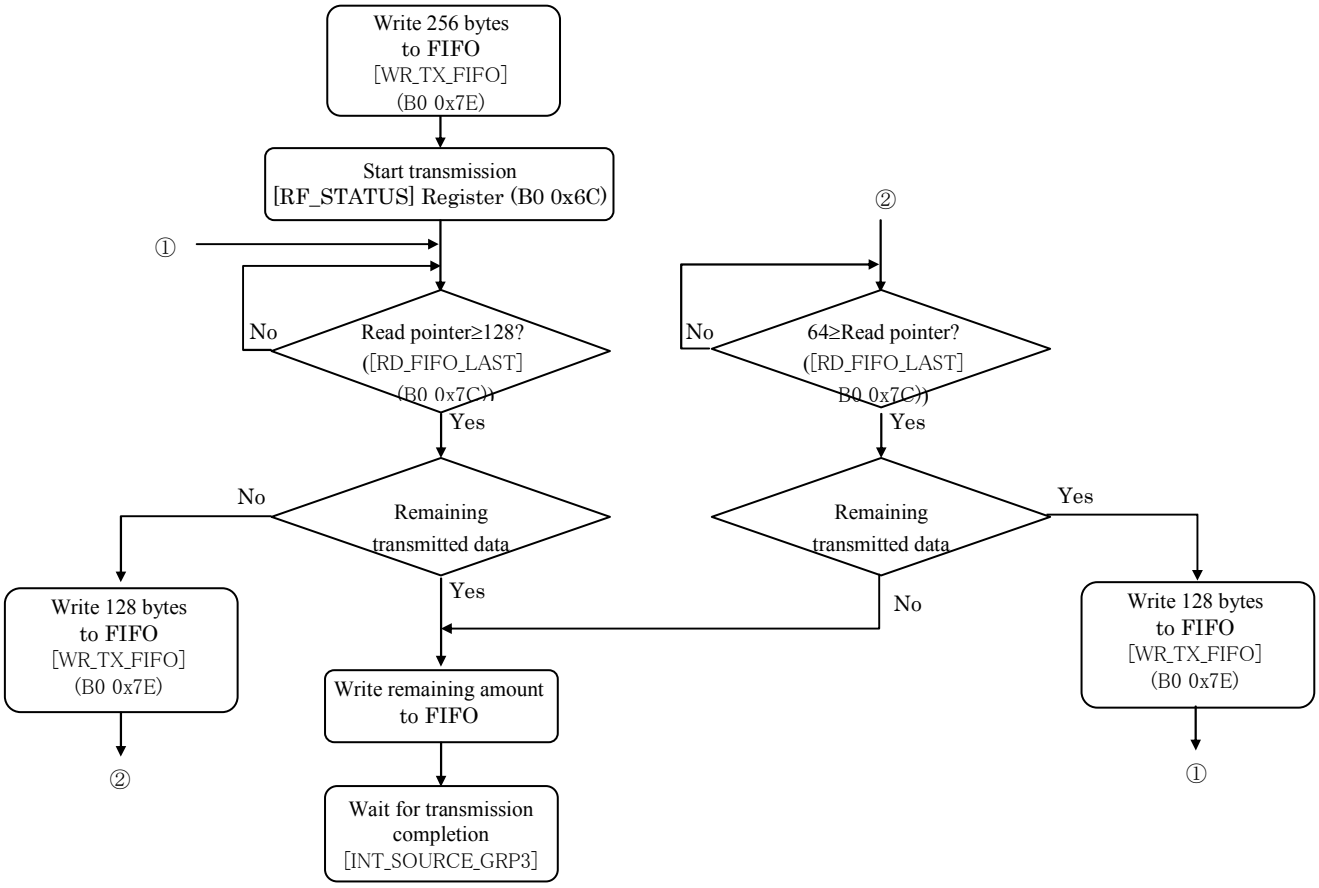
＊When the amount of written data reaches [FIFO_TX_SET] register (B0 0x6A), transmission starts.

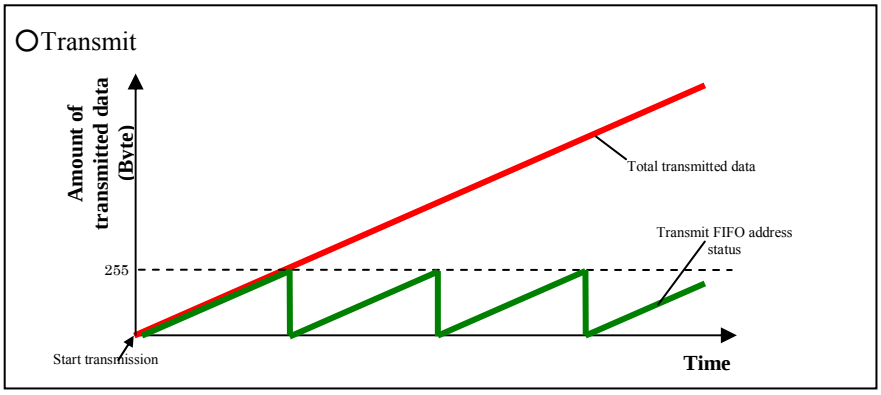
③Check [RD_FIFO_LAST] register (B0 0x7C). When FIFO address status is 128 byte or more and the remaining of transmitted data is 128 bytes or more, 128 bytes is written to FIFO.

④Check [RD_FIFO_LAST] register (B0 0x7C). When FIFO address status is 64 byte or less and the remaining of transmitted data is 128 bytes or more, 128 bytes is written to FIFO.

⑤Repeat ③ and ④ until for the necessary amount of transmitted data.

⑥Check the transmit completion interrupt (bit0 (INT[16])/ bit1 INT[17] of [INT_SOURCE_GRP3] (B0 0x26)) after the last data has been written.





The address status increments after data transmission starts. When 256th byte is transmitted, the address status reverts to 0 to increment again.

(2) At reception (when FIFO is accessed in units of 128 bytes)

①Set bit7 (FIFO_ADR_EN) of [PACKET_MODE_SET] register (B0 0x45) and then set RX_ON (bit3-0 (SET_TRX) of [RF_STATUS] register)(start receiving).

②Check [RD_FIFO_LAST] register (B0 0x7C). When FIFO address is 5 or more, read 5 bytes from FIFO ([RD_RX_FIFO] register (B0 0x7F)). At this time, when the Length is less than 5, the packet is discarded because it is less than the minimum packet length of IEEE802.15.4. When it is equal to or more than 5 and less than 128, wait for receive completion then read the remaining from FIFO. * It is not always true when an original packet format other than IEEE802.15.4 is used.

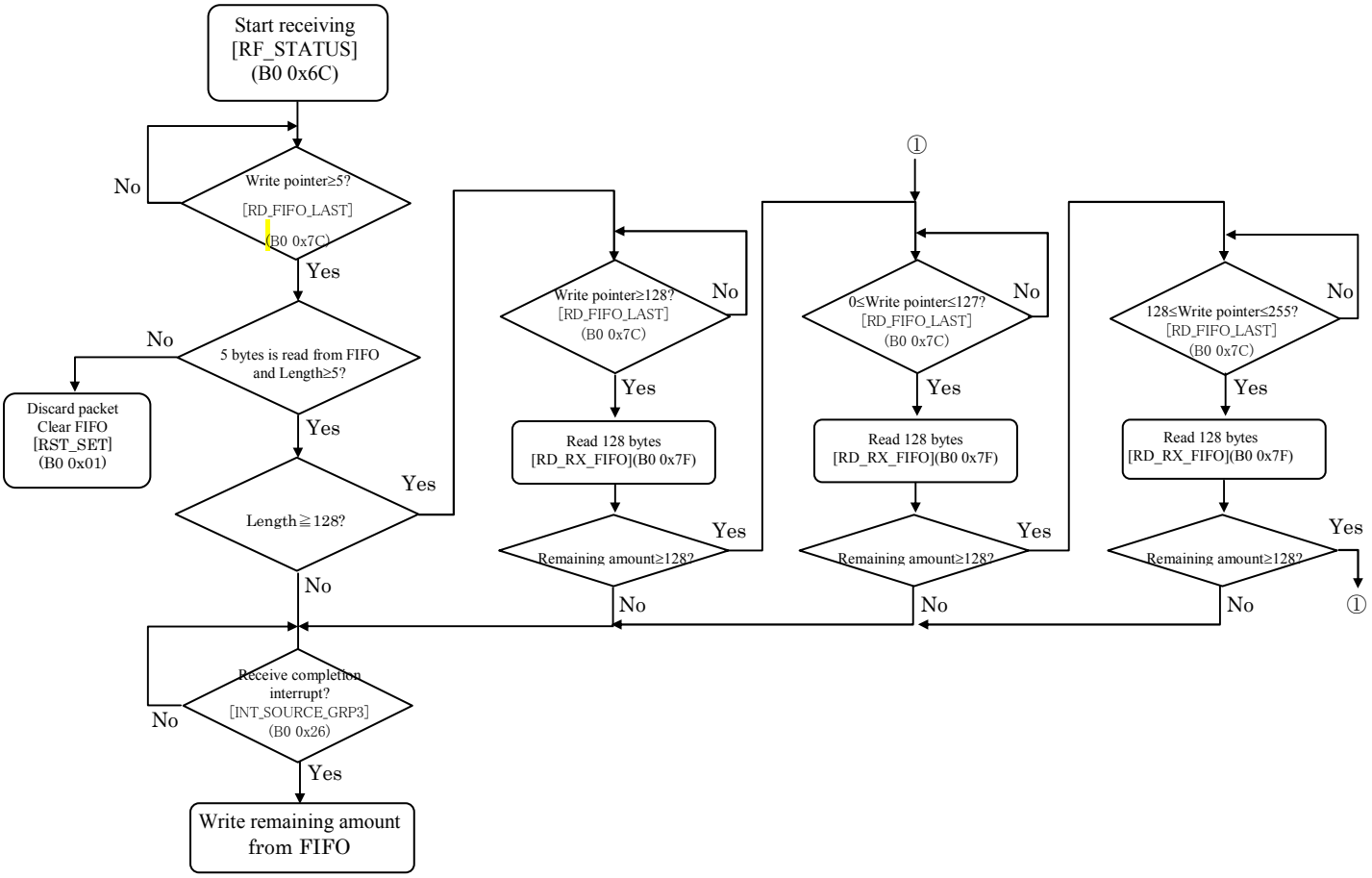
③②When the Length of ② is equal to or more than 128 and FIFO address is 128 or more, read 123 bytes from FIFO. And then, when the remaining amount to read is less than 128, read the remaining from FIFO after receive completion.

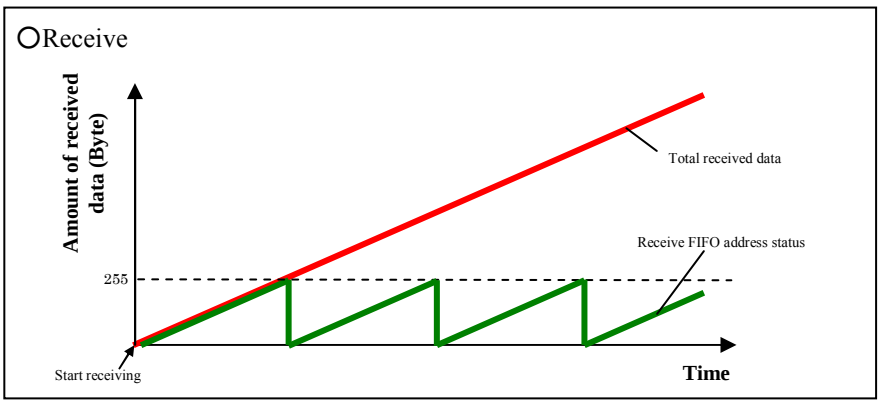
④③When the remaining amount of ③ is equal to or more than 128 and FIFO address is 0 to 127, read 128 bytes from FIFO. And then, when the remaining amount to read is less than 128, read the remaining from FIFO after receive completion.

⑤④When the remaining amount of ④ is equal to or more than 128 and FIFO address is 128 to 255, read 128 bytes from FIFO. And then, when the remaining amount to read is less than 128, read the remaining from FIFO after receive completion.

④Repeat ④ and ⑤ until for the necessary amount of received data.

⑤Check the reception completion interrupt (bit2 (INT[18])/ bit3 (INT[19]) of [INT_SOURCE_GRP3](B0 0x26) and read the remaining amount of received data from FIFO.



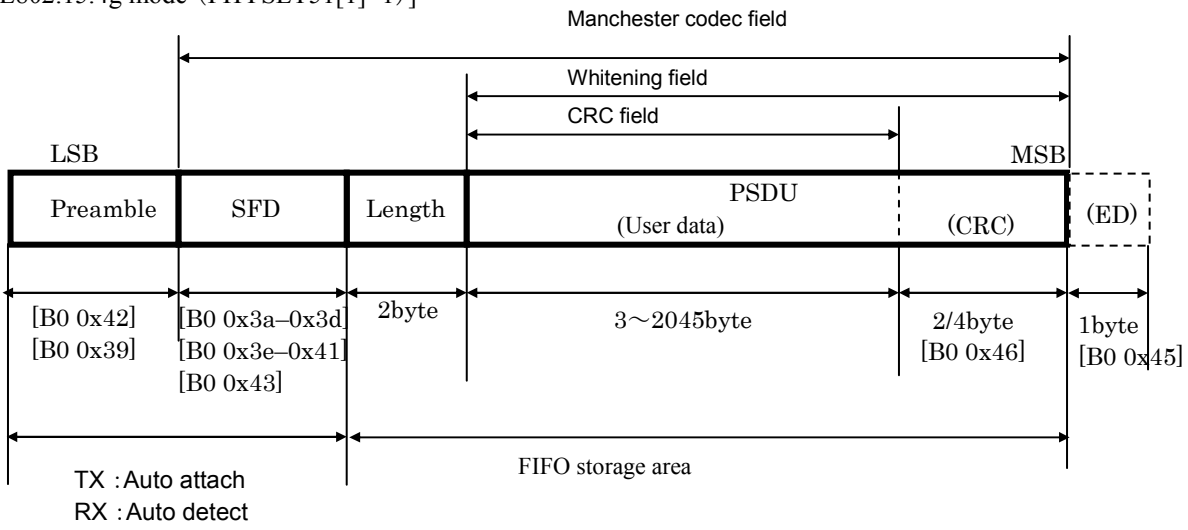


The address status increments after data reception starts. When 256th byte is received, the address status reverts to 0 to increment again.

●Packet Format

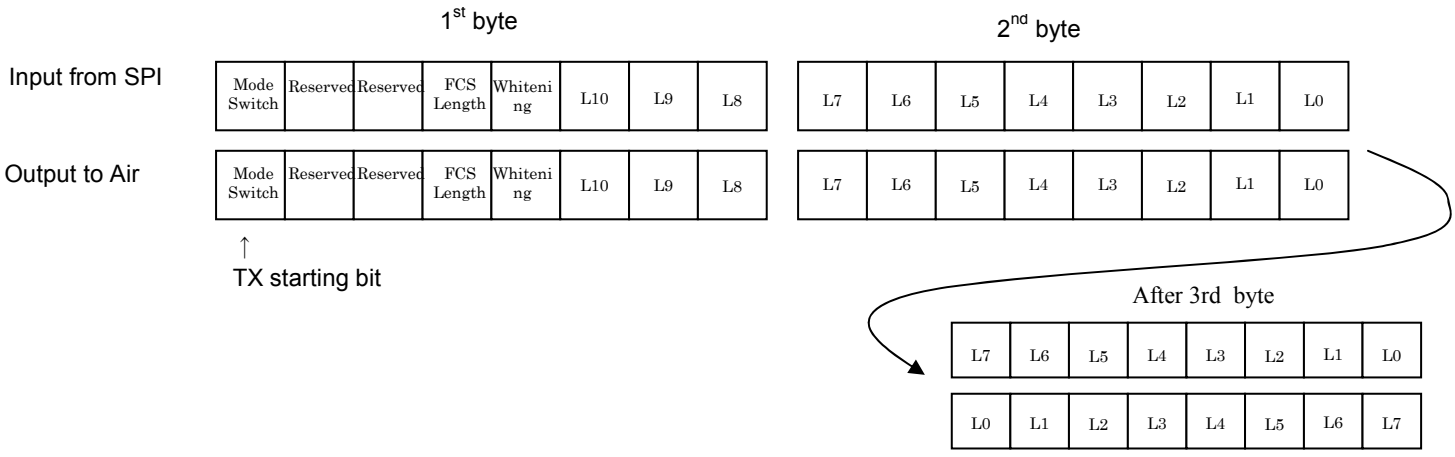
Following packet format is supported. (In the DIO mode, the packet format is Preamble, SFD+DIO data)
It is not necessary to attach or detect preamble and SFD pattern by upper layer stack, those packet format handling will be done by hardware automatically.

[IEEE802.15.4g mode (PHYSET51[1]=1)]

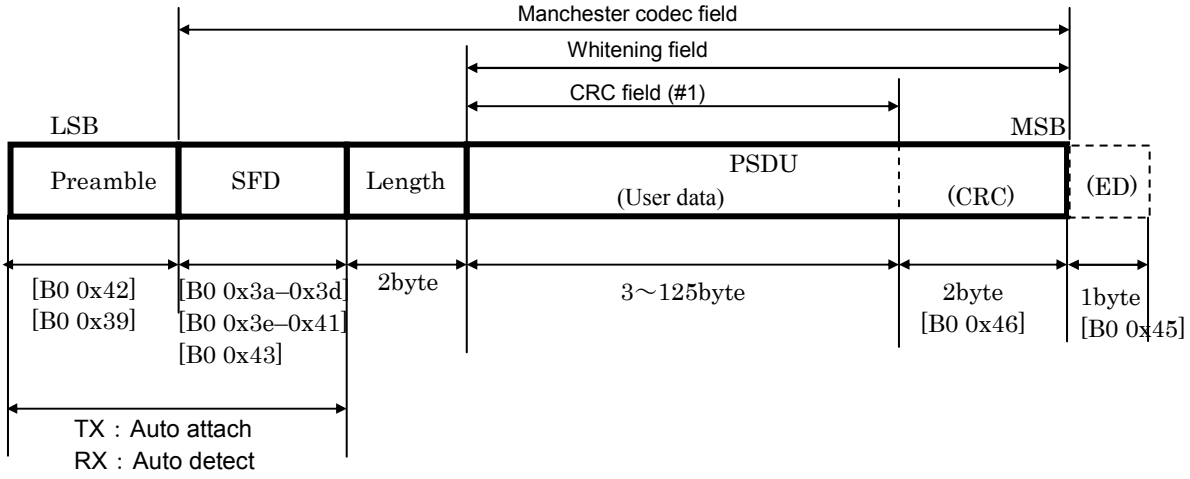


[Remarks]

1. #In IEEE802.15.4g case bit assignment of Length field (PHR) is different from IEEE802.15.4d format. After 3rd byte will be LSB first.
2. For CRC32 setting, the minimum length of user data is 4 bytes. Use CRC16 when 3-bytes data is transmitted/received. For CRC32 setting, ACK packet cannot be received.

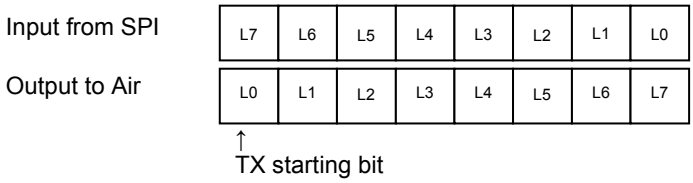


[IEEE802.15.4d mode（PHYSET51[1]=0）]



#1 if EXP_CRC_EN bit (PHYSET101 bit1) is 1 in 802.15.4d mode, CRC computation will be applied to extended to Length field (Length+PSDU).

[Remarks]
#In IEEE802.15.4d case bit assignment of Length field (PHR) is different from IEEE802.15.4g format. LSB first will be used.



●Data Whitening

This LSI support data whitening function which is defined by IEEE 802.15.4g. Default value of data whitening hardware can be configured by register [PN9_SET_L] (B0, 0x7a) and [PN9_SET_H] (B0, 0x7b) PN9[8:0] It is enabled by register [PN9_SET_H] bit7(PN9_EN) bit.

In case of register [PACKET_MODE_SET] (B0,0x45) bit4(Whitening)=0b1, whitening condition is set by bit1(IEEE_MODE) setting.Whitening. Please refer to "Packet Format" for application area.

・In IEEE802.15.4d mode, data whitening applied to TX or RX operation

・In IEEE802.15.4g mode, data whitening will be applied when PHR data whitening bit=0b1

With this function, PN9 generator will start working, and XOR function will be applied to PSDU field of each packet.

TX : En = Rn ⊕ PN9n
RX : Rn = REn ⊕ PN9n

En : Whitening bits
Rn : TX data
PN9n : PN9 pattern（Initial state 111111111）

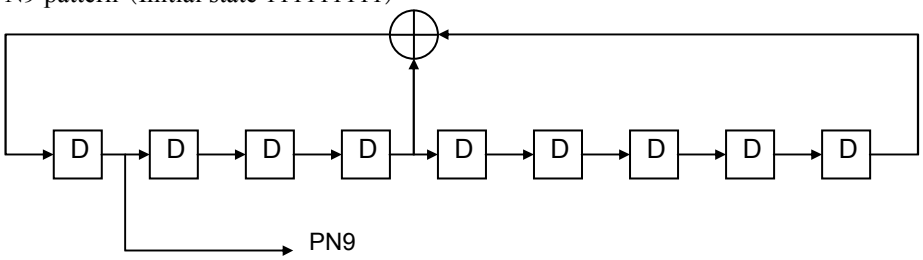
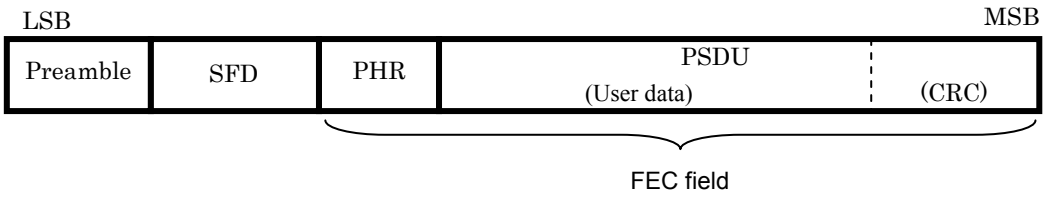


Fig. PN9 pattern generator

●FEC Function

This LSI supports FEC function which is defined in IEEE 802.15.4g standard. FEC function will be applied to PHR and PSDU bit field. Tail bits will be attached at the end of bit sequence in order to return encoder state to zero. Please refer to IEEE 802.15.4g for more details.



●Energy Detection value (ED value) Function

This LSI has function that detect received signal strength indicator (RSSI) as received energy detection value (here in after ED value). ED value function will be started automatically when [ED_CNTRL] register (B0, 0x1b) bit7 (ED_CALC_EN)=0b1, and it is in RX_ON status. While CCA operation is active or diversity operation is active, ED value will be obtained, but ED value register [ED_RESULT] register (B0, 0x16) will not be updated.

Averaging process will be applied to ED values. The number of averaging samples can be defined by register [ED_CNTRL] bit2-0 (ED_AVG[2:0]). In diversity mode, register [2DIV_ED_AVG] (B0, 0x6d) bit2-0 (2DIV_ED_AVG[2:0]) is also used. End of averaging process can be asserted by register [ED_CNTRL] bit4 (ED_DONE) =0b1, [ED_RSLT] register will be updated simultaneously.

ED_DONE bit will be cleared by one of following conditions

① New antenna is selected
② Gain parameter is changed
③ Suspend ED value detection and it is restarted

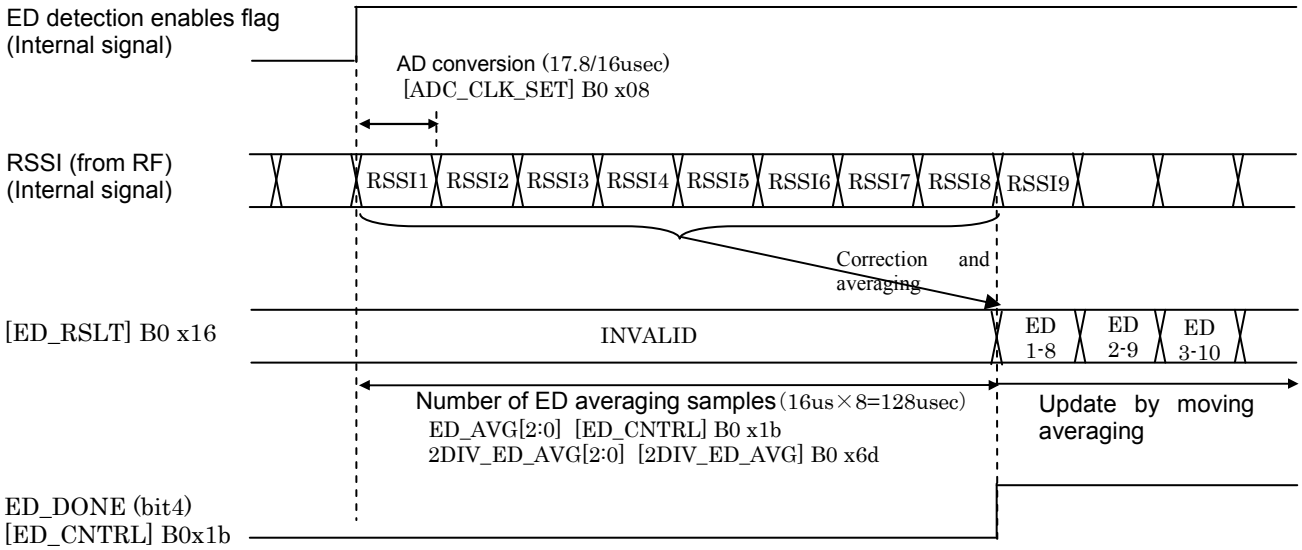
Time to compute ED value averaging process will be estimated by following equations.

ED value averaging process time = AD conversion period (17.7us/16us) * number of ED value averaging samples

#AD conversion period can be selectable by register AD clock frequency (BANK0, address 0x08 ： ADC_CK_SEL)

AD clock frequency = 1.8MHz：17.7us
2.0MHz：16us

[Time Chart]



●Diversity Function

TBD

TBD

TBD

TBD

●CCA (Clear Channel Assessment) Function

This LSI has CCA function that will check availability of certain channel. 3 type of modes are available, normal mode, continuous mode, IDLE detection mode.

[CCA mode setting]

	[CCA_CNTRL] (B0, 0x15)	
	Bit3 (CCA_EN)	Bit5 (CCA_LOOP_START)
Normal mode	0b1	0b0
Continuous mode	0b1	0b1

	[CCA_CNTRL] (B0, 0x15)	[AUTO_ACK_SET] (B0, 0x55)
	Bit7 (CCA_AUTO_EN)	Bit4 (AUTO_ACK_EN)
IDLE detection mode	0b1	0b1

○Normal mode

Normal mode determine IDLE or BUSY. CCA (normal mode will be executed if receiver is activated by RX_ON while CCA_ENbit=0b1 and CCA_LOOP_START bit=0b0.

The judgement of CCA is determined by comparison between ED value and threshold value defined by [CCA_LEVEL] (B0, 0x13). If ED value exceed CCA threshold, it is determined as BUSY, set [CCA_CNTRL] CCA_RSLT[1:0] (bit1, 0) to 0b01. If ED value is smaller than CCA threshold, and it is maintained for time period by [IDLE_WAIT_L], [IDLE_WAIT_H] (B0, 0x17 and 0x18), it is determined as IDLE. CCA_RSLT[1:0] will be set to 0b00.

CCA complete interrupt will be taken place when BUSY or IDLE state is detected. [CCA_CNTRL] register CCA_DONE bit (bit2) will become 0b1 at same time. CCA_EN bit will be automatically cleared to 0b0

When CCA completion interrupt is cleared, CCA_RSLT[1:0] is initialized (0b00). CCA_RSLT[1:0] need to be read before clearing CCA completion interrupt.

If the ED value exceeds the value set by [CCA_INGNORE_LEVEL] register (B0 0x12), IDLE judgment is not made when the target ED value is contained in the averaging target. At this time, when the average ED value is more than CCA_LEVEL, CCA completes with BUSY judgment. However, the average ED value is less than CCA_LEVEL, CCA_RSLT[1:0] is set to 0b11 without IDLE judgment, and CCA continues until BUSY state is detected or the target ED value is out of the averaging target and IDLE state is detected. For detail behavior when the ED value exceeds CCA_INGNORE_LEVEL, refer to "Excluding IDLE judgment by strong input".

Time from the CCA execution instruction to the CCA completion is calculated as the following equations.

[When IDLE state is detected]

CCA execution time = (number of averaged ED values + IDLE_WAIT setting) x A/D conversion period + period to stabilize the filter (A/D conversion period x 2)

[When BUSY state is detected]

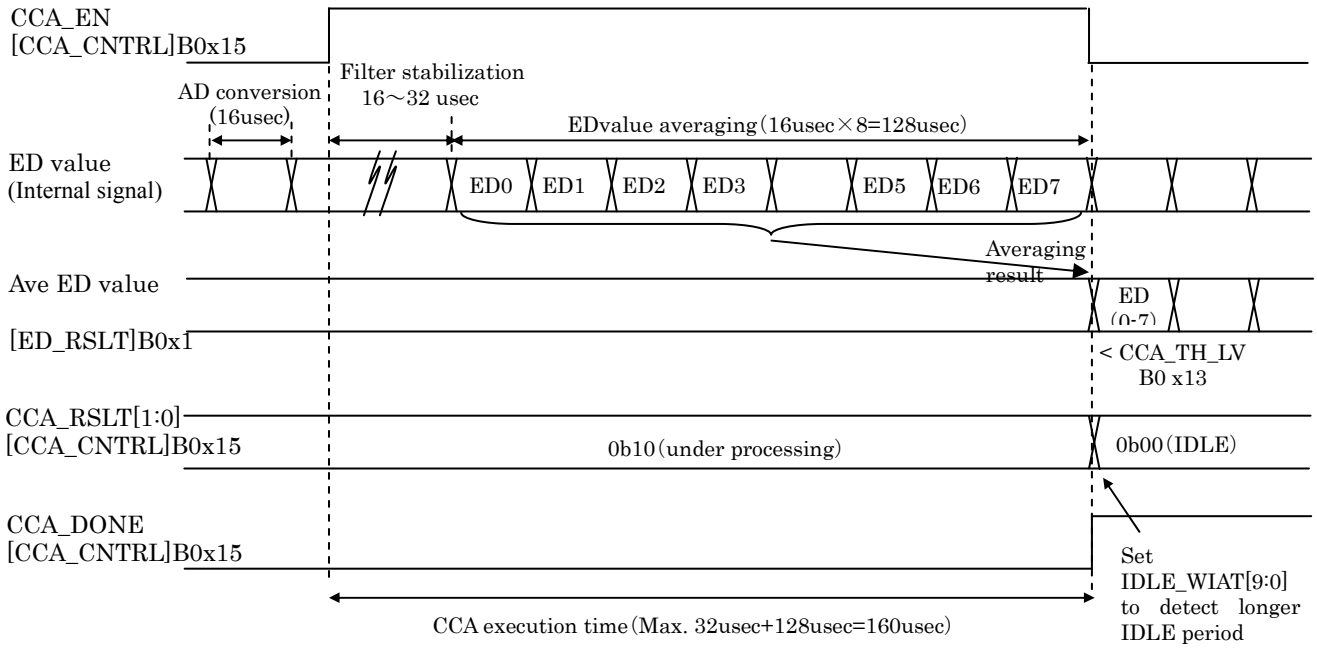
CCA execution time = number of averaged ED values x A/D conversion period + period to stabilize the filter (A/D conversion period x 2)

* The above equations do not consider IDLE judgment excluded by CCA_INGNORE_LEVEL.For details of CCA_INGNORE_LEVEL operation, see ″ Excluding IDLE judgment by strong input ″.
* A/D conversion period can be switched by using [ADC_CLK_SET] register (B0 0x08) bit4 (ADC_CLK_SET).
  ADC_CLK_SET=0b0: 17.8us , 0b1: 16us

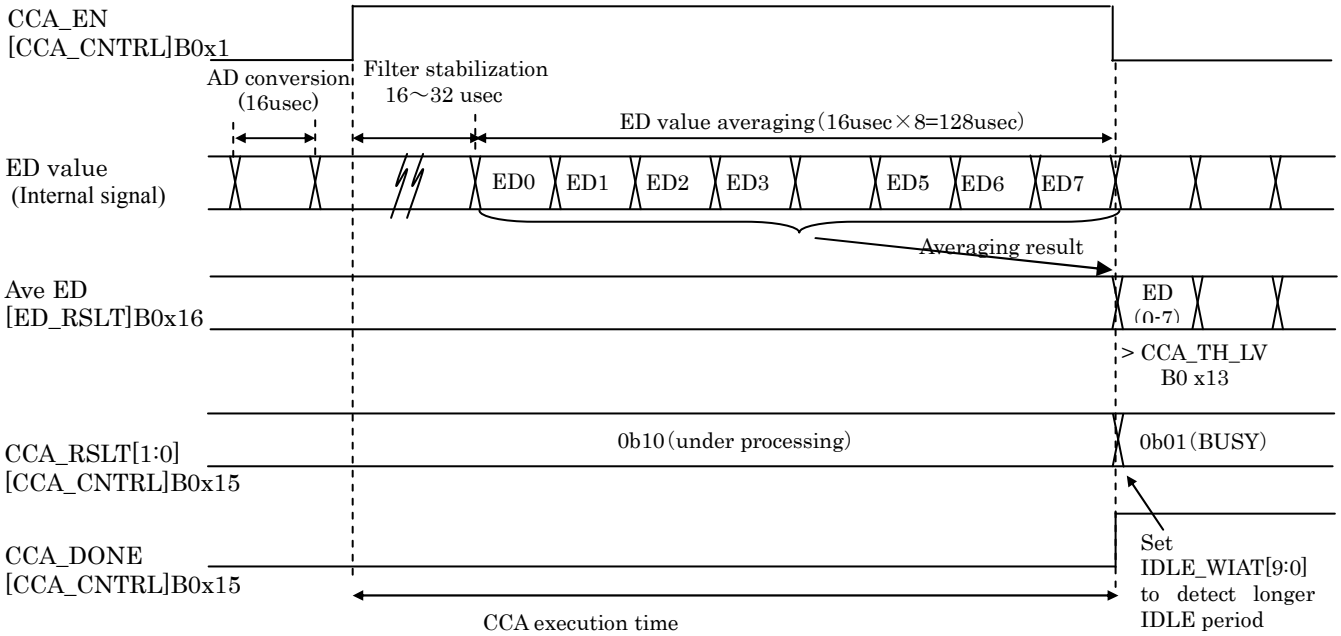
Timing chart of CCA normal mode is shown below.

[Conditions]
ADC_CK_SEL=0b1 (2MHz) [ADC_CLK_SET] (B0x08)
ED_AVG[2:0]=0b011 (averaging 8samples) [ED_CNTRL] (B0x1b)
IDLE_WAIT[9:0]=0b00_0000_0000 (IDLE detection period 0uS) [IDLE_WAIT_L], [IDLE_WAIT_H](B0x17,x18)

[IDLE judged case]



[Judged as BUSY]



○Continuous mode

In continuous mode, CCA operation will be repeated until HOST CPU stop its operation. It will be executed by RX_ON while CCA_EN bit=0b1, CCA_LOOP_START bit=0b1.

Similar to normal mode, ED value will be compared with threshold value defined by [CCA_LEVEL] register (B0, 0x13). If ED value exceed CCA threshold, it is determined as BUSY, set [CCA_CNTRL] CCA_RSLT[1:0] (bit1, 0) to 0b01. If ED value is smaller than CCA threshold, and it is maintained for time period by [IDLE_WAIT_L], [IDLE_WAIT_H] (B0, 0x17 and 0x18), it is determined as IDLE. CCA_RSLT[1:0] will be set to 0b00. IDLE_WAIT[9:0]For detail behavior of IDLE_WAIT[9:0], refer to "Long IDLE detection".

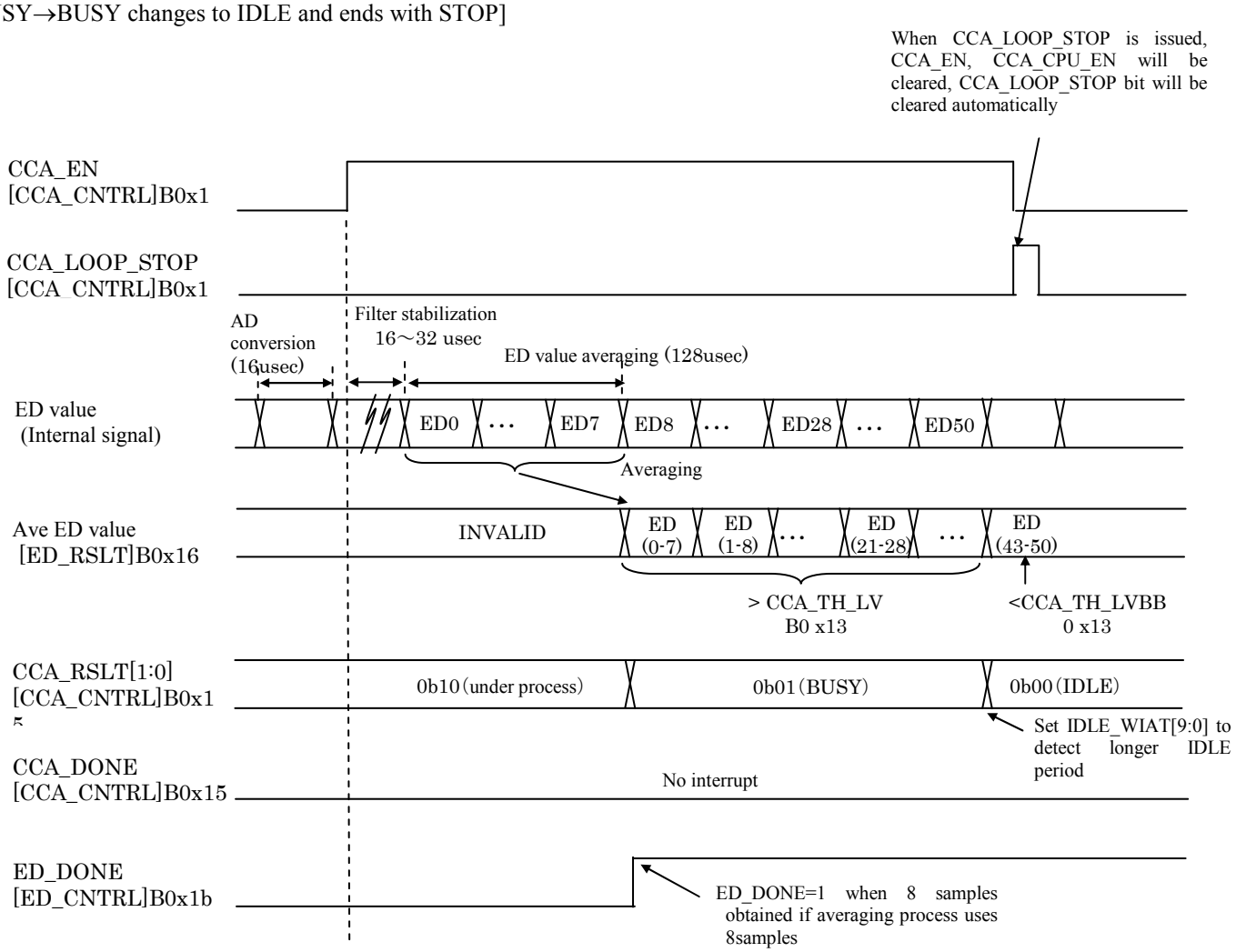
If the ED value exceeds the value set by [CCA_INGNORE_LEVEL] register (B0 0x12), IDLE judgment is not made when the target ED value is contained in the averaging target. At this moment, the average ED value is more than CCA_LEVEL, CCA_RSLT[1:0] is set to 0b01 with BUSY judgment. However, the average ED value is less than CCA_LEVEL, CCA_RSLT[1:0] is set to 0b11 without IDLE judgment. For detail behavior when the ED value exceeds CCA_INGNORE_LEVEL, refer to "Excluding IDLE judgment when strong input occurs".

In continuous mode, CCA operation will not be stopped when BUSY or IDLE status is determined, it will be repeated until register [CCA_CNTRL] CCA_LOOP_STOP bit(bit6) become 0b1. Comparison will be performed each time when new ED value is obtained. CCA_DONE bit (bit2) will not be 0b1, no interrupt will be asserted.

Time chart of CCA continuous mode is shown below.

[Conditions]
ADC_CK_SEL=0b1 (2MHz) [ADC_CLK_SET] (B0x08)
ED_AVG[2:0]=0b011 (Averaging samples) [ED_CNTRL] (B0x1b)
IDLE_WAIT[9:0]=0b00_0000_0000 (IDLE detection period 0uS)[IDLE_WAIT_L], [IDLE_WAIT_H] (B0x17,x18)

[BUSY→BUSY changes to IDLE and ends with STOP]



[Note]
•CCA induces an internal no input state. The no input state is released after filter stabilization.
・When no input changes to a -80dBm input, it takes about 32us for the ED value to be shown as -80dBm.

○IDLE detection mode

TBD

T.B.D.

○Excluding IDLE judgment by strong input

T.B.D.

○IDLE detection spent long time

T.B.D.

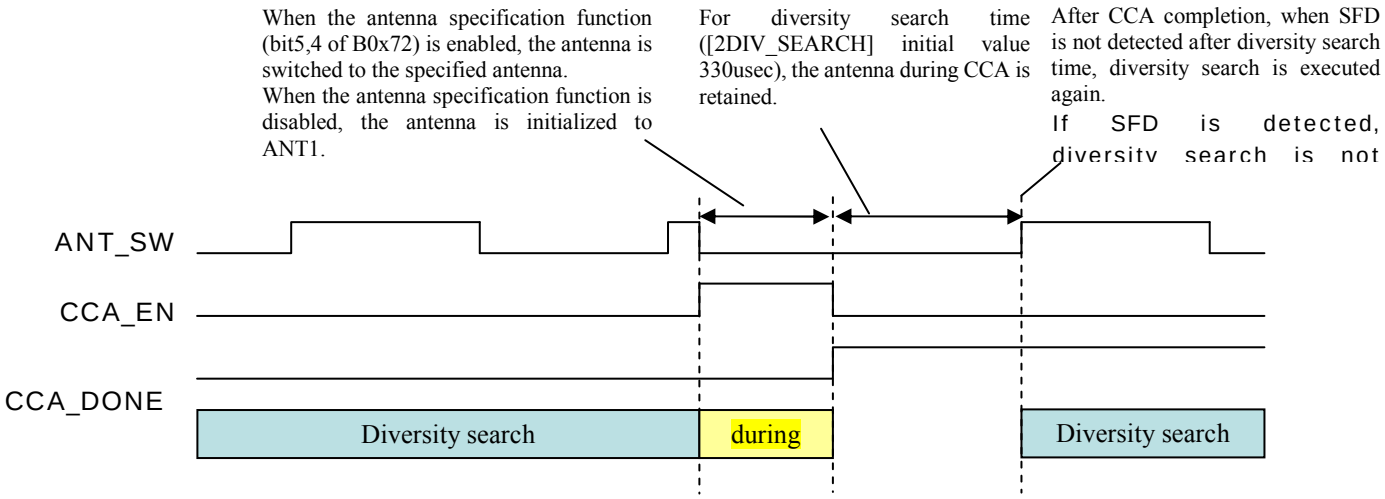
T.B.D.

○CCA execution with diversity

(1)CCA execution during diversity search

When CCA execution is instructed during diversity search, the diversity search stops, and CCA operates.
When CCA operates, the antenna is fixed to the initial value (*1) to be retained until next diversity search. However, when the antenna specification function (bit5-4 of [2DIV_RSLT] register (B0 0x72)) is enabled, the antenna is fixed to the one specified with this register function to be retained until next diversity search.
After CCA completion, when SFD is not detected after the diversity search time set by using bit6-0 of [2DIV_SEARCH] register (B0 0x6f (default approx. 330usec), diversity search is executed again. When SFD is detected during CCA or after completion of CCA, diversity search is not executed.

* 1： Upper setting in the "At reception" column on each table of "Function Description Diversity Function ANT_SW/TRX_SW".

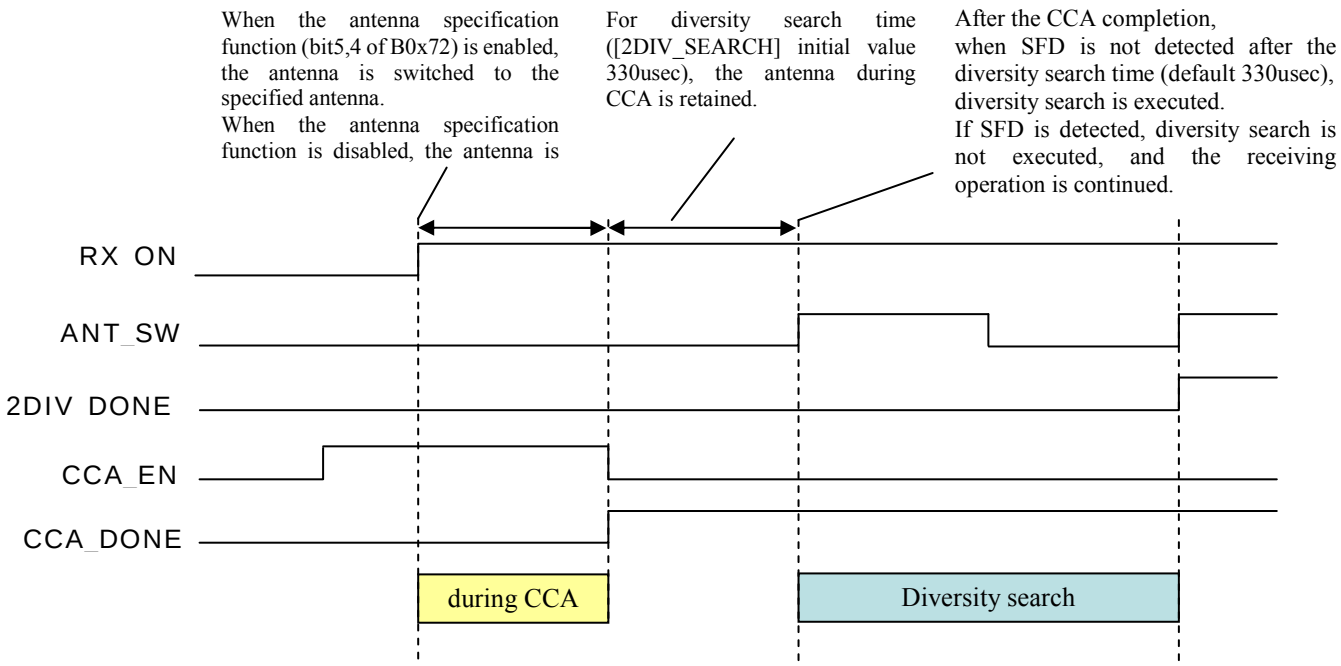


[Note]
When CCA is executed during diversity search, set the timeout for waiting for the CAA completion interrupt. If the diversity search completion and the CCA execution occur at the same time, CCA completion interruption may not be notified. If timeout occurs, the CCA result (bit1-0 (CCA_RSLT) of [CCA_CNTRL] register (B0 0x15)) stores the latest result. When you want to execute CCA again, issue CCA_LOOP_STOP (bit6 of [CCA_CNTRL] register(B0 0x15)) first.
See the CCA execution time in "Normal Mode" to determine an adequate period for timeout.
For details of the CCA execution flow when using diversity, see the flow chart of "CCA during diversity".
Receive operations are parallel during CCA. Even if CCA_DONE is not notified, an SFD detection interruption (bit3 of INT_SOURCE_GRP2), received FIFO access error interruption (bit6 of INT_SOURCE_GRP2), FIFO-Full trigger interruption (bit3-2 of INT_SOURCE_GRP1), reception completion interruption (bit3-2 of INT_SOURCE_GRP3), or CRC detection error interruption (bit 5-4 of INT_SOURCE_GRP3) may be notified.

For details of the diversity function, see "Diversity Function".

(2) CCA set to be executed before RX_ON with diversity ON

When diversity ON and CCA execution are set before RX_ON, CCA operates without diversity search operation after RX_ON.
After CCA completion, when SFD is not detected after the diversity search time set by using bit6-0 of [2DIV_SEARCH] register (B0 0x6f (default approx. 330usec), diversity search is executed. When SFD is detected during CCA or after completion of CCA, diversity search is not executed.



○How to set CCA threshold

The CCA threshold ([CCA_LEVEL]B0 0x13) must be set to the ED value corresponding to the input level to be detected, considering device variations, temperature variations, and loss on the antenna or matching circuit. The relationship between the input level and the ED value is expressed by the following equation.

ED value = 255/70 x (107 + input level [dBm])

Note that, when CCA is executed, the ED value is higher than normal because the BPF setting is changed. By considering this correction and above variation, set the CCA threshold as follows.

CCA threshold = 255/70 x (107 + input level [dBm] - variation - other loss) + correction for CCA

Parameter	Value
Variations (device and temperature)	6dB
Other loss	Loss on antenna, matching circuit and so on
Correction for CCA	12@100kbps, 15@200kbps, 0@other rates

Example: To set the input level threshold to -75dBm
Condition: Other loss 1dB, 100kbps

CCA threshold = 255/70 x (107 - 75 - 6 - 1) + 12
≅ 103
= 0x67

You can verify whether the CCA threshold is adequate or not by executing CCA for each input level to check the level where state changes from IDLE to BUSY.

●SFD detection

This LSI has Frame synchronization pattern detection function. Up to 2 pattern of SFD sequence can be stored in registers. It supports “MRFSKFSD” of IEEE 802.15.4g standard and SFD pattern that is valiable by condition of FEC scheme.
Please refer to IEEE 802.15.4g standard for more details

In IEEE802.15.4g standard, SFD group which is defined by phyMRFSKSFD and SFD which is determined by condition of FEC scheme (coded, uncoded). This LSI has registers corresponding each conditions.

(1) TX mode

SFD pattern in TX mode will be defined by register MRFSKSFD(bit6) and FEC_EN(PHYSET52 0x46 bit6).

①SFD length shorter than or equal to 2 bytes

FEC_EN	MRFSKSFD	
	0	1
0	SFD_PAT[15:0]	SFD_PAT2[15:0]
1	SFD_PAT[31:16]	SFD_PAT2[31:16]

②SFD length longer than 3 bytes

FEC_EN	MRFSKSFD	
	0	1
0/1	SFD_PAT[31:0]	SFD_PAT2[31:0]

(2) RX mode

If SFD length is shorter than or equal to 2 bytes and FEC_EN=1, matching 2 pattern either coded or uncoded will be used. Perform FEC process if SFD pattern matching is succeeded. Otherwise uncoded pattern of SFD code will be used, and process following to SFD will be performed.

①SFD length shorter than or equal to 2bytes

FEC_EN	MRFSKSFD	SFD pattern		SFD detect	Process following to SFD
		uncoded	coded		
1	0	SFD_PAT[15:0]	SFD_PAT[31:16]	Uncoded or coded	Perform FEC if pattern match with coded pattern, otherwise detemined as uncoded
1	1	SFD_PAT2[15:0]	SFD_PAT2[31:16]	Uncoded or coded	Perform FEC if pattern match with coded pattern, otherwise determined as uncoded
0	0	SFD_PAT[15:0]	-	Uncoded	Determined as uncoded
0	1	SFD_PAT2[15:0]	-	Uncoded	Determined as uncoded

②SFD length longer than 3bytes

FEC_EN	MRFSKSFD	SFD pattern		SFD detect	Process following to SFD
		uncoded	Coded		
1	0	SFD_PAT[31:0]	-	Uncoded	Determined as uncoded
1	1	SFD_PAT2[31:0]	-	Uncoded	Determined as uncoded
0	0	SFD_PAT[31:0]	-	Uncoded	Determined as uncoded
0	1	SFD_PAT2[31:0]	-	Uncoded	Determined as uncoded

In case of IEEE 802.15.4g (2bytes SFD), recommended configuration will be as follows..

Symbol	Address:	Value in register
SFD1_SET1	0x3a	0x09
SFD1_SET2	0x3b	0x72
SFD1_SET3	0x3c	0xF6
SFD1_SET4	0x3d	0x72
SFD2_SET1	0x3e	0x5E
SFD2_SET2	0x3f	0x70
SFD2_SET3	0x40	0xC6
SFD2_SET4	0x41	0xB4

●AUTO_ACK Function

In Packet transmission and reception, AUTO_ACK function is assisting function to help upper layer stack to transmit acknowledge packet automatically. Followings are detail of the AUTO_ACK function.

*Ack transmission (MCU request ACK transmission)
1) Analyze Frame Control field in received data, if Ack request bit is set to 0b1, then obtain Sequence Number from received data.

2) After RX completed, perform CRC check and if FCS is OK, then move to Ack packet transmission preparation state (enable TX_ON). (Here, RX complete interrupt will take place)

3) When TX_ON is enabled, wait until Ack transmission preparation complete interrupt. And wait for Ack transmission request.

4) MCU analyze Address field and Pending data in received data, and it decide to require Ack packet to send, [AUTO_ACK_SET] register (B0, 0x55) bit1(ACK_SEND) will become 0b1, issue Ack transmission request.
(Note) if there is a Pending data, the Frame Pending bit of Frame Control Field is set to 0b1 before Ack transmit enabled instruction is issued.

5) Ack packet transmission start
Frame Control Field in Ack packet uses data from registers [ACK_FRAME1] and [ACK_FRAME2] (B0, 0x53 and 0x54). It attaches Sequence Number obtained from received data.

6) After Ack packet transmitted, TX complete interrupt will be issued.
(Note) As RF status remains TX_ON, it is required to configure [RF_STATUS] register (B0, 0x6c) bit[3:0] (SET_TRX) 0b1000 (TRX_OFF) to return to IDLE status.

*Ack transmission (MCU request stop ACK transmission)
1) Analyze Frame Control field in received data, if Ack request bit is set to 0b1, then obtain Sequence Number from received data.

2) After RX completed, perform CRC check and if FCS is OK, then move to Ack packet transmission preparation state (enable TX_ON). (Here, RX complete interrupt will take place)

3) When TX_ON is enabled, wait until Ack transmission preparation complete interrupt. And wait for Ack transmission request.

4) MCU analyze Address field and Pending data in received data, and it decide not to require Ack packet to send, [AUTO_ACK_SET] register (B0, 0x55) bit0(ACK_STOPB) will become 0b1, issue Ack transmission stop request.

5) This LSI remove Ack packet, set RF status to TRX_OFF.

[Note]
1. When using AutoAck function, set bit6 (FEC_EN) of [FEC/CRC_SET] register (B0 0x46) to 0b0 (FEC disable) before transmitting Ack packets. When Ack packets are transmitted without AutoAck, FEC function becomes enabled.
2. Before reading received data from FIFO to receive Ack request packets, check the CRC bit information in the received Length via MCU, and set CRC mode with bit3 (CRC_EN), bit2-1 (CRC_MODE), and bit0 (CRC_DONE) of [FEC/CRC_SET] register (B0 0x46).

*Ack Transmission (Timer ACK transmission):
Condition） [ACK_TIMER_EN] register bit0 (AUTO_TIMER_EN)=0b1.

1）Analyze Frame Control field in received data, if Ack request bit is set to 0b1, then obtain Sequence Number from received data.

2）After RX completed, perform CRC check and if FCS is OK, then move to Ack packet transmission preparation state (enable TX_ON). (Here, RX complete interrupt will take place)

3） When TX_ON is enabled, Ack timer start counting, Ack transmission preparation complete interrupt take place, wait for Ack transmission request.

4）When time period defined by registers [ACK_TIMER_L] and [ACK_TIMER_H] (B0, 0x50 and 0x51) is expired, Ack packet transmission will be started.

5） After Ack packet has been transmitted, issue TX complete interrupt.
(Note) As RF status remains TX_ON, it is required to configure [RF_STATUS] register (B0, 0x6c) bit[3:0] (SET_TRX) 0b1000 (TRX_OFF) to return to IDLE status.

[Additional Function]
・There is function to perform CCA automatically after data received.

*Ack Reception
Condition） Register [AUTO_ACK_SET] (B0 0x55) bit6 (AUTO_RX_EN)=0b1.

1）After compete transmission of data packet with Ack request, TX complete interrupt will be issued. And set RX_ON enable, wait for Ack packet to receive.

2）When Ack packet is received, RX complete interrupt will be issued.
(Note) As RF status remains RX_ON, it is required to configure [RF_STATUS] register (B0, x6c) bit[3:0] (SET_TRX) 0b1000 (TRX_OFF) to return to IDLE status.

*Ack Reception (Stop waiting Ack packet)
Condition） Register [AUTO_ACK_SET] (B0 0x55) bit6 (AUTO_RX_EN)=0b1.

1）After compete transmission of data packet with Ack request, TX complete interrupt will be issued. And set RX_ON enable, wait for Ack packet to receive.

2）Issue Stop request by [AUTO_ACK_SET] register (B0, 0x55) bit0 (ACK_STOP)=0b1

3) It stops waiting Ack packet, set RF status to TRX_OFF.

●Address Filtering Function:

This function analyze data field highlighted as yellow in the MAC header (IEEE802.15.4) part of RX packets, to receive packets only matched to register set [PANID] to [SHT_ADDR1_1] (B2, 0x61 to 0x6E). It is possible to compare address such as PANID, 64bit Address, 16bit short address or IGB bits.

Byte：2	1	0 / 2	0/2/8	0 / 2	0/2/8	variable	2
Frame Control	Sequence Number	Destination PAN identifier	Destination Address	Source PAN identifier	Source address	Frame payload	Frame Chack sequence
		Addressing fields					
MAC header						MAC payload	MAC footer

Bits：0-2	3	4	5	6	7-9	10-11	12-13	14-15
Frame type	Security enabled	Frame pending	Ack. req.	PAN-ID Compression	Reserved	Dest. addressing mode	Frame Version	Source addressing mode

Fig. MAC header and Frame Control Field

Destination Addressing Mode：（Indicates address mode of destination device）

00 : Indicates Beacon or Ack Packet（Receive Beacon, Ack packet can be refused）
01 : Reserved（Does not receive）
10 : Data RX in 16 bits address
11 : Data RX in 64 bits address

Destination.PAN-ID：（Indicates PAN-ID which destination device is belonging）

0xFFFF : Indicate broadcasting, receive this packet regardless to address mode.
16 bits address mode : Receive packet only if same PAN-ID which is currently belonging (specified by register) is indicated.
64 bits address mode : This section is not referred.
#PAN-IDEN has to be enabled.

Destination Address：（Indicates desitination device address）

16 bit address mode: Receive packet only if current device address is indicated
64 bit address mode: Receive packet only if current device address is indicated or multicast transmission (I/G bit is 1)
IGB_EN, EXT_ADDEN, SHT_ADDEN0, SHT_ADDEN1 can be used.

It is possible to refuse Ack packet by register [AUTO_ACK_SET] (B0,0x55) bit7 (RX_ACK_CANCEL) and bit6 (AUTO_RX_EN) by following function table shown below.
This function sill be available only with Address Filtering Function is ON (one of [ADDFIL_CNTRL] (B2,0x60) bit4-0 is set to 0b1)

[AUTO_ACK_SET] B0, 0x55		Operation
Bit7 (RX_ACK_CANCEL)	Bit6 (AUTO_RX_EN)	
0b1	0b1	Receive first packet only ACK request bit is transmitted.
0b1	0b0	Remove all received ACK packets.
0b0	any	Receive all ACK packets.

It is possible to configure following procedure when received packet does not matched to expecting address by register [PACKET_MODE_SET] (B0, 0x45) bit5 (ADDFIL_NG_SET) and when it will be performed by bit0 (ADDFIL_IDLE_DET)

bit5 : (ADDFIL_NG_SET)

1 : When NG detected, data will be removed after data receptrion completetd.

0 : When NG detected, data will be removed immediately.

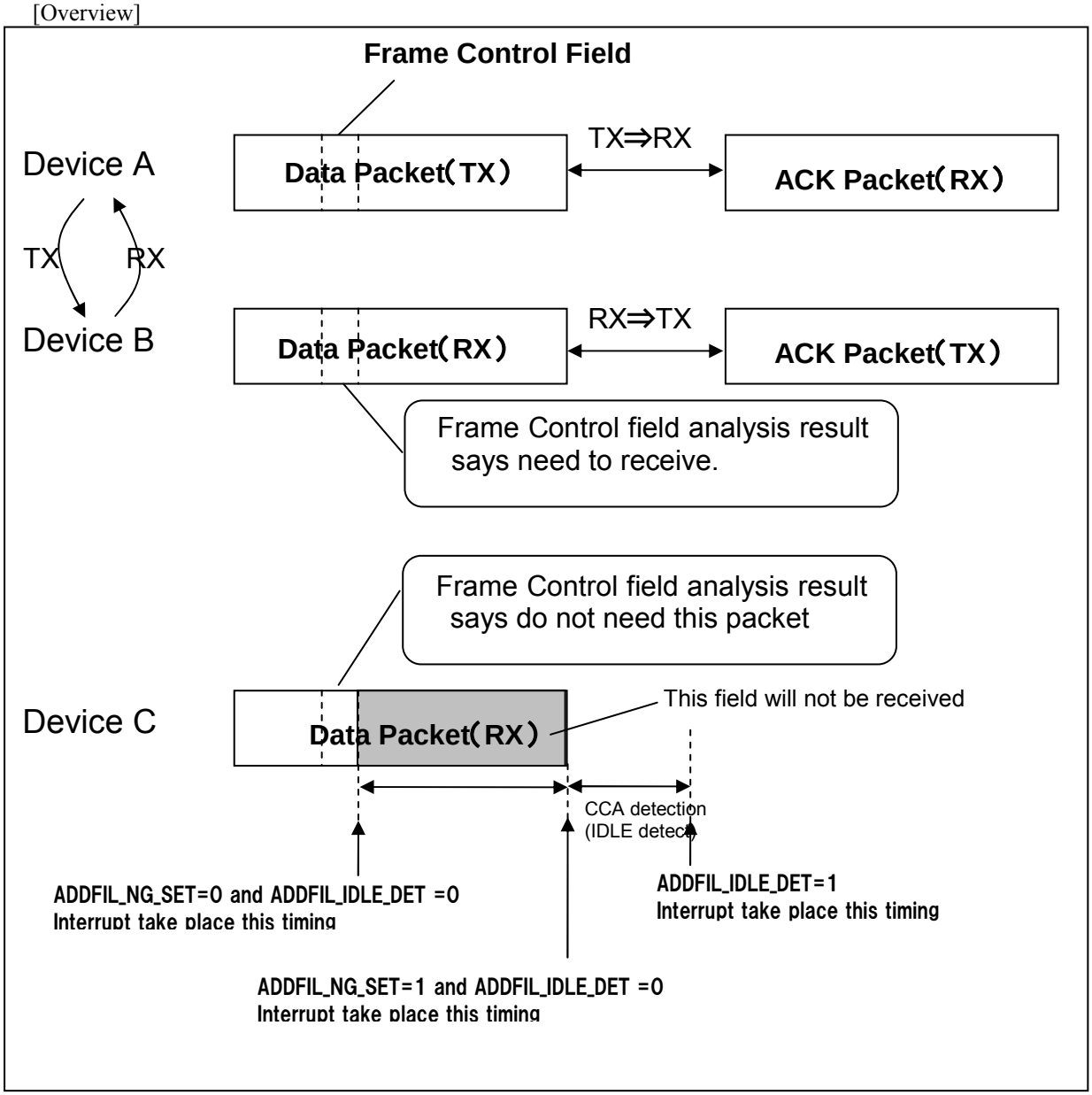
bit0 : (ADDFIL_IDLE_DET)

1 : After data removal, perform CCA and interrupt report when IDLE state is detected.

0 : After data removval, interrupt report immediately.

When data is removd, packet destroyed interrupt will be issued by address filtering function. The number of destroyed packets can be counted by [DISCARD_COUNT0] and [DISCARD_COUNT1] registers (B2, 0x6f and 0x70). Can be counted up to 1023 packets.

[Overview]



Interrupt generation timing with timing control function for interrupt notification (address filter destroy interrupt ([INT_SOURCE_GRP1] register INT[3]) and CRC error interrupt ([INT_SOURCE_GRP3] register INT[20]/INT[21]))

Interrupt generation timings of address filter destroy interrupt and CRC error interrupt are changed by the interrupt notification timing control bits. Generation timings of address filter destroy interrupt①, CRC error interrupt②, and CCA completion interrupt③ for each case are as follows.

			Setting 1		Setting 2		Setting 3		Setting 4	
	Setting	setting register	Case1	Case2	Case3	Case4	Case5	Case6	Case7	Case8
Input	Destroy after address mismatch	[PACKET_MODE_SET] (B0 0x45) bit5=0b0	○	○	–	–	○	○	–	–
	Hold after address mismatch until packet expiration	[PACKET_MODE_SET](B0 0x45) Bit5=0b 1	–	–	○	○	–	–	○	○
	Run CCA after address mismatch	[PACKET_MODE_SET](B0 0x45) bit5=0b 1	–	–	–	–	○	○	○	○
	CRC_OK	–	○	–	○	–	○	–	○	–
	CRC_NG	–	–	○	–	○	–	○	–	○
result	Address filter destroy interrupt	[INT_SOURCE_GRP1] INT[3]	①	①	①	①	①	①	①	①
	CRC error detection interrupt	[INT_SOURCE_GRP3] INT[21/20], [INT_SOURCE_GRP1] INT[7:6]	②	②	–	②	②	②	–	②
	CCA detection completion interrupt	[INT_SOURCE_GRP1] INT[8]	–	–	–	–	③	③	③	③

(1)INT_TIM_CTRL = 0

		PHY HDR	MAC HDR	DATA	CCA (IDLE detection	
Setting 1	Case1		①②			①⇒②:1111ns
	Case2		①②			①⇒②:1111ns
Setting 2	Case3			①		
	Case4			①②		① and ② at same time
Setting 3	Case5		②		③①	③⇒①:555ns
	Case6		②		③①	③⇒①:555ns
Setting 4	Case7				③①	③⇒①:555ns
	Case8			②	③①	③⇒①:555ns

(2)INT_TIM_CTRL = 1

		PHY HDR	MAC HDR	DATA	CCA (IDLE detection	
Setting 1	Case1		①			①⇒②:1111ns
	Case2		①			①⇒②:1111ns
Setting 2	Case3			①		
	Case4			①②		① and ② at same time
Setting 3	Case5			①	③	
	Case6			①	③	
Setting 4	Case7			①	③	
	Case8			①②	③	

●Interrupts

Several intterupts functions are supported to inform internal status of This LSI. When one of interrupt taken placed, SINTN (#10 pin) will become Low.
Interrupt source can be segmented to 4groups by registers [INT_SOURCE_GRP1] to [INT_SOURCE_GRP4] (B0, 0x24-0,˜27).
Each interrupts have capability to disable by mask bits.

○Interrupt sources

Group	Name	Function:
GRP4	INT[25]	PLL unlock detection
	INT[24]	Auto_Ack preparation complete
GRP3	INT[23]	FIFO1 data transmission requested
	INT[22]	FIFO0 data transmission requested
	INT[21]	FIFO1 data reception with CRC error
	INT[20]	FIFO0 data reception with CRC error
	INT[19]	FIFO1 data reception completed
	INT[18]	FIFO0 data reception completed
	INT[17]	FIFO1 data transmission completed
	INT[16]	FIFO0 data transmission completed
GRP2	INT[15]	TX FIFO access error
	INT[14]	RX FIFO access error
	INT[13]	TX Length error
	INT[12]	RX Length error
	INT[11]	SFD detection
	INT[10]	RF state transition completed
	INT[09]	Diversity detection completed
	INT[08]	CCA detection completed
GRP1	Reserved	Reserved
	Reserved	Reserved
	INT[05]	FIFO_FULL
	INT[04]	FOFO_EMPTY
	INT[03]	Address Filtering Function packet destroy completed
	INT[02]	VCO calbration completed
	INT[01]	Reserved
	INT[00]	CLK stabilization completed

○Interrupt generation timing

Here is the time from start point to interrupt generation or interrupt generation timing for each interrupt notification. See below for the timeout operation waiting for an interrupt notification.

[Note]

(1)The following table assumes 100kbps for numeric values. Replace the value described as "symbol time" with 20, 5, and 2.5 for 50kbps, 200kbps, and 400kbps, respectively.

(2)The following table assumes the following format of transmitted/received data for numeric values.

10 bytes	2bytes	2 bytes	24 bytes	2 bytes
Preamble	SFD	Length	User data	CRC

(3)Even when an interrupt notification is set to OFF, this LSI internally holds the interrupt. When the interrupt notification setting is then changed from OFF to ON without clearing the interrupt, it will be notified.

Interrupt notification		Starting point	Time from start point to interrupt generation or interrupt generation timing
INT[0]	CLK stabilization completion	RESETN released (Power-on)	660us
		SLEEP released (Returned to SLEEP)	660us
INT[1]			
INT[2]	VCO calibration End	VCO calibration started	230us
INT[3]	Address filtering function packet destroy completion	SFD detection	(1)If set to notify destroy immediately after the address filter is judged as NG When judged as NG (2)If set to notify destroy after the data receive is completed (With FEC disabled) 2245.55us((Length to CRC:bit) x 10(symbol time)=2240us, internal delay=5.55us) (With FEC enabled) 4795.55us(FEC decryption/internal delay=315.55us, (Length to CRC:bit) x 2 x 10(symbol time)=4480us)
INT[4]	FIFO-EMPTY	TX_ON instruction (Transmit) (* 1)	If empty trigger level is set to 0x02 (With FEC disabled) (Preamble to data 23 byte) x 10 (symbol time)=2960us (With FEC enabled) 5066us(RF starting/internal delay =106us, unencoded data length ((preamble to SFD)=960us), encoded data length ((Length to data 23 bytes) x 2 x 10(symbol time)=4000us))
		-(Receive)	When remaining amount of FIFO exceeds the trigger level by FIFO read
INT[5]	FIFO-FULL	-(Transmit)	When remaining amount of FIFO exceeds the trigger level by FIFO write
		SFD detection (reception)	If full trigger level is set to 0x05 (With FEC disabled) 640us((Length2 bytes + data 6 bytes) x 10us(symbol time)) (With FEC enabled) 1585us(FEC decryption/internal delay=305us, encoded data length (Length2 bytes + data 6 bytes) x 2 x 10(symbol time)=1280us)
INT[6]			
INT[7]			
INT[8]	CCA detection completion	Start CCA	(1)Normal mode (Number of averaged ED values + CCA_IDLE_SET setting + 2) x A/D conversion period (2) IDLE detection mode ○When IDLE state is detected (Number of averaged ED values + CCA_IDLE_SET setting + 2) x A/D conversion period ○When BUSY state is detected

			(Number of averaged ED values + 2) x A/D conversion period (*) A/D conversion period can be switched by using AD clock frequency (BANK0: 0x08: ADC_CK_SEL). AD clock frequency=1.8MHz: 17.7us , 2.0MHz: 16us [Note] When running CCA during diversity, set the abort timer for CCA detection completion notification. When CCA is run during diversity, CCA detection notification completion is not notified fairly infrequently.
INT[9]	Diversity detection completion	-	When the diversity search is completed
INT[10]	RF state transition completion	TX_ON instruction	(At IDLE) 122us (At reception) 89us
		RX_ON instruction	(At IDLE) 136us (At transmission) 142us
		TRX_OFF instruction	(At transmission) 410us (At reception) 11us
		Force_TRX_OFF Instruction	(At transmission) 410us (At reception) 10us
INT[11]	SFD detection	-	When SFD is detected
INT[12]	Receive length error	SFD detection	80us
INT[13]	Transmit length error	-	When transmitted data is written to FIFO
INT[14]	Receive FIFO access error	-	(1)When data is received without FIFO free space (2)When insufficient reading from FIFO causes overflow (3)When too much reading from FIFO causes underflow
INT[15]	Transmit FIFO access error	-	(1)When data is written without FIFO free space (2)When adding to FIFO causes overflow (3)When there is no data to transmit during transmission
INT[16/17]	FIFO0/FIFO1 data transmission completion	TX_ON instruction (* 1)	(With FEC disabled) 3354us(starting/internal delay=154us, (preamble to CRC:bit) x 10(symbol time)=3200us) (With FEC enabled) 5664us(RF starting/internal delay =224us, unencoded data length ((preamble to SFD:bit) x 10(symbol time)=960us), encoded data length ((Length to CRC:bit) x 2 x 10(symbol time)=4480us)
INT[18/18]	FIFO0/FIFO1 data reception completion	SFD detection	(With FEC disabled) 2245us((Length to CRC:bit) x 10(symbol time)=2240, internal delay=5us) (With FEC enabled) 4795us(FEC decryption/internal delay=315us, (Length to CRC:bit) x 2 x 10(symbol time)=4480us)
INT[20/21]	FIFO0/FIFO1CRC error detection	SFD detection	(With FEC disabled) 2245us((Length to CRC:bit) x 10(symbol time)=2240, internal delay=5us) (With FEC enabled) 4795us(FEC decryption/internal delay=315us, (Length to CRC:bit) x 2 x 10(symbol time)=4480us)
INT[22/23]	FIFO0/FIFO1 data transmit request acceptance completion	-	When a Length of data is completely written to FIFO (It is during the transmitting when data is added by using FIFO trigger)
INT[24]	AutoAck preparation completion	Transmission completed	92us
INT[25]	PLL unlock	-	(At transmission) During transmission after PA enable (At transmission) During reception after RX enable

(* 1) When TX_ON instruction is issued and transmitted after writing a Length of transmitted data to FIFO

○Interrupt clear condition

Interrupt notification		Requirements for clearing interrupt
INT[0]	CLK stabilization completion	After the interrupt occurs
INT[1]		
INT[2]	VCO calibration completion	After the interrupt occurs
INT[3]	Address filtering function packet destroy completion	After the interrupt occurs
INT[4]	FIFO-EMPTY	After the interrupt occurs (before the next EMPTY trigger generation timing)
INT[5]	FIFO-FULL	After the interrupt occurs (before the next FULL trigger generation timing)
INT[6]		
INT[7]		
INT[8]	CCA detection completion	After the interrupt occurs (clear before the next CCA execution) * Note that this also clears the CCA result.
INT[9]	Diversity detection completion	After the data receive completion notification (INT[18/19]), cleared with data receive completion notification interrupt * Cannot be cleared during data reception.
INT[10]	RF state transition completion	After the interrupt occurs
INT[11]	SFD detection	After the interrupt occurs
INT[12]	Receive length error	After the interrupt occurs
INT[13]	Transmit length error	After the interrupt occurs
INT[14]	Receive FIFO access error	After the interrupt occurs
INT[15]	Transmit FIFO access error	After the interrupt occurs (clear before the next packet transmission)
INT[16/17]	FIFO0/FIFO1 data transmission completion	After the interrupt occurs (clear before the next packet transmission)
INT[18/19]	FIFO0/FIFO1 data reception completion	After the interrupt occurs (clear before the next packet reception)
INT[20/21]	FIFO0/FIFO1CRC error detection	After the interrupt occurs * Note that this also clears the CRC result (CRC_RSLT1/0).
INT[22/23]	FIFO0/FIFO1 data transmit request Reception completed	After the data transmit completion notification (INT[16/17]) (clear before the next packet transmission) * Cannot be cleared during data transmission.
INT[24]	AutoAck preparation completion	After the interrupt occurs
INT[25]	PLL unlock	After the interrupt occurs (clear before the next packet transmission/reception)

●Temperature Measurement Function

This LSI has function that measure temperature information. It is possible to obtain as analog data from A_MON pin (#24 pin) or digital data from register [TEMP_MON] (B0, 0x78). It can be selected by register [RSSI/TEMP_OUT] (B1, 0x03).

[Note]
Register [RSSI/TEMP_OUT] (B1 0x03) bit4（TEMP_OUT） and bit5(TEMP_ADC_OUT) should not be 0b1at same time.

[Analog output]
This LSI has internal current source. The current will be drawn to 75kohm of load resistance to be attached to A_MON pin (#24pin). Temperature information can be taken from voltage level at load resistance.

Current draw will be 10uA in typical at 25deg.C. Temperature information can be converted from following equation.

Itemp = (273+ Temp) / (273+25) x 10 (uA)

Conversion equation between A_MON voltage (75kohm load resistance attached) and temprature will be as follows.

Vamon = (273+ Temp) / (275+25) x 10E-6 x 75000

If temprature is range between -40deg.C to +85deg.C, Vamon will be range of 0.59V to 0.9V. Therefore temperature can be obtained by following equation.

Temp = Vamon x 397.3 - 273

[Digital output]
In digital domain, 4samples of output from 6bits A/D converter are summed and it will be stored in the register [TEMP_MON] (B0, 0x78).
The register will be updated every 17.8uS (if [ADC_CLK_SET] (B0, 0x08) is configured to 2MHz, update time interval will be 16 uS)

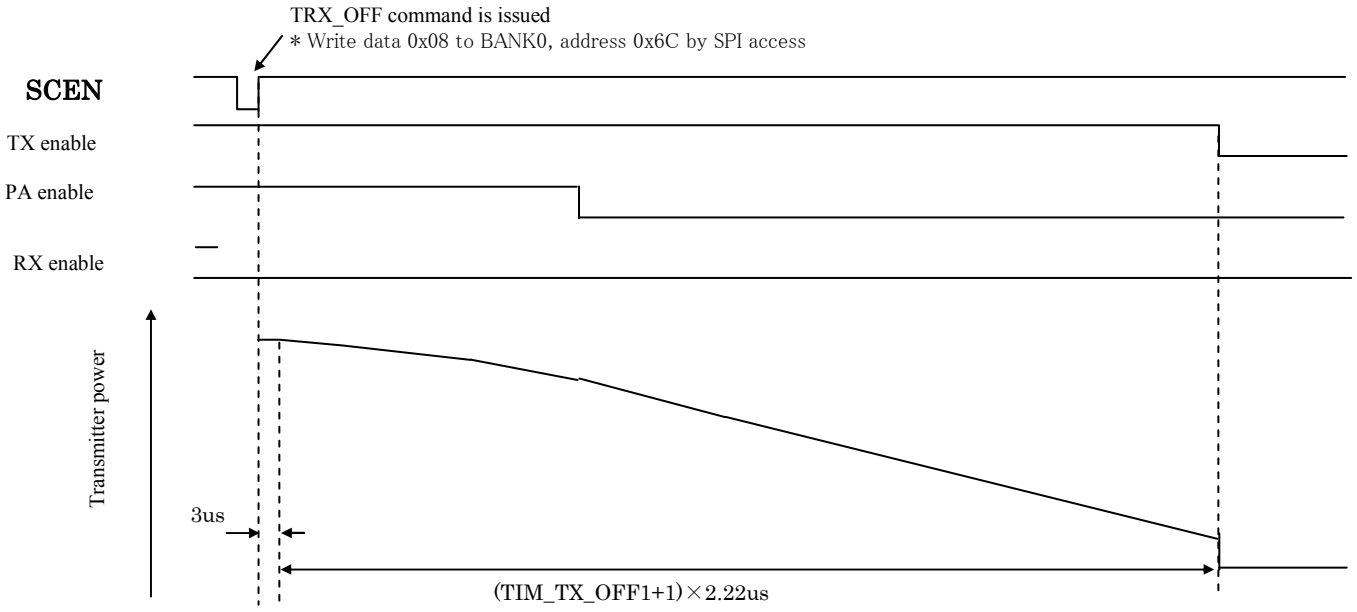
●Lamp control function

Lamp control function reduces spurious emission when transmission is stopped. There are two cases where transmission is stopped; switched to TRX_OFF and to reception. Both cases are supported by the lamp control function.

The following registers are used for lamp control.
[RAMP_CNTRL] register (B2 0x2c) bit4 (TXOFF_RAMP_EN)...Lamp control enable
[TX_OFF_ADD1] register (B1 0x55) bit7-0 (TIM_TX_OFF1)...TX_OFF timing control (to transition from TX to TRX_OFF)
[RX_ON_ADJ2] register (B1 0x3f) bit6-4 (TIM_RX_ON2) ...RX_ON timing control (to transition from TX to RX)
[GAIN_CONTRL] register (B0 0x6e) bit7-2 (TIM_TX_OFF2) ...TX_OFF timing control (to transition from TX to RX)

[Operation Overview]
(1)When switching from transmission to TRX_OFF (with lamp control enabled)

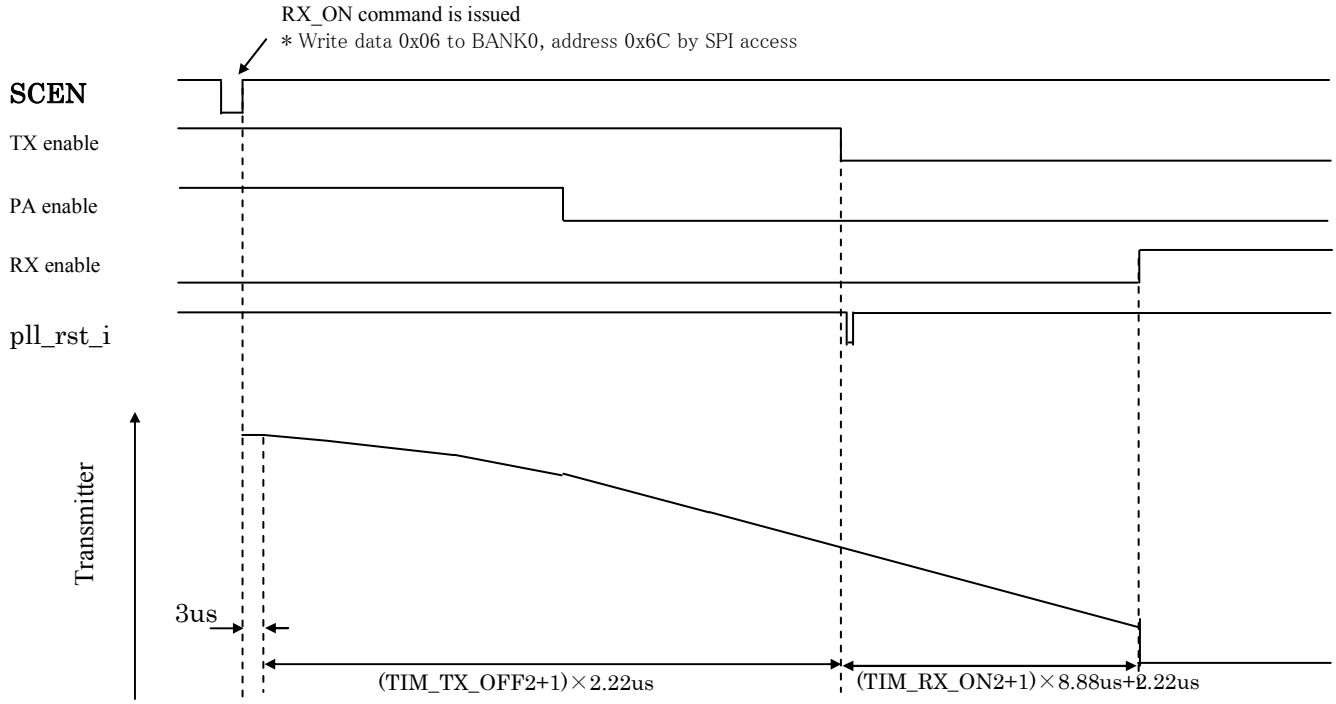
Register setting
[RAMP_CNTRL] register (B2 0x2c) bit4 (TXOFF_RAMP_EN) = 1
[TX_OFF_ADD1] register (B1 0x55) bit7-0 (TIM_TX_OFF1) = 0xb4(400us setting), 0x42 (150us setting)
[RX_ON_ADJ2] register (B1 0x3f) bit6-4 (TIM_RX_ON2) = 0x3
[GAIN_CONTRL] register(B0 0x6e) bit7-2 (TIM_TX_OFF2) = 0x2D



(2)When switching from transmission to reception (with lamp control enabled)

Register setting

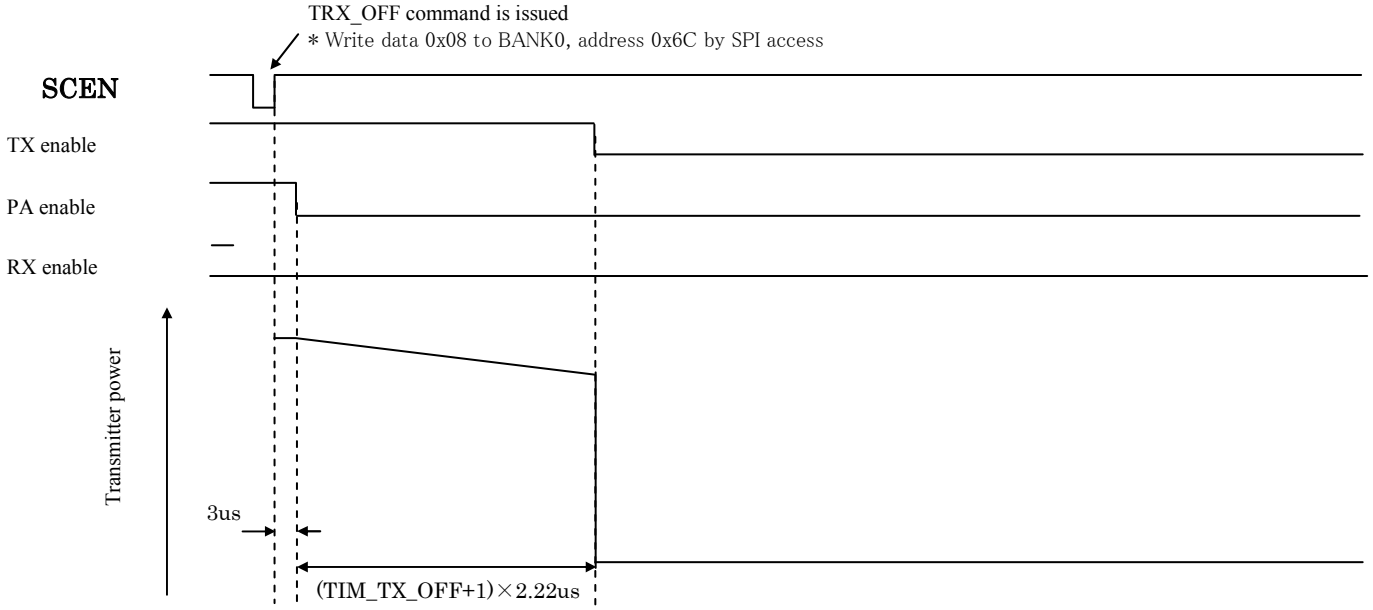
[RAMP_CNTRL] register (B2 0x2c) bit4 (TXOFF_RAMP_EN) = 1
[TX_OFF_ADD1] register (B1 0x55) bit7-0 (TIM_TX_OFF1) = 0xb4
[RX_ON_ADJ2] register (B1 0x3f) bit6-4 (TIM_RX_ON2) = 0x3
[GAIN_CONTRL] register (B0 0x6e) bit7-2 (TIM_TX_OFF2) = 0x2D



(3)When switching from transmission to TRX_OFF (with lamp control disabled)

Register setting

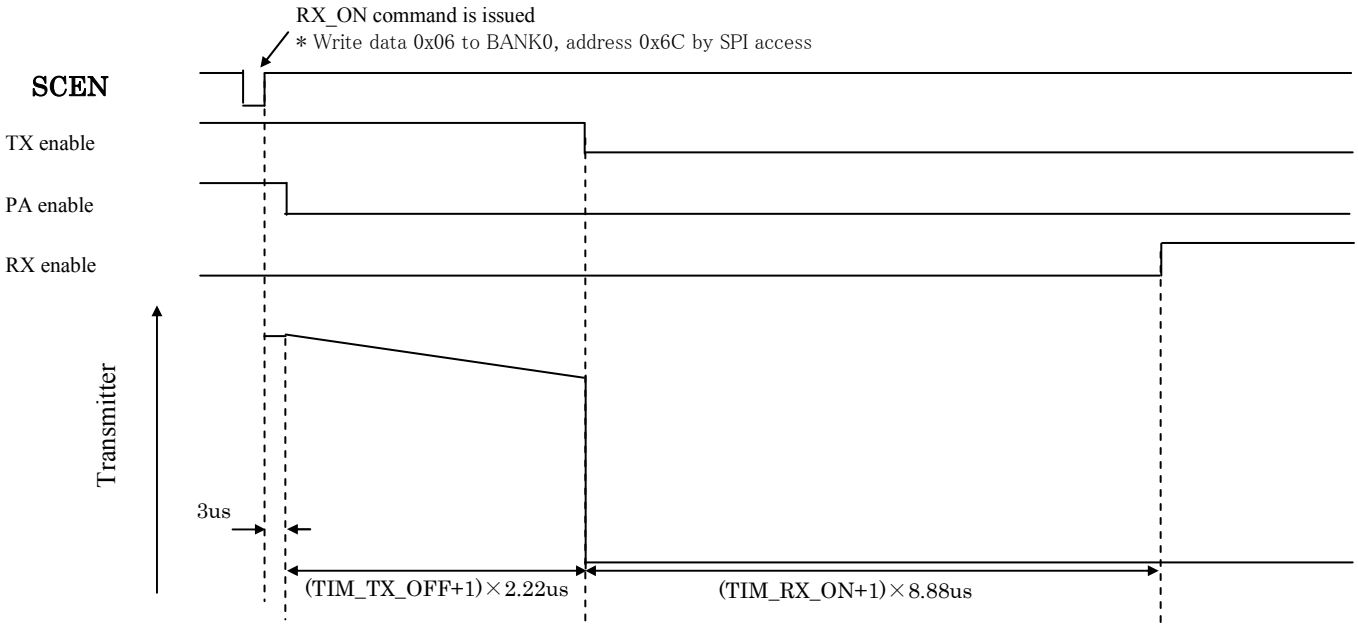
[RAMP_CNTRL] register (B2 0x2c) bit4 (TXOFF_RAMP_EN) = 0
[TX_OFF_ADD1] register (B1 0x55) bit7-0 (TIM_TX_OFF1) = 0xb4
[RX_ON_ADJ2] register (B1 0x3f) bit6-4 (TIM_RX_ON2) = 0x3
[GAIN_CONTRL] register (B0 0x6e) bit7-2 (TIM_TX_OFF2) = 0x2D



(4)When switching from transmission to reception (with lamp control disabled)

Register setting

[RAMP_CNTRL] register (B2 0x2c) bit4 (TXOFF_RAMP_EN) = 0
[TX_OFF_ADD1] register (B1 0x55) bit7-0 (TIM_TX_OFF1) = 0xb4
[RX_ON_ADJ2] register (B1 0x3f) bit6-4 (TIM_RX_ON2) = 0x3
[GAIN_CONTRL] register (B0 0x6e) bit7-2 (TIM_TX_OFF2) = 0x2D



■RF CONFIGRATION

●Programming Channel Frequency

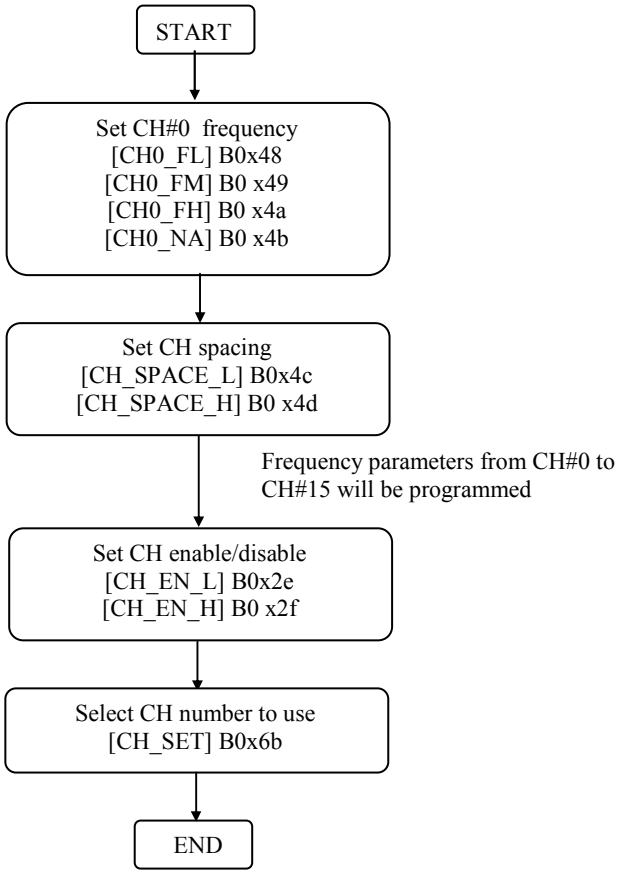
It is possible to set 16 channels in maximum (CH#0 to CH#15). This channel frequency can be configured by Channel #0 frequency parameter [CH0_FL], [CH0_FM], [CH0_FH] and [CH0_NA] (B0, 0x48-0x4B) and channel spacing parameter [CH_SPACE_L] and [CH_SPACE_H] (B0, 0x4c and 0x 4d). Usage of 16 channels can be enabled or disabled by register [CH_EN_L] and [CH_EN_H] (B0, 0x2e and 0x 2f).
The channel which will be used can be set by [CH_SET] register (B0, 0x6B) defined as channel number (#0 to #15)

[Notes]
Total range of frequency from CH#0 to CH#15 can not be integer multiple of 36MHz. (ex: 900MHz, 936MHz) The channel frequency needs to meet the following formula. If it does not meet the following formula, change the channel #0 frequency setting ([CH0_FL],[CH0_FM],[CH0_FH],[CH0_NA]).In case of those situation required, some channels can be disabled by [CH_EN_L] and [CH_EN_H] register

$$36\text{MHz}\times n + 2.2\text{MHz} \leq \text{channel frequency} < 36\text{MHz}\times(n+1) - 500\text{kHz} \quad * \ n=\text{integer}$$

Note that, if this formula does not hold, the expected channel frequency is not achieved, or it does not operate normally due to PLL unlock.

[Channel frequency programming flow]



○Programming Channel#0 Frequency parameter

It is possible to configure channel #0 frequency by registers [CH0_FL], [CH0_FM], [CH_FH] and [CH_NA] (B0 0x48-0x4b). Following equations will represent PLL parameters.

Setting frequency=Carrier frequency at TX mode

Frequency setting of Fractional-N type PLL will be derived following parameters..

f	: PLL oscillation frequency
f_{REF}	: PLL reference frequency (input clock: 36MHz)
P	: Dual modulus parameter（fixed to 4）
N	: N counter parameter
A	: A counter parameter
F	: F counter parameter

Each frequency register will have following values.

$N = int[f / f_{REF} / P]$

$A = int[f / f_{REF} - N \times P]$

$F = int[\{ f / f_{REF} - (N \times P + A) \} \times 2^{20}]$ ・・・Internal block uses 20bit width

Therefore frequency error will be $ferr = f - [f_{REF} \times \{(N \times P + A) + F/2^{20}\}]$

Ex）If f=923.1MHz, each parameter will be as follows when f_{REF} = 36MHz

$N = int[(923.1M / 36M / 4)] = 6$

$A = int[(923.1M / 36M - 6 \times 4)] = 1$

$F = int[\{923.1M / 36M - (6 \times 4 + 1)\} \times 2^{20}] = 672836$ (0xA4444)

Here

[CH0_FL] (B0, 0x48) = 0x44
[CH0_FM] (B0, 0x49) = 0x44
[CH0_FH] (B0, 0x4a) = 0x0A
[CH0_NA] (B0, 0x4b)= 0x61

In this case freuqency error will be $ferr = 923.1M - [36M \times \{(6 \times 4 + 1) + 672836 / 2^{20}\}] = +31.7Hz$

○Programming Channel spacing

It is possible to configure channel spacing by using registers［CH_SPACE_L］and [CH_SPACE_H] (B0, 0x4c and 0x4d). Channel spacing is frequency interval between centre frequency of certain channel and that of next channel.
PLL parameter values for channel spacing will be computed by following equation.

Setting Frequency =Wanted channel spacing

Parameter for CH_SP_F will be derived from following equation.

$CH\_SP\_F = int[\{ f / f_{REF} \} \times 2^{20}]$ ・・・internal block uses 20bit width

ex）In case of Channel spacing is 400kHz, each parameter will be computed as follow when f_{REF} = 36MHz.

$CH\_SP\_F = int[\{0.4M \div 36M\} \times 2^{20}] = 11650$ (0x2D82)

[CH_SPACE_L] (B0, 0x4c) = 0x82
[CH_SPACE_H] (B0, 0x4d) = 0x2D

●Programming IF Frequency

T.B.D.

●Programming BPF band width

T.B.D.

●Programming Frequency deviation

It is possible to configure frequency deviation by register [F_DEV_L] and [F_DEV_H] (B0, 0x4e and 0x4f) when GFSK modulation is used. PLL parameter will be computed by following equation.

Setting Frequency=Wanted frequency deviation

Parameter for F_DEV will be derived from following equation

$F\_DEV=int[\ \{\ f \div f_{REF}\ \} \times 2^{20}\ ]$ ・・・internal block uses 20bit width

ex) In case of data rate at 100kbps, configure f =50kHz, each parameter will be computed as follow when f_{REF} = 36MHz.

$F\_DEV = int[\ \{0.05M \div 36M\} \times 2^{20}\ ] = 1456$ (0x05B0)

[F_DEV_L] (B0 0x4e)= 0xb0
[F_DEV_H] (B0 0x4f)= 0x05

Following table shows example of parameter for frequency deviation that will be m=1 for each data rate.

Symbol	50kbps	100kbps	150kbps	200kbps
F_DEV_L	0xD8	0xB0	0x44	0x60
F_DEV_H	0x02	0x05	0x04	0x0B

For 10kbps/20kbps/40kbps, see "Initial setting register."

●Programming Gaussian Filter

BT products value of GFSK can be configure by registers [GFIL00] to [GFIL11] (B0, 0x59-0x64). Following table shows example of BT value and register configuration. Default value of [DATA_SET] register (B0, 0x47) is GFSK is enabled, and data rate is configured as 100kbps. BT value will be 0.5.

Tbl. Gaussian filter register setting (10kbps/20kbps/40kbps/50kbps/100kbps/150kbps/200kbps) (HEX)

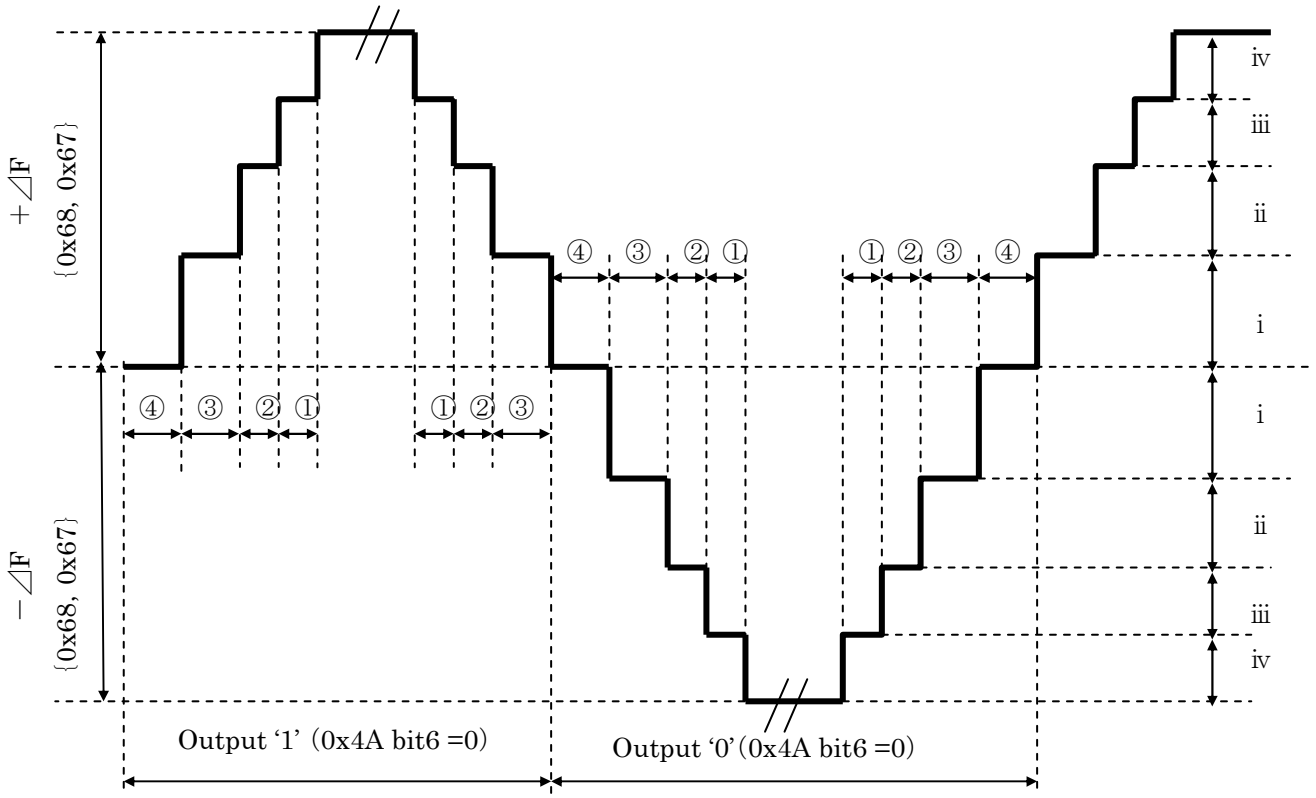
Symbol	Address:	bit	BT=1.0	BT=0.5	BT=0.4	BT=0.3	BT=0.25
GFIL00	0x59	[1:0]	0	0	0	0	1
		[3:2]	0	0	0	0	1
		[5:4]	0	0	0	1	1
		[7:6]	0	0	0	1	2
GFIL01	0x5a	[3:0]	0	0	0	1	3
		[7:4]	0	0	1	2	4
GFIL02	0x5b	[3:0]	0	0	1	3	5
		[7:4]	0	1	2	5	6
GFIL03	0x5c	[7:0]	00	01	03	06	07
GFIL04	0x5d	[7:0]	00	03	05	08	09
GFIL05	0x5e	[7:0]	00	05	08	0A	0A
GFIL06	0x5f	[7:0]	00	09	0C	0C	0C
GFIL07	0x60	[7:0]	03	0F	0F	0E	0D
GFIL08	0x61	[7:0]	0B	15	13	10	0E
GFIL09	0x62	[7:0]	1D	1A	17	13	0F
GFIL10	0x63	[7:0]	35	1F	1A	14	10
GFIL11	0x64	[7:0]	40	20	1A	14	12

Tbl. Gaussian filter register setting (400kbps(Optional.)) (HEX)

Symbol	Address:	bit	BT=1.0	BT=0.5	BT=0.4	BT=0.3	BT=0.25
GFIL00	0x59	[1:0]	0	0	0	0	0
		[3:2]	0	0	0	0	0
		[5:4]	0	0	0	0	0
		[7:6]	0	0	0	0	0
GFIL01	0x5a	[3:0]	0	0	0	0	0
		[7:4]	0	0	0	0	0
GFIL02	0x5b	[3:0]	0	0	0	0	0
		[7:4]	0	0	0	0	1
GFIL03	0x5c	[7:0]	00	0	00	00	01
GFIL04	0x5d	[7:0]	00	0	00	01	03
GFIL05	0x5e	[7:0]	00	0	01	03	05
GFIL06	0x5f	[7:0]	00	0	02	07	09
GFIL07	0x60	[7:0]	00	03	07	0C	0F
GFIL08	0x61	[7:0]	00	0B	10	14	15
GFIL09	0x62	[7:0]	05	1D	1F	1D	1A
GFIL10	0x63	[7:0]	3C	35	2D	24	1F
GFIL11	0x64	[7:0]	7E	40	34	28	20

●Programming FSK modulation

In FSK modulation, each modulation parameters can be defined by following registers [FSK_FDEV1] to [FSK_FDEV4] (B0, 0x59-0x5c) and [FSK_TIME1] to [FSK_TIME4] (B0, 0x65-0x68).



param	Symbol	Address:	Function:	param	Symbol	Address:	Function:
i	FSK_FDEV1	0x59	Freq dev 33.4x2(Hz)	①	FSK_TIME1	0x65	Modulation timing by 4MHz counter
ii	FSK_FDEV2	0x5a		②	FSK_TIME2	0x66	
iii	FSK_FDEV3	0x5b		③	FSK_TIME3	0x67	
iv	FSK_FDEV4	0x5c		④	FSK_TIME4	0x68	

[Note]

1. Data rate 400kbps is not supported by FSK.

●Programming Data rate changing

T.B.D.

● Programming narrow band option changing

T.B.D.

■RF adjustment

●PA adjustment

T.B.D.

●I/Q adjustment

T.B.D.

●VCO adjustment

T.B.D.

○Programming Lowest Freaquency of VCO

T.B.D.

○Programming Highest Freaquency of VCO

T.B.D.

T.B.D.

●Energy Detection value adjustment

T.B.D.

■OTHER SETTING

●BER measurement setting

When you want to measure BER using this LSI, you must change the following register settings on the tested device (receiver).

[BANK 0] () represents the address.
Write 0x01 to [PLL_MON/DIO_SEL] register (0x69)

[BANK 1]
Write 0x80 to [DEMOD_SET] register (x01)

[BANK 2]
Write 0x00 to [SYNC_MODE] register (0x12)
Write 0x10 to [DEMOD_SET2] register (0x0a)

■FLOW CHARTS

●Initialization

T.B.D.

T.B.D.

●TX mode (with DIO mode)

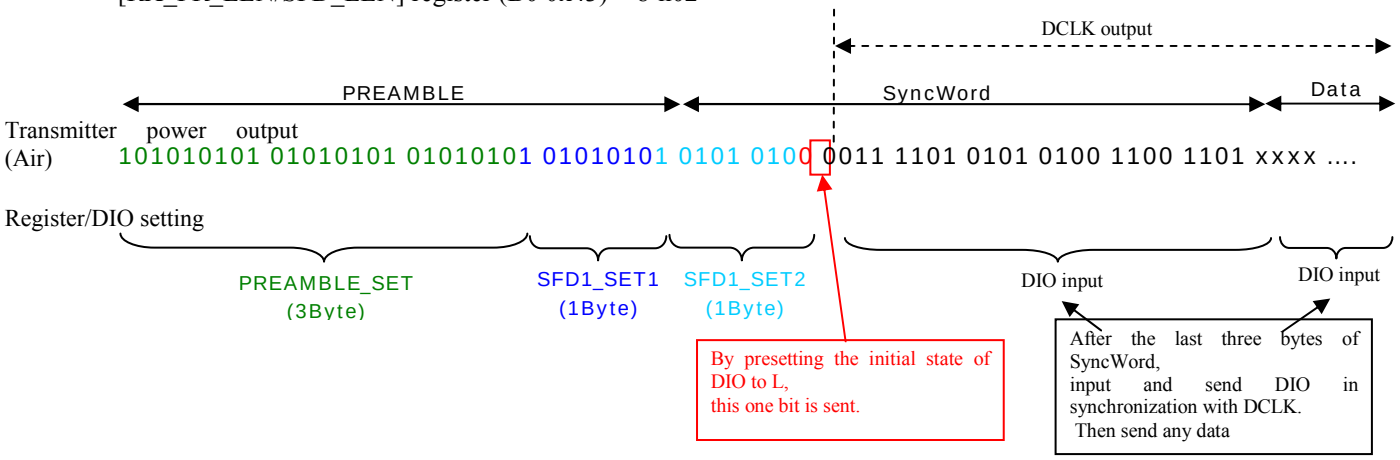
It is possible to use DIO mode by writing [PLL_MON/DIO_SEL] register (B0, 0x69)bit1 (DIO_EN)=0b1and bit0(RX_FIFO_MON)=0b1.. PB (preamble) and SFD transmission followed by TX data input from DIO will be output. TRX_OFF will be issued to complete TX mode. (Example: bit0 of [FEC/CRC_SEC] register (B0 0x46)=0b0, [WR_TX_FIFO] register (B0 0x7e)=00-01-02(FIFO write)). For the first bit at DIO transmission, a fall of DCLK does not occur because DCLK output starts from L. Therefore, input the first bit data to the DIO pin (initial state) before FIFO dummy write.

The relationship between [PREAMBLE_SET] and [SFD1_SETx] registers and DIO input setting and transmitted packets is described below.

Example) When supporting prEN 13757-4rev Mode C FormatA

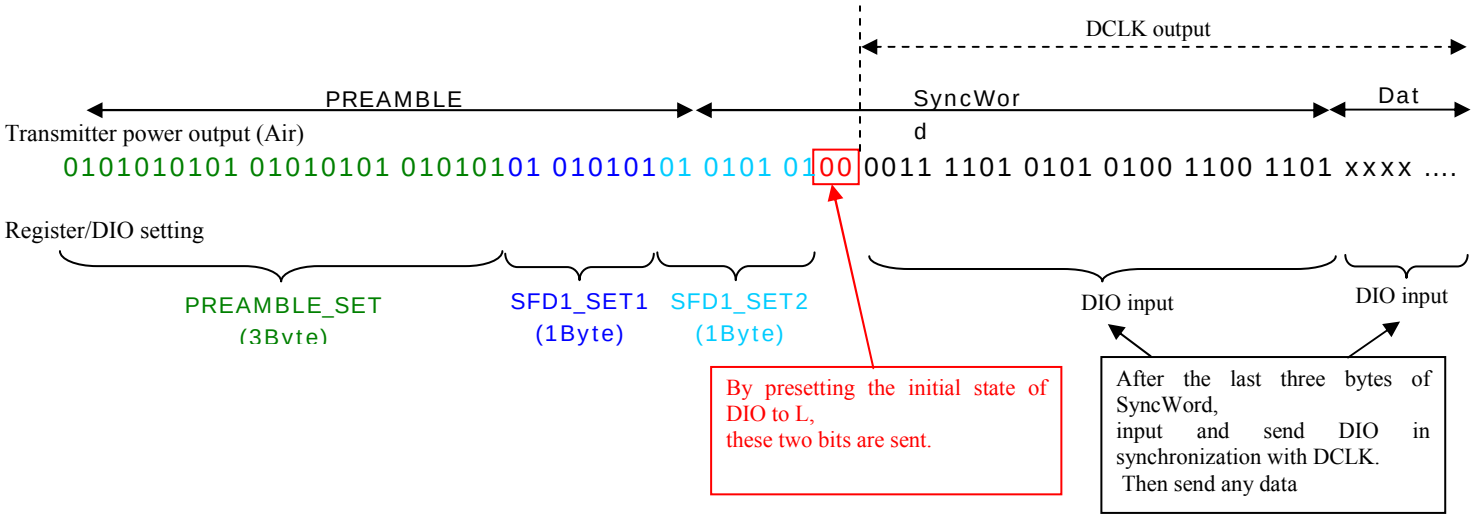
[DIO input with DCLK posedge synchronization]

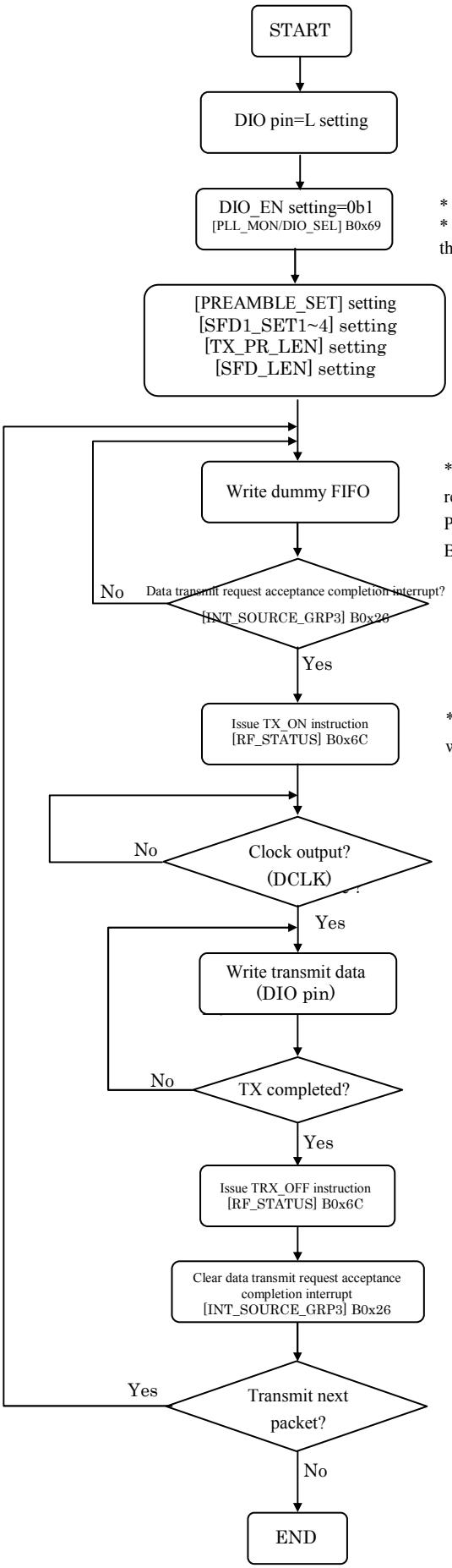
[PREAMBLE_SET] register (B0 0x39) = 0x55
[SFD1_SET1] register (B0 0x3A) = 0x55
[SFD1_SET2] register (B0 0x3B) = 0x55
[TX_PB_LEN] register (B0 0x42) = 8'h03
[RX_PR_LEN/SFD_LEN] register (B0 0x43) = 8'h02



[DIO input with DCLK negedge synchronization]

[PREAMBLE_SET] register (B0 0x39) = 0xAA
[SFD1_SET1] register (B0 0x3A) = 0xAA
[SFD1_SET2] register (B0 0x3B) = 0xAA
[TX_PB_LEN] register (B0 0x42) = 8'h03
[RX_PR_LEN/SFD_LEN] register (B0 0x43) = 8'h02





* The first bit of the transmit data is input to the DIO pin.
* RX_FIFO_MON(B0 0x69 bit9) setting does not affect this DIO mode transmit operation.

* Write 00-01-02(CRC setting disable) to [WR_TX_FIFO] register (B0x7e).
Preamble/SFD is sent with the data and setting set by B0x39 - B0x42.

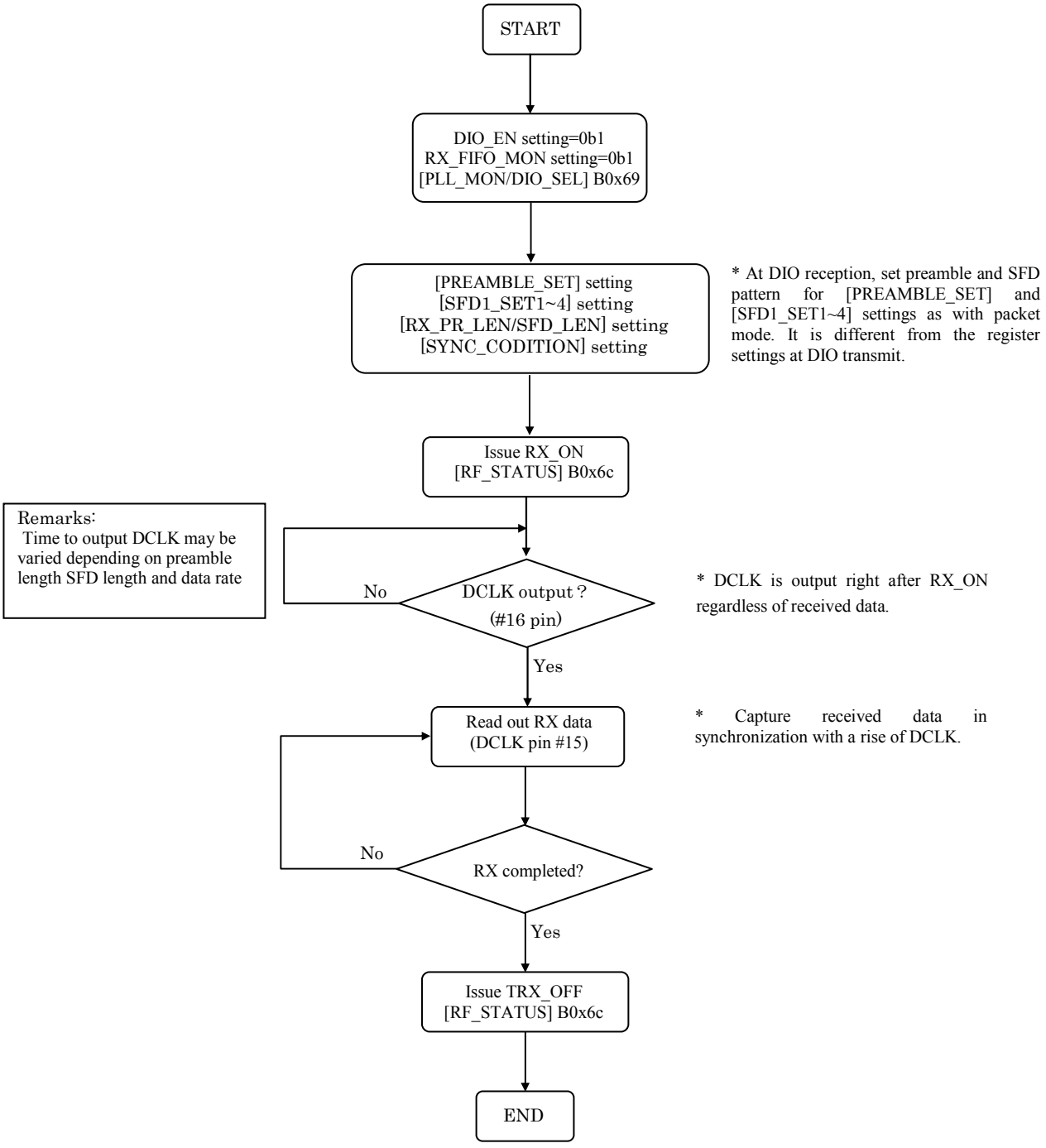
* TX_ON instruction works in the same way as before FIFO dummy write.

※Time to start DCLK output may be varied depending on preamble length and SFD length and data rate.

※Input the second and later bits of the transmit data in synchronization with a fall of DCLK.

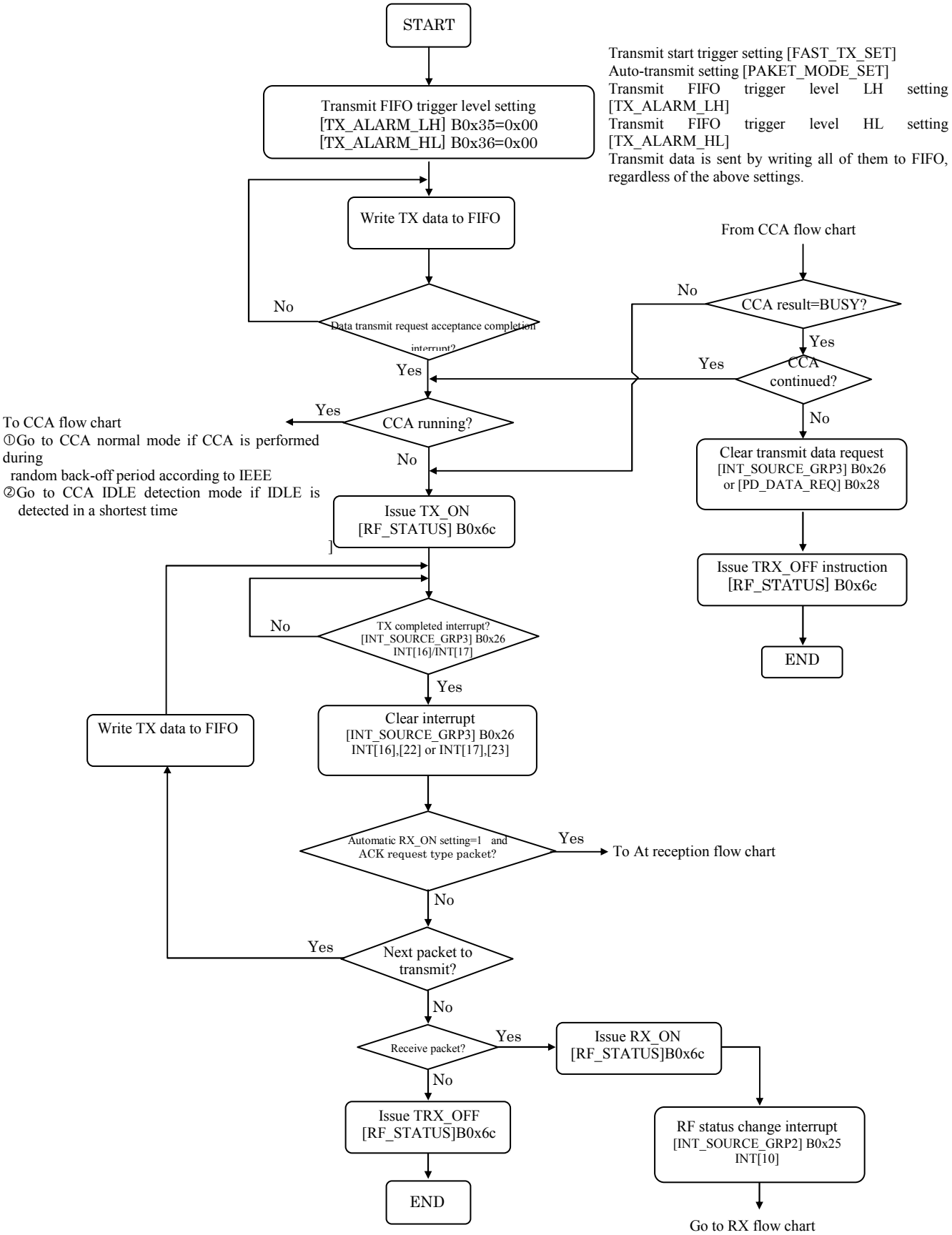
●RX mode（with DIO mode）

It is possible to use DIO mode by writing [PLL_MON/DIO_SEL] register (B0 x69) bit1 (DIO_EN)=0b1. PHY block will search for pattern matching to preamble data and following SFD data from incoming data from DeMOD (Demodulator) block. Once pattern matching done, RX data will output from DIO pin. Issue TRX_OFF, to stop RX mode.
This LSI internally detects SFD and notifies of it with a detection completion interrupt, according to the settings of [PREAMBLE_SET] register (B0 0x39), [SFD1_SET1] register (B0 0x3a) – [SFD1_SET4] register (B0 0x3d), [RX_PR_LEN/SFD_LEN] register (B0 0x43), and [SYNC_CONDITION](B0 0x44), as with FIFO. The first rise of DCLK after the interrupt notification is the first received data after SFD (at 100kbps setting. It takes about 9us from SFD detection interrupt notification to the next rise of DCLK).



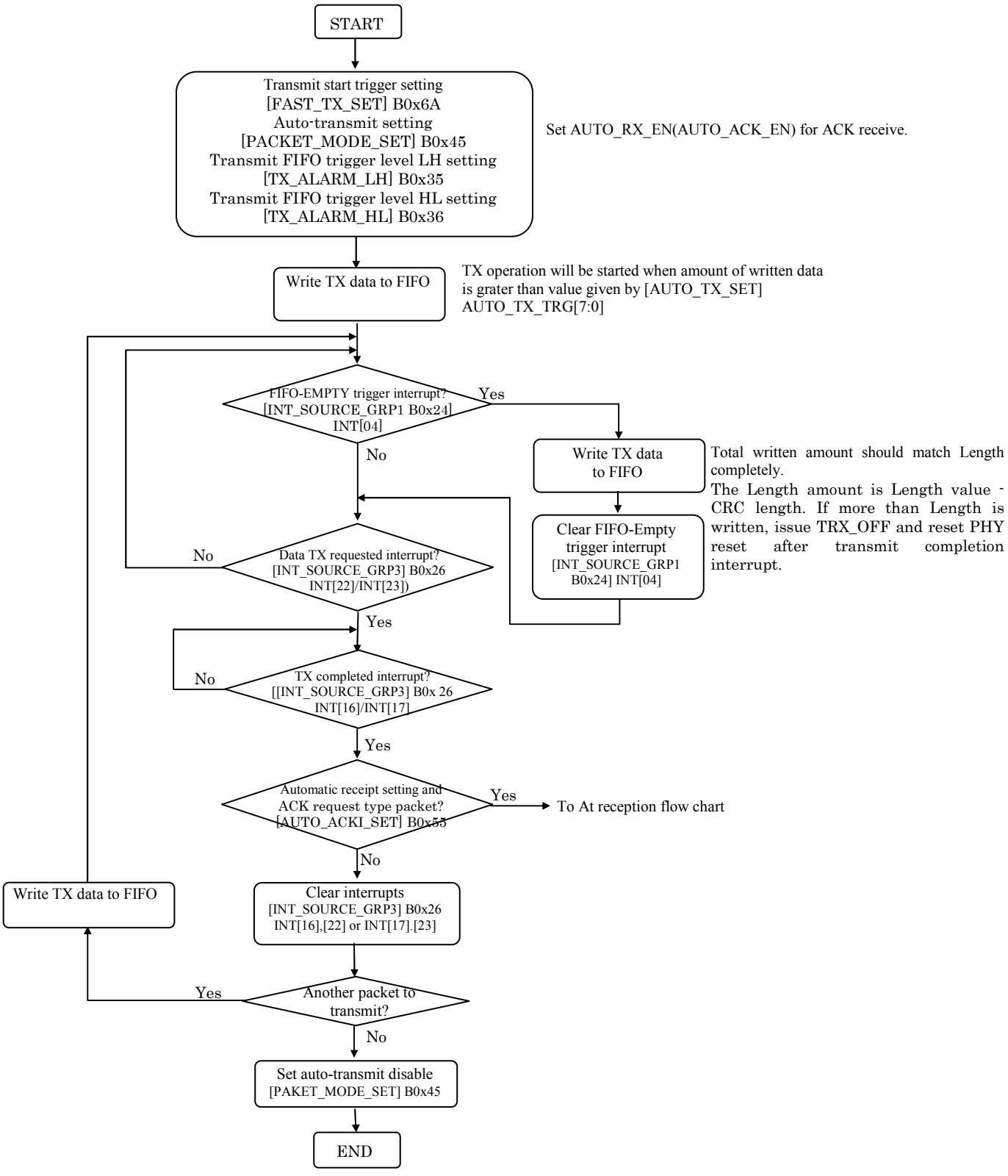
●TX mode（with packet mode, packet length < 256byte）

It is possible to use packet mode by writing [PLL_MON/DIO_SEL] register (B0, 0x69) bit1 (DIO_EN)=0b0. In packet mode, each packet data to transmit will be written into FIFO. The data in the FIFO is transmitted after PB (preamble), SFD data. Writing TX data into FIFO, and then followed by TX_ON, data transmission will start. If there is interrupt reporting completion of TX data, clear the interrupt. Write another packet if more packet data to send. Or receive data after transmit data, enable RX_ON by [RF_STATUS] register (B0, 0x6c). Issue TRX_OFF to stop data transmission.
Packet transmission interval time can be configure by [SIFS_LEN] , [SIFS_PD], [LIFS_PD]. There are 2 bank of FIFO which will be used alternately. If CRC computation is enabled, the computation will be done by automatically by hardware, attach CRC result to the end of packet data.


START
Transmit FIFO trigger level setting
[TX_ALARM_LH] B0x35=0x00
[TX_ALARM_HL] B0x36=0x00
Transmit start trigger setting [FAST_TX_SET]
Auto-transmit setting [PAKET_MODE_SET]
Transmit FIFO trigger level LH setting [TX_ALARM_LH]
Transmit FIFO trigger level HL setting [TX_ALARM_HL]
Transmit data is sent by writing all of them to FIFO, regardless of the above settings.
Write TX data to FIFO
No
Data transmit request acceptance completion interrupt?
Yes
From CCA flow chart
No
CCA result=BUSY?
Yes
Yes
CCA continued?
No
Yes
CCA running?
To CCA flow chart
①Go to CCA normal mode if CCA is performed during
random back-off period according to IEEE
②Go to CCA IDLE detection mode if IDLE is detected in a shortest time
No
Clear transmit data request
[INT_SOURCE_GRP3] B0x26
or [PD_DATA_REQ] B0x28
Issue TX_ON
[RF_STATUS] B0x6c
]
Issue TRX_OFF instruction
[RF_STATUS] B0x6c
END
No
TX completed interrupt?
[INT_SOURCE_GRP3] B0x26
INT[16]/INT[17]
Yes
Write TX data to FIFO
Clear interrupt
[INT_SOURCE_GRP3] B0x26
INT[16],[22] or INT[17],[23]
Automatic RX_ON setting=1 and
ACK request type packet?
Yes
To At reception flow chart
No
Yes
Next packet to transmit?
No
Receive packet?
Yes
Issue RX_ON
[RF_STATUS]B0x6c
No
Issue TRX_OFF
[RF_STATUS]B0x6c
END
RF status change interrupt
[INT_SOURCE_GRP2] B0x25
INT[10]
Go to RX flow chart

●TX mode (with packet mode, packet length >= 257byte)

Writing TX data to FIFO not to occurring FIFO become neither Full nor Empty. Normally when amount written data become same as packet length, TX operation will be started. However if [PACKET_MODE_SET] register (B0 0x45) bit2 (AUTO_TX) is 0b1, which is enabling automatic TX function, when TX data is written to FIFO is same as amount of data given by register [AUTO_TX_SET] (B0 0x6a), TX operation will be started automatically.

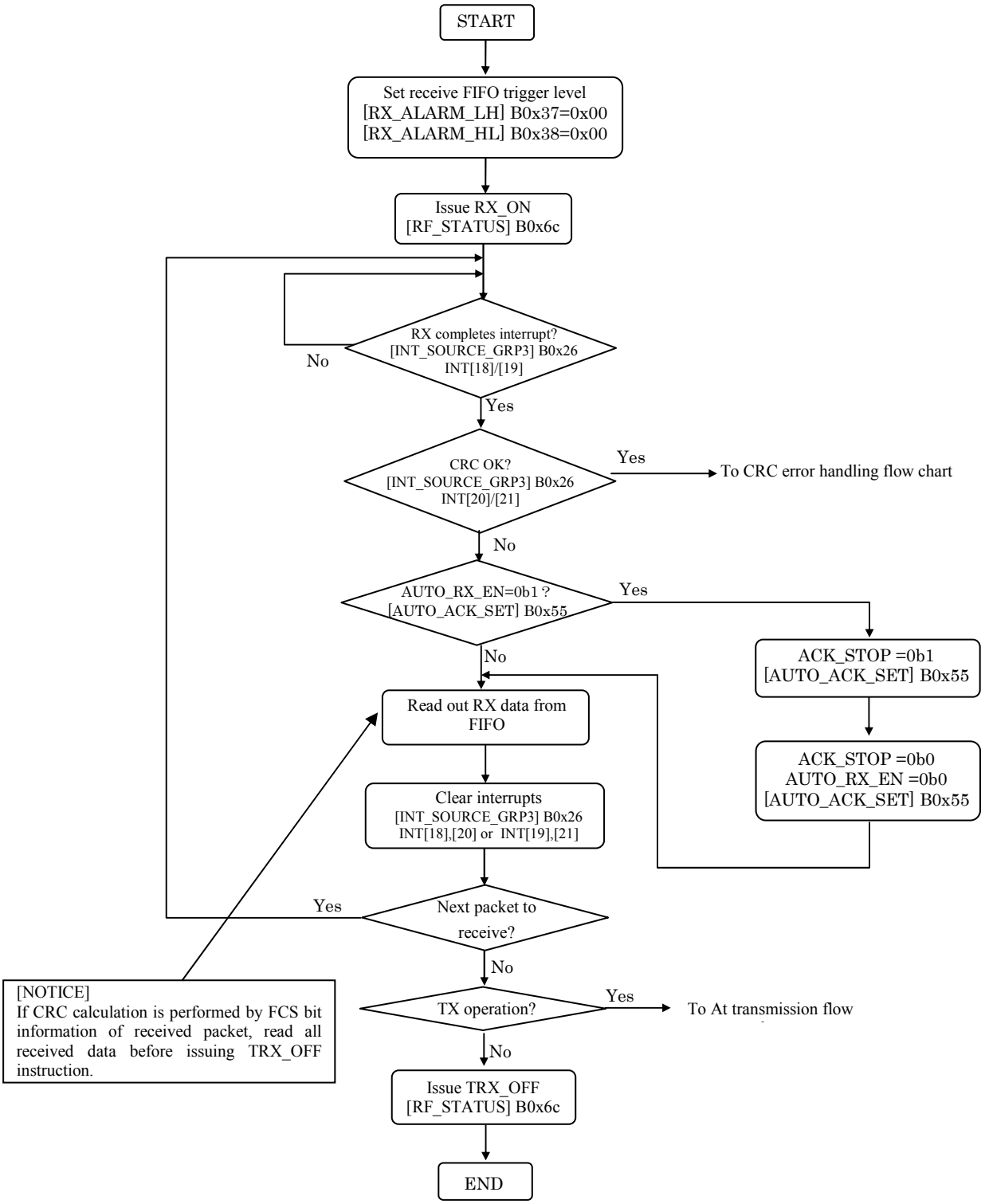


●TX mode (Ack receiving with address filter,)

T.B.D.

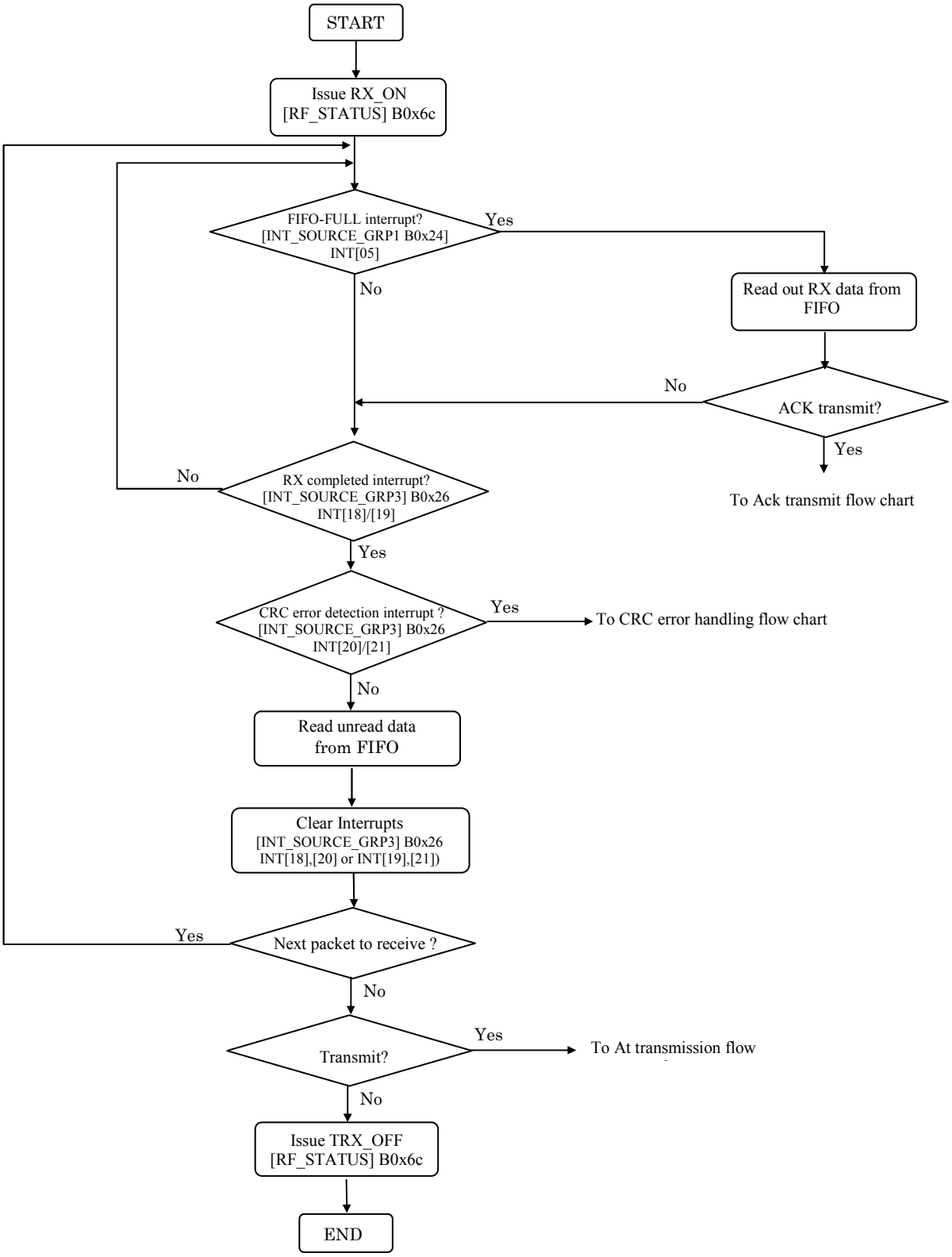
●RX mode (with packet mode, packet length < 256 bytes)

It is possible to use packet mode by writing [PLL_MON/DIO_SEL] register bit1 (DIO_SEL)=0b0, PHY block will search for pattern matching to preamble data and following SFD data from incoming data from DeMOD (Demodulator) block. Once pattern matching done, RX data will be stored into FIFO. If RX complete interrupt is taken place, read out received data from FIFO. If there is CRC error reported by interrupt, FIFO data has to be cleared by register [INT_SOURCE_GRP1] bit7 (FIFO_CLR1) or bit6 (FIFO_CLR0). If there are another packet to receive, maintain RX status then wait for interrupt for RX complete. If TX operation is required after received packet data, set [RF_STATUS] register (B0, 0x6c) to set TX enable. Issue TRX_OFF if there is no data to receive.



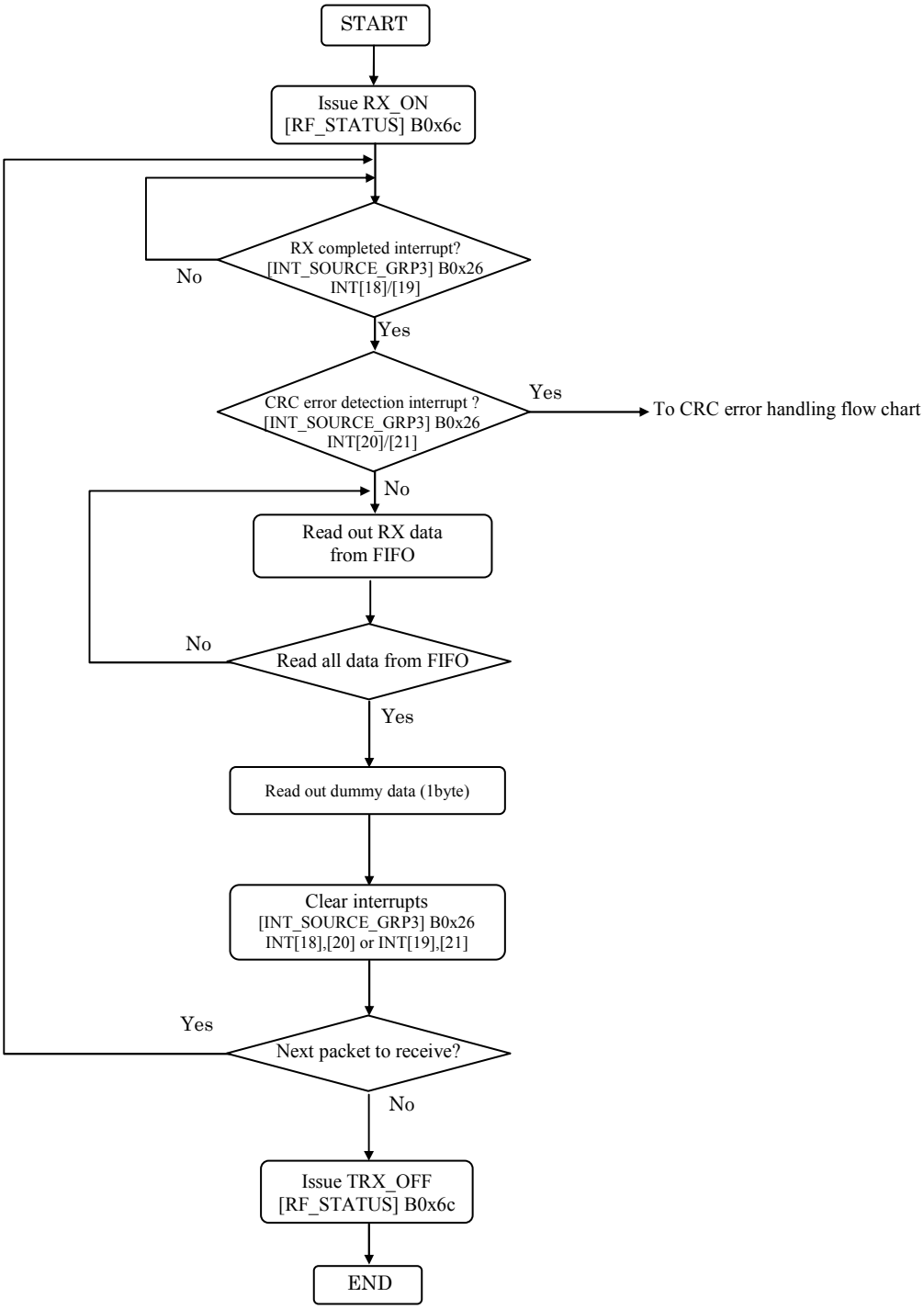
●RX mode (with packet mode, packet length >= 257 bytes)

Reading RX data from FIFO not to occurring FIFO become neither Full nor Empty.



●RX mode (with IEEE802.15.4d mode)

Principle of flow is same as IEEE 802.15.4g, if IEEE 802.14.4d mode is selected by register [PACKET_MODE_SET] (B0, 0x45) bit1 (IEEE_MODE)=0b0. However it is required to read out 1byte of dummy data after reading amount of data given by Length field.



●ACK TX mode (with AUTO_ACK, packet length < 256 bytes)

T.B.D.

●ACK TX mode (with AUTO_ACK, packet length >= 257 bytes)

T.B.D.

●ACK TX mode (without AUTO_ACK)

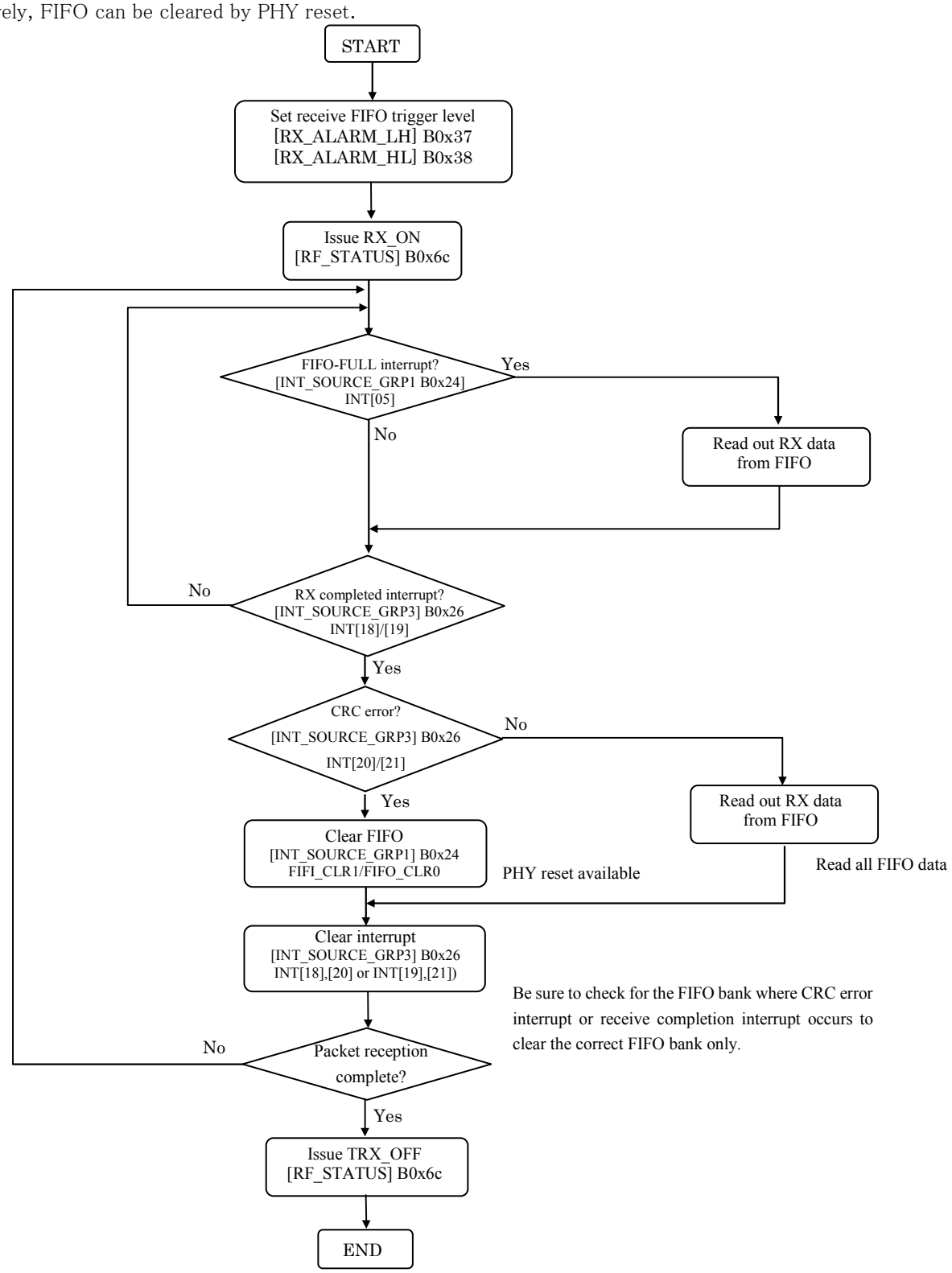
T.B.D.

●Address Filter

T.B.D.

●Clear FIFO

If data receive completion interrupt occurs before reading all received data, and you decide to leave the remaining data unread due to CRC error, etc., cleat FIFO (write 0b0 to bit7-6(FIFO_CLR1-0) of [INT_SOURCE_GRP1] register (B0 0x24)) and the interrupt (write 0b0 to bit5-2(INT[21-18]) of [INT_SOURCE_GRP3] register (B0 0x26)). Interrupt will be cleared, and maintain RX mode or issue TRX_OFF to stop RX mode. Be sure to clear the correct FIFO bank only. Alternatively, FIFO can be cleared by PHY reset.

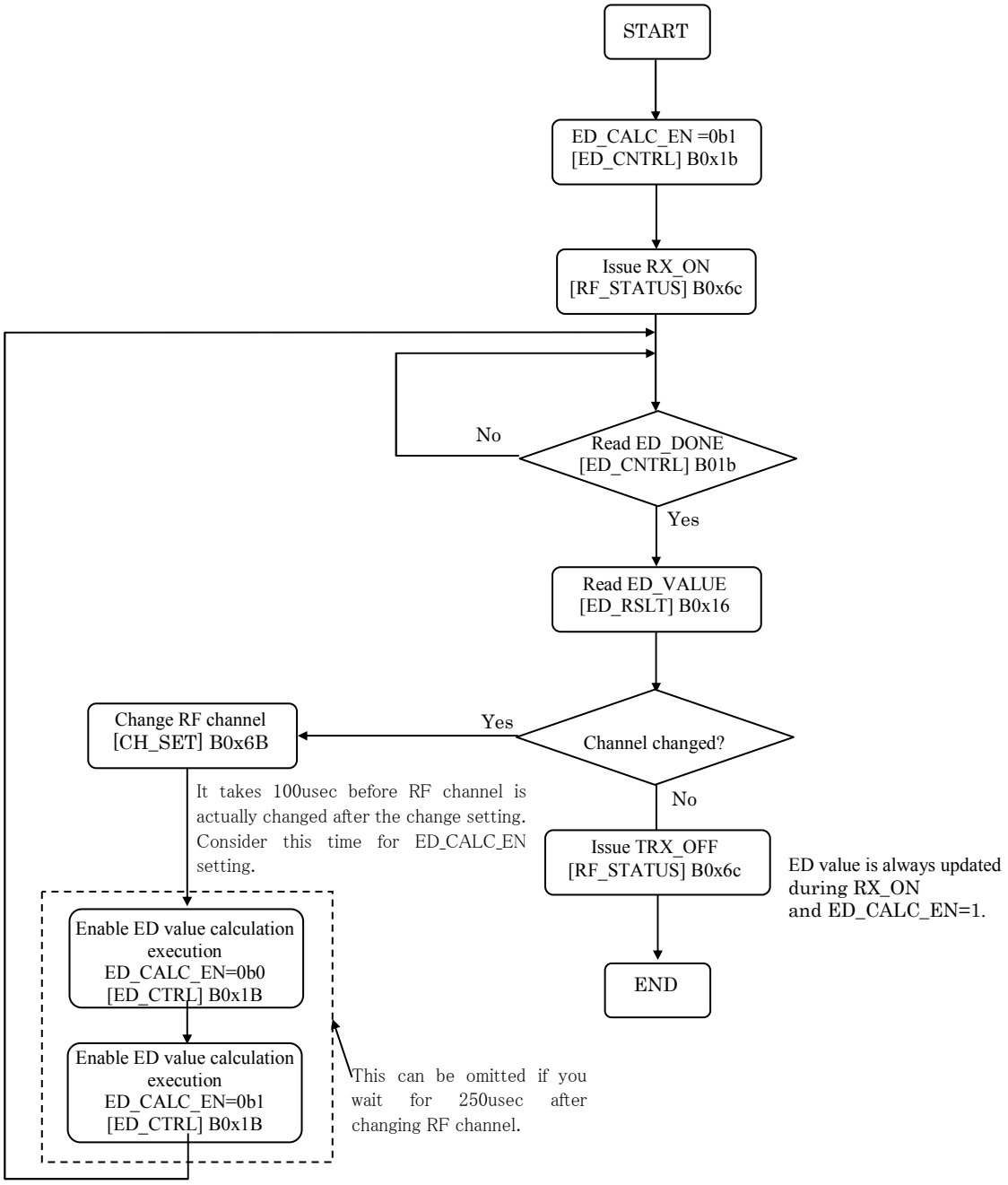


●SLEEP

T.B.D.

●ED value detection

When issue RX_ON while ED value detection enable [RD_CNTRL] register (B0, 0x1b) bit7 (ED_CALC_EN)=0b1 automatic ED value detection will be started. ED values will be updated when RX_ON is issued while ED_CALC_EN=1.



●CCA operation

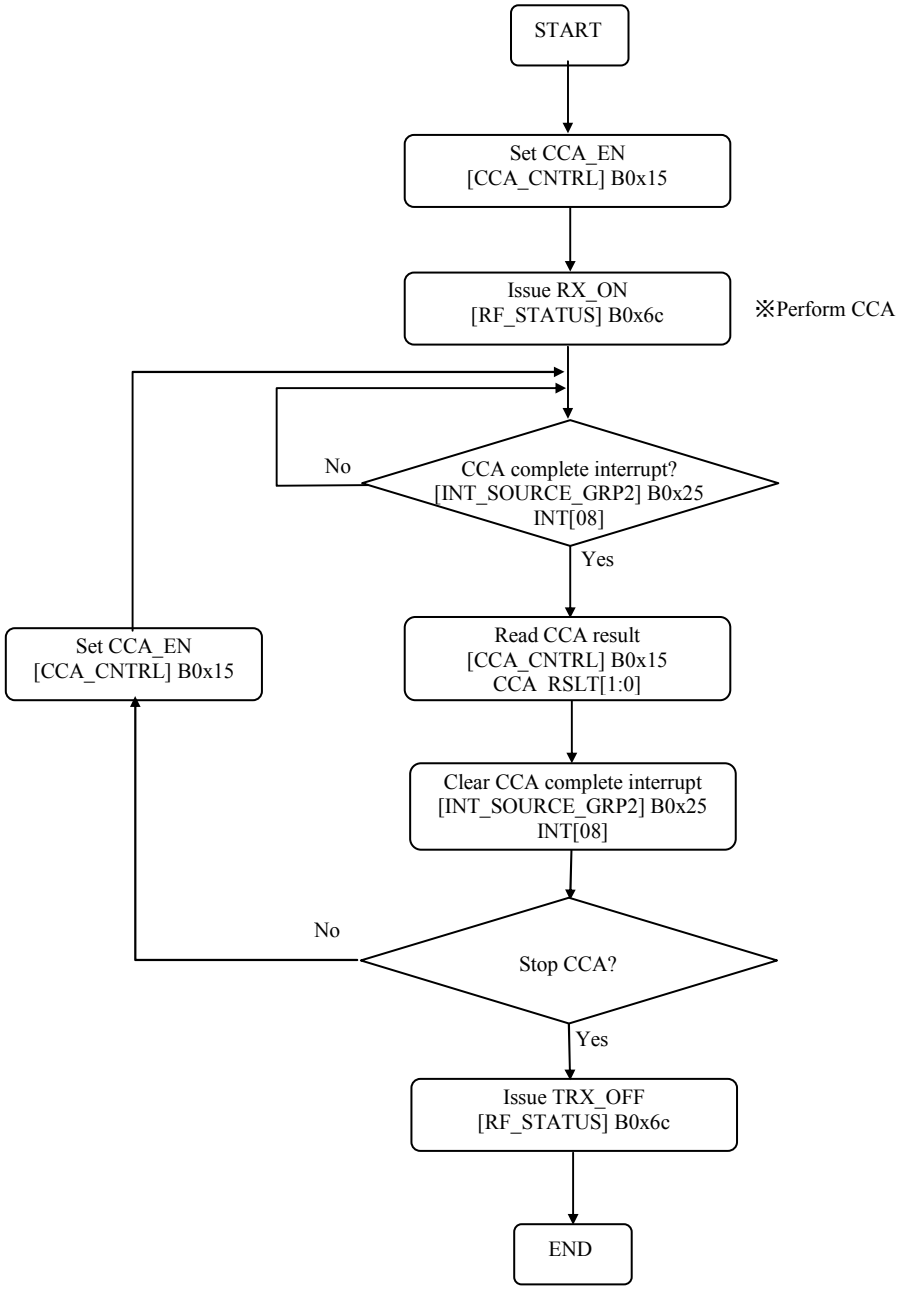
○Normal mode

CCA normal mode will be executed if receiver is activated by RX_ON while CCA_EN bit=0b1 and CCA_LOOP_START bit=0b0. The judgement of CCA is determined by comparison between ED value and threshold value defined by [CCA_LEVEL] (B0, 0x13). After CCA performed, CCA_EN bit will be set to disabled, and RF status maintain RX mode.

CCA can be performed by setting CCA_EN to 0b1 during RX_ON. In this case, the filter stabilization period 16usec – 32usec (A/D conversion x 2) of WAIT is automatically added before CCA. If CCA_EN is set before RX_ON, it is not added because transition time to RX_ON contains the filter stability period.

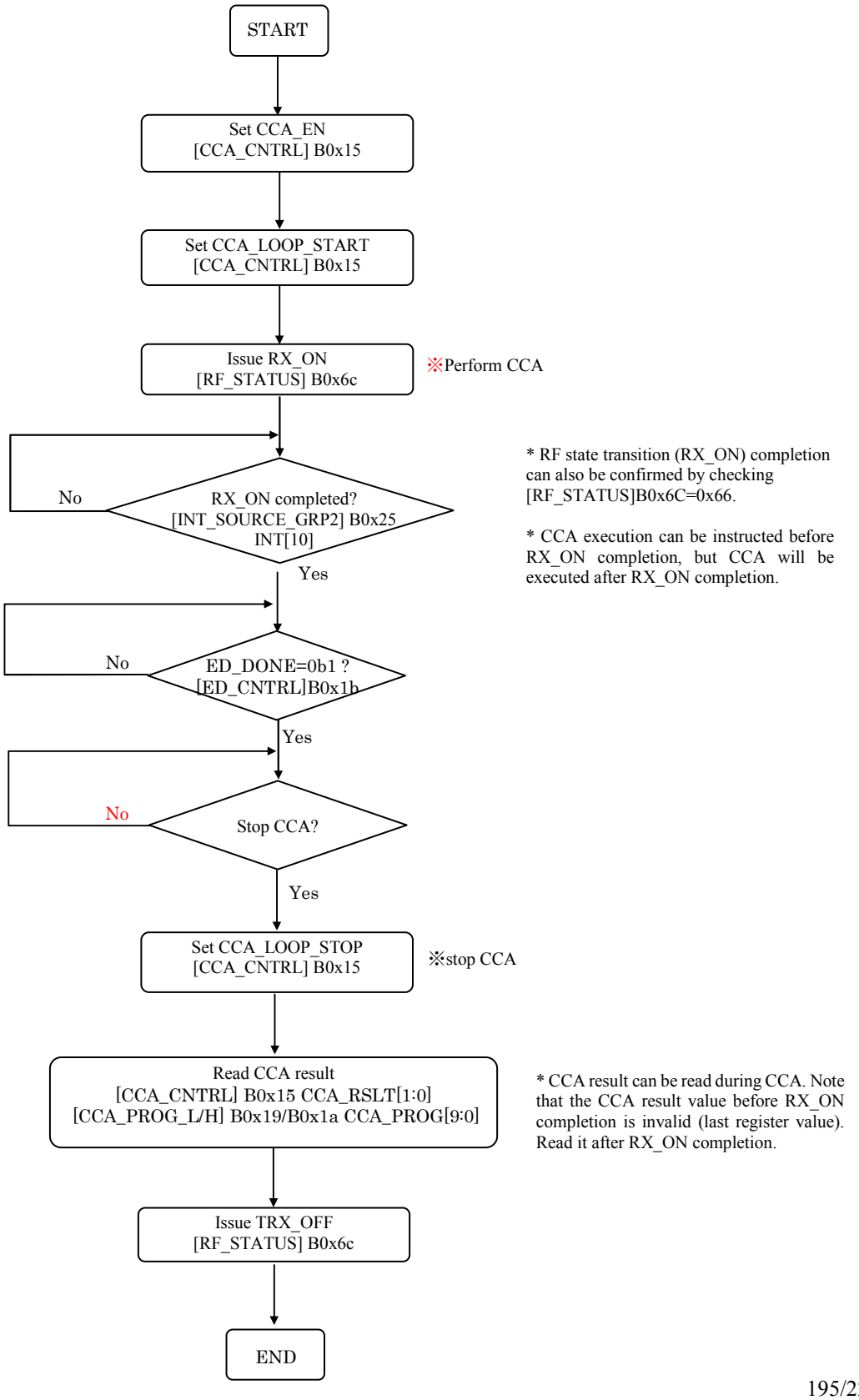
If desired wave is received and synchronization is established during CCA, the BPF bandwidth during CCA is kept to continue receiving. If CCA is performed while establishing synchronization, it is performed using the BPF bandwidth after establishing synchronization.

CCA can also be performed during diversity search. In this case, diversity search is automatically restarted after CCA completion.



○Continuous mode

In continuous mode, CCA operation will be repeated until HOST CPU stop its operation. It will be executed by RX_ON while CCA_EN bit=0b1, CCA_LOOP_START bit=0b1.Comparison will be performed each time when new ED value is obtained. CCA_DONE bit (bit2) will not be 0b1, no interrupt will be asserted. Bit1-0(CCA_RSLT) and [CCA_PROG_L/H] register (B0 0x19,0x1a) are always updated during CCA. When CCA_STOP is set to 1, these values are retained.

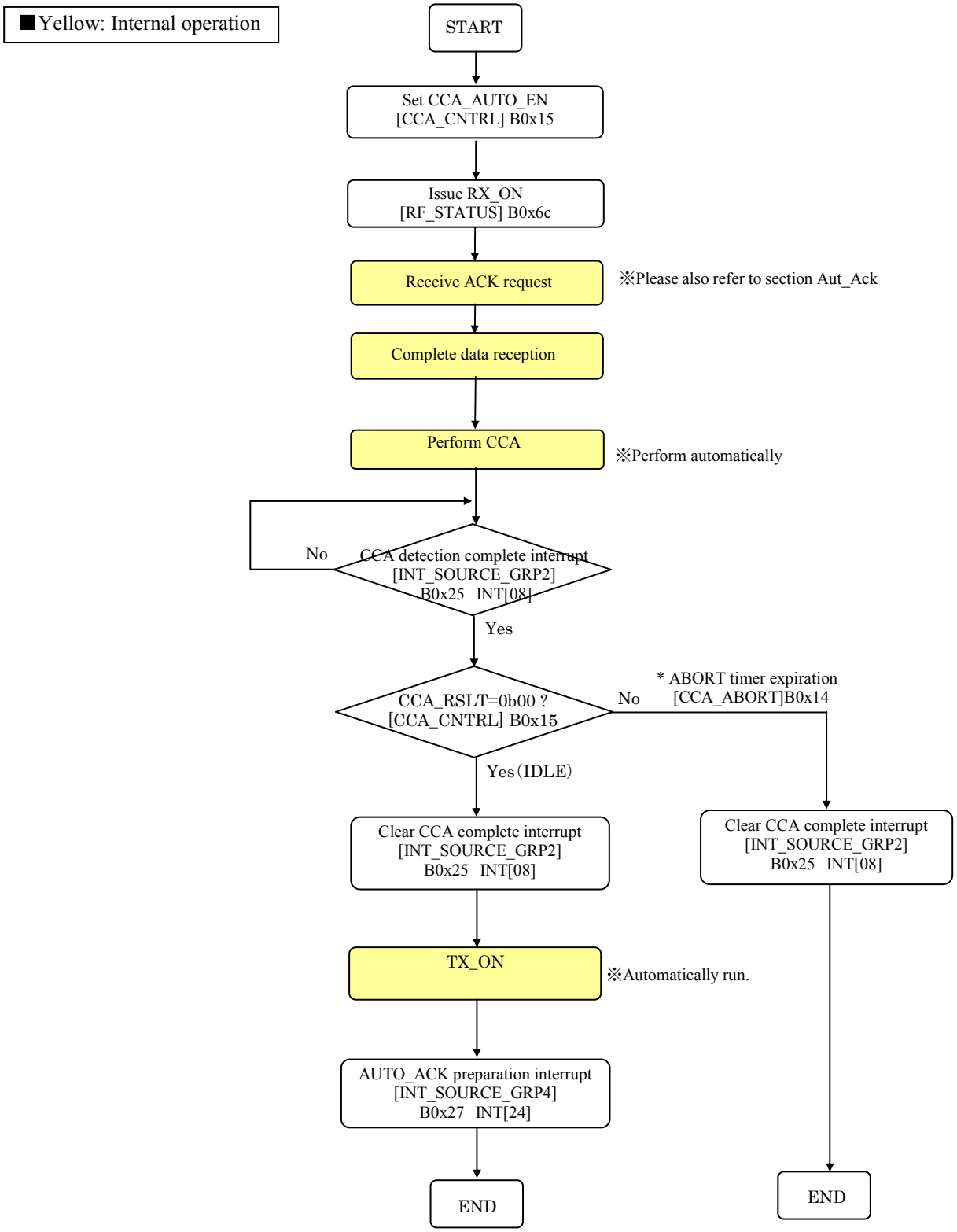


○IDLE detection mode

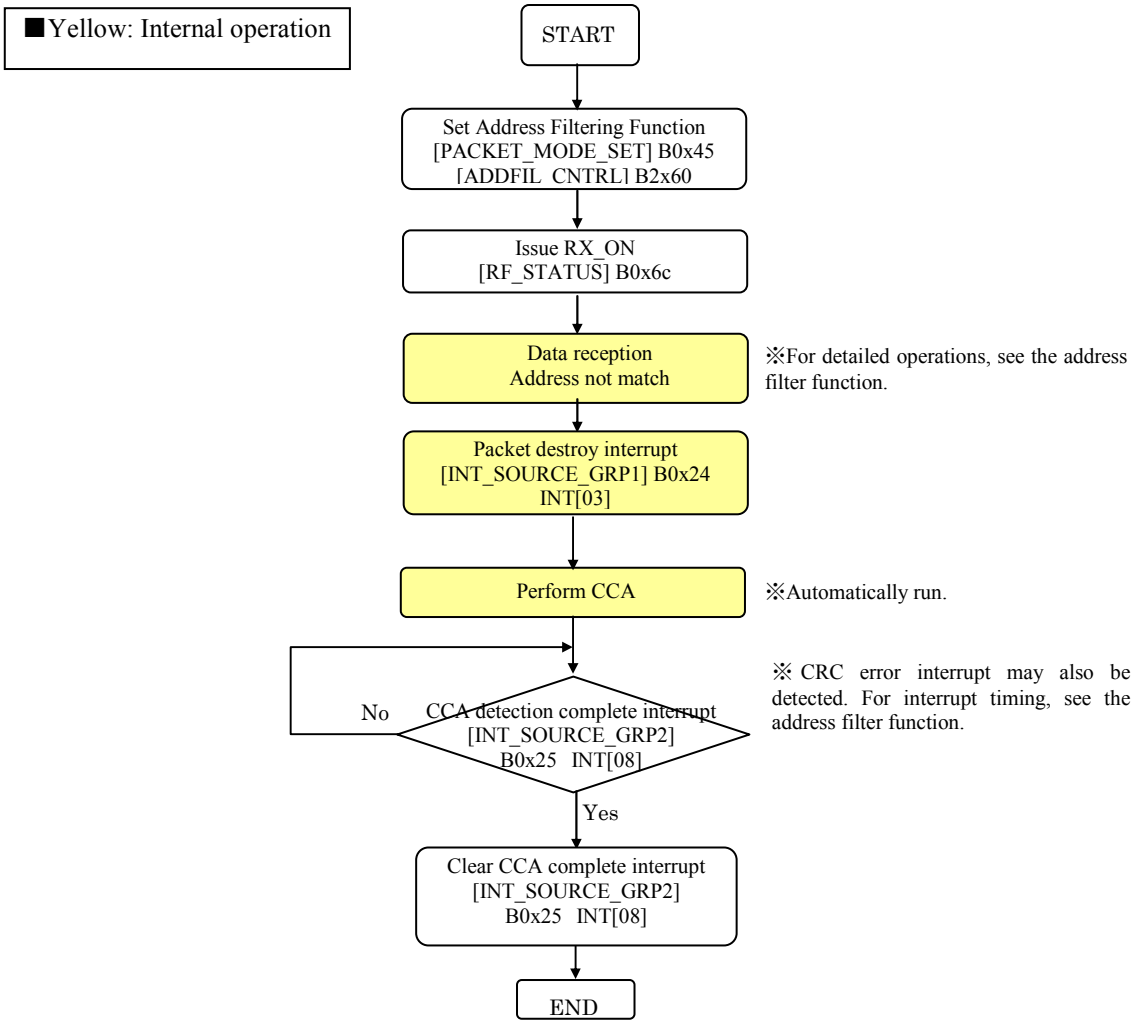
T.B.D.

There is two way of IDLE detection mode perform CCA until IDLE status of channel is detected.

1. Perform CCA in IDLE detection mode when Autobacs operation if [CCA_CNTRL] (B0 0x15) bit7 (CCA_AUTO_EN)=0b1



2. One of bit in [ADDFIL_CNTRL] register (B2 0x60) bit4-0 is set to 0b1, and address filtering function is enabled. And [PACKET_MODE_SET] register (B0 0x45) bit0 (ADDFIL_IDLE_DET)=0b1, perform CCA in IDLE detection mode after data is removed.



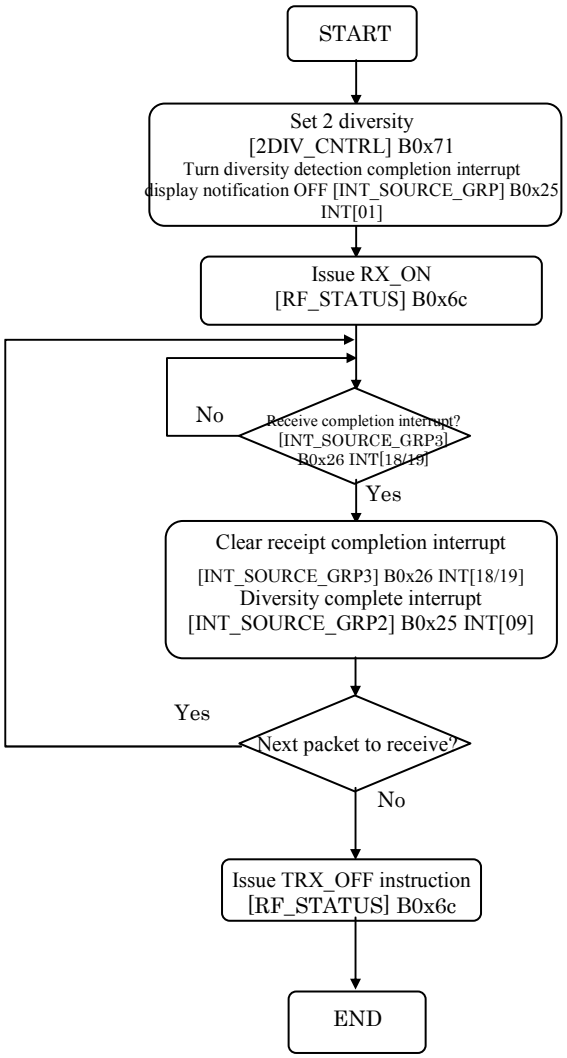
●2 diversity operation

If RX_ON is issued while [2DIC_CNTRL] register (B0, 0x71) bit1 (2DIV_EN)=0b1, switching antenna while receiving data and obtain ED value from both branches, then select the branch has higher ED value.

After that, antennas are switched to acquire each ED value when detecting received data, and the antenna with the higher value is used. This LSI automatically operates the ANT search timer after diversity completion. When a preamble cannot be detected at timer expiration, it is determined that the first preamble detection is a false detection caused by thermal noise, etc., the antenna search is automatically performed again. This behavior does not need a register setting. Therefore, the high order MCU does not need to consider wrong diversity completion due to thermal noise. To run diversity for the next packet, clear the receive completion interrupt and the diversity detection completion interrupt after the receive is completed on the high order MCU.

For details, see the energy detection value (ED value) acquisition function.

The ED value acquired by the diversity and the diversity antenna result are cleared at the diversity detection completion interrupt clearing, or at the receive completion interrupt (INT_SOURCE_GRP3 register (B0 0x26) INT[18],INT[19]) clearing when the antenna search is automatically performed again due to the wrong diversity completion judgment. Read the ED value acquired by the diversity and the diversity antenna result before clearing the receive completion interrupt.



* When 2DIV_EN is changed from 0b0 to 0b1 during RX_ON, antenna search is performed after search timer ([2DIV_SEARCH]B0x6f) expiration. If SFD is detected while counting search timer, receiving is continued without performing antenna search.

●CCA execution with 2 diversity

T.B.D.

T.B.D.

●Process when an error occurs

○CRC Error

T.B.D.

○TX FIFO Access Error

T.B.D.

○RX FIFO Access Error

T.B.D.

○PLL Unlock Detection

T.B.D.

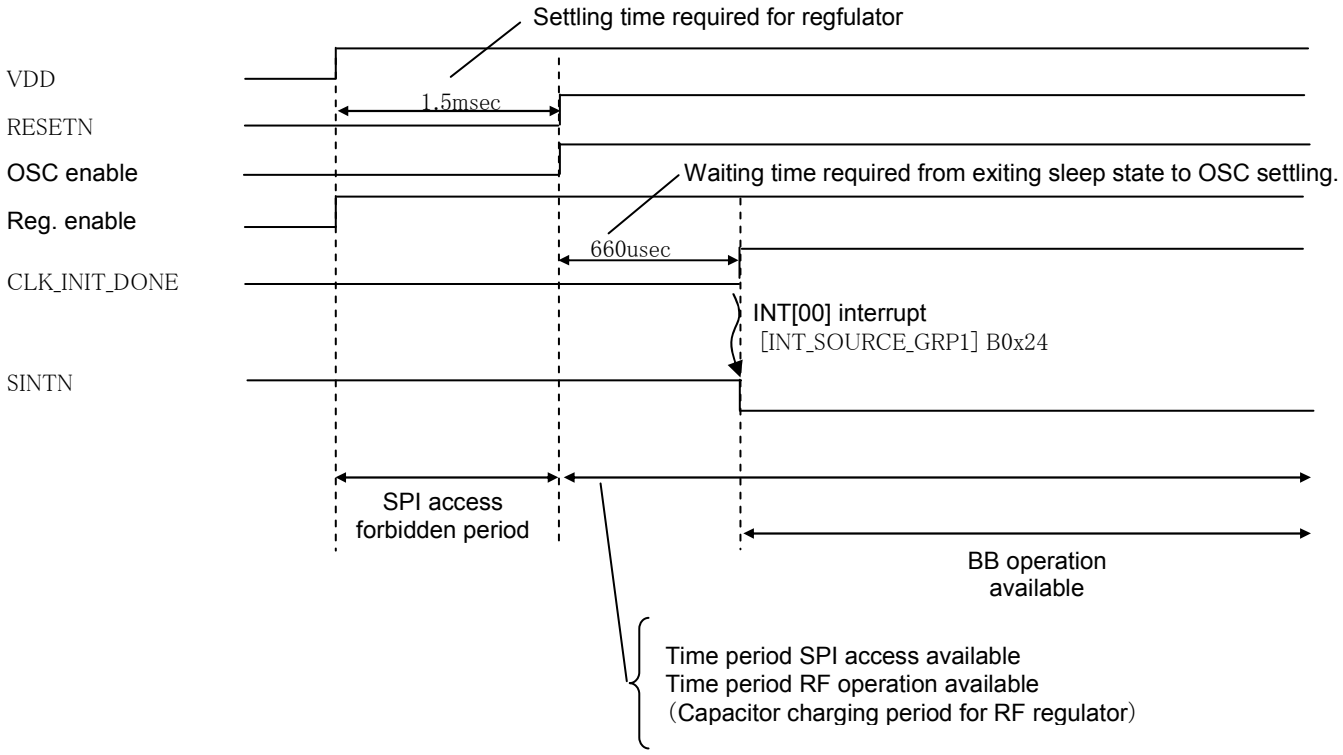
T.B.D.

■TIMING CHART

Timing chart of major operation mode is shown.

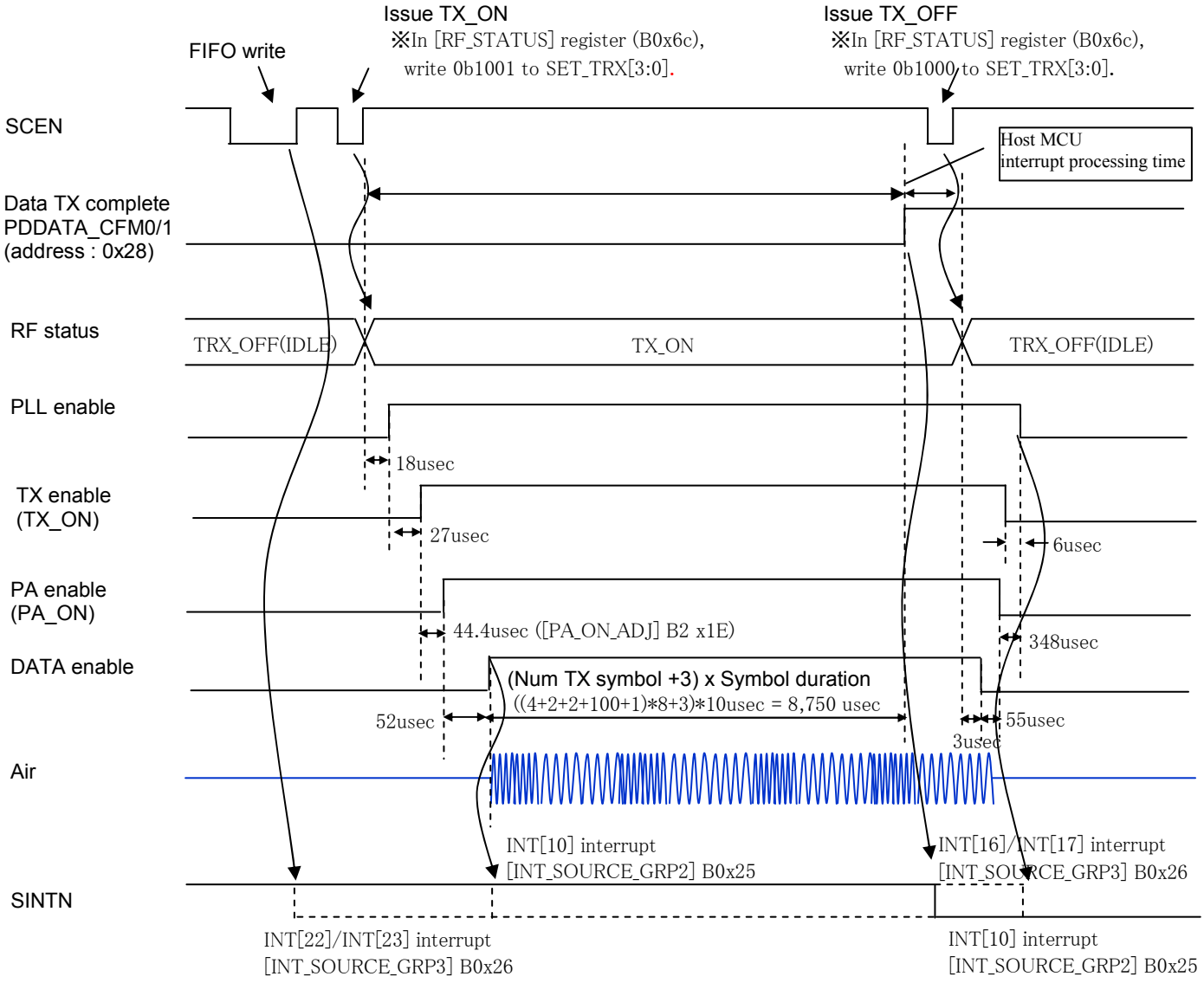
[Notes]
Bold signal indicates input or output pins, others indicate intenal signal or internal status

●Start up



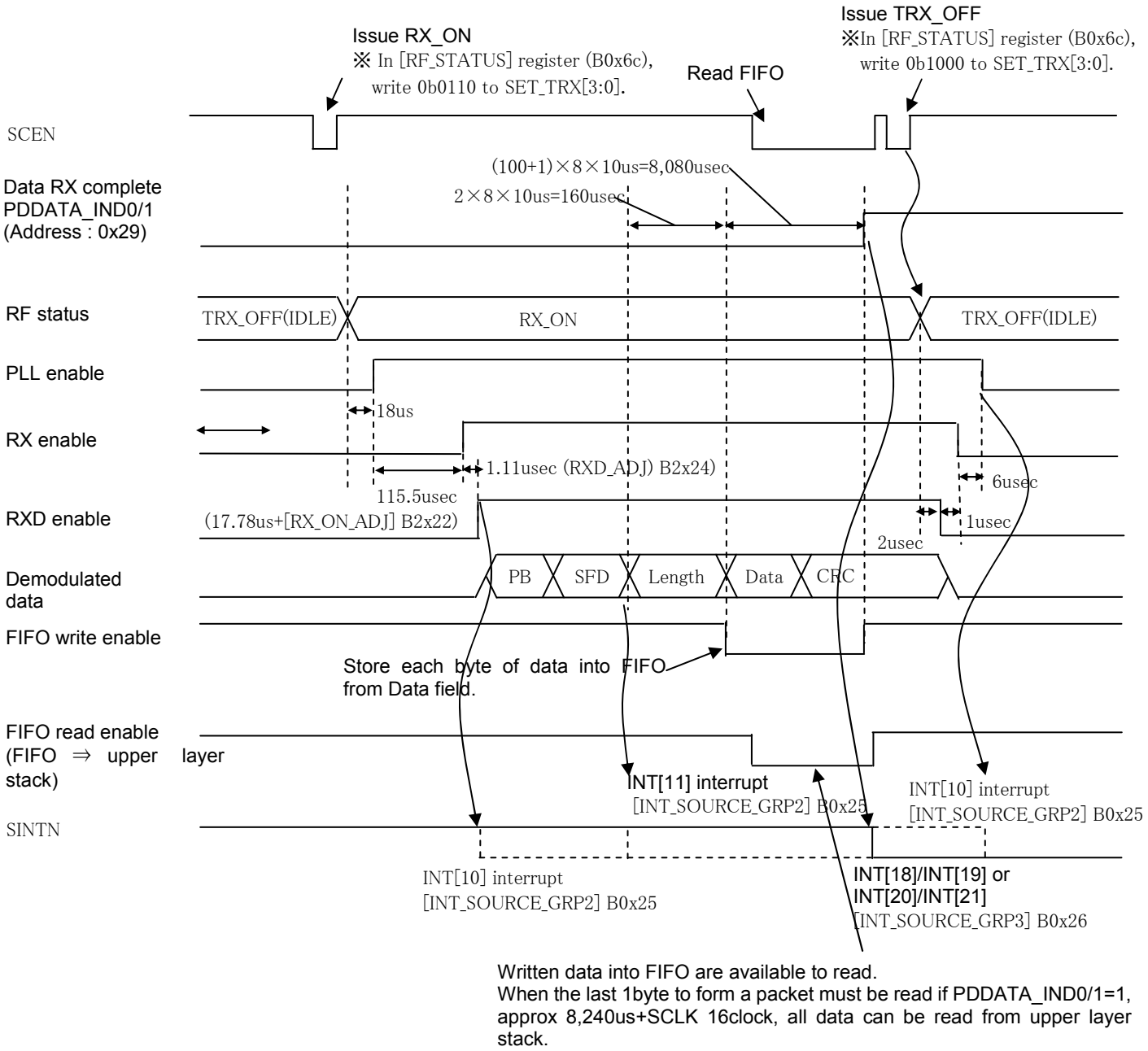
●TX mode

Conditions
・Symbol rate : 100kbps
・Preamble length : 4Byte
・SFD length : 2Byte
・Length : 2Byte
・CRC : 8bit(1Byte)
・Data length : 100Byte
・Lamp control function : On
* Lamp control timing can be adjusted by the following registers.
B0 0x6E/B1 0x3F/B1 0x55(for details, see the lamp control function.)



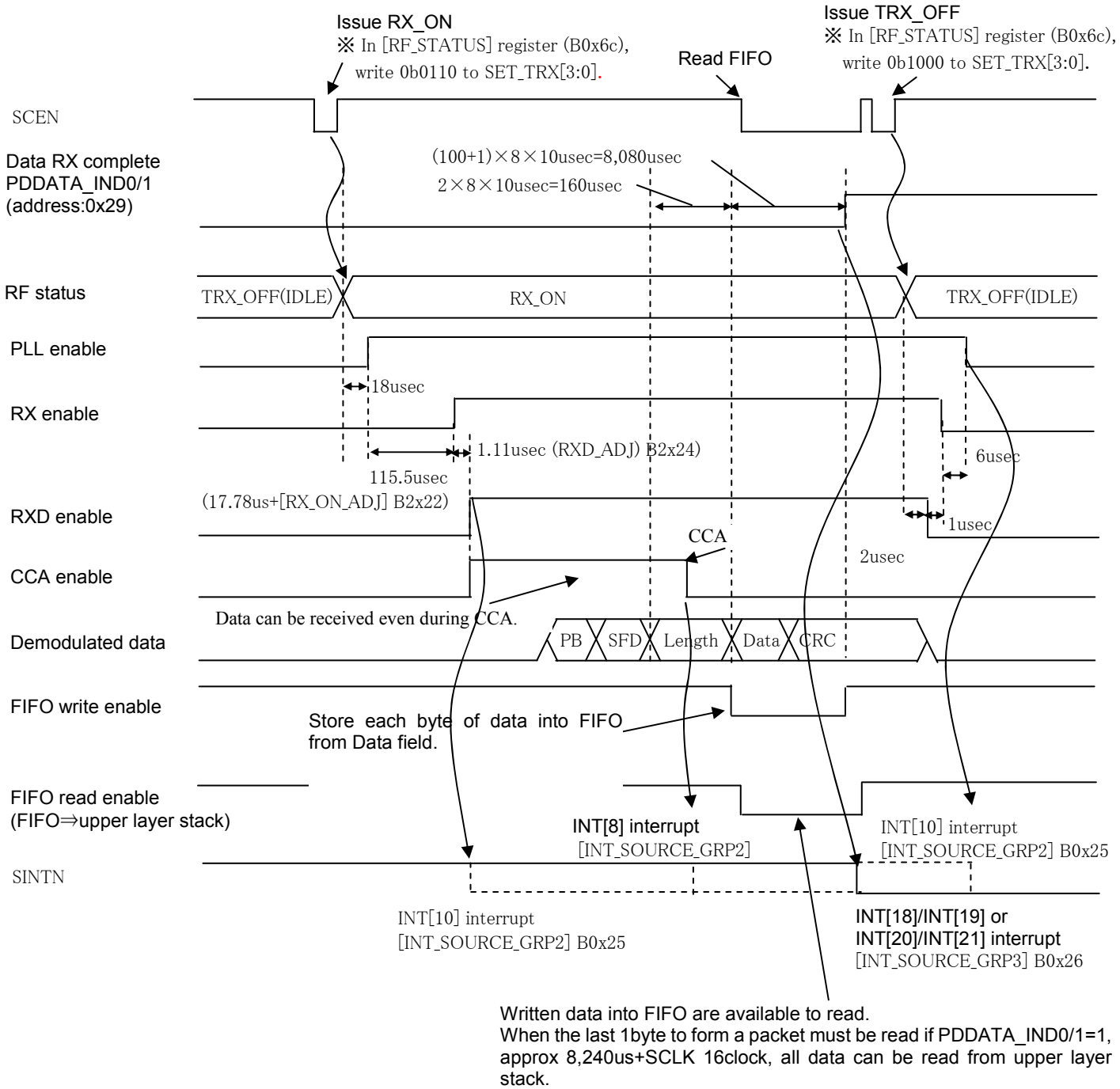
●RX mode (without CCA)

Conditions
・Symbol rate : 100kbps
・Preamble length : 4Byte
・SFD length : 2Byte
・Length : 2Byte
・CRC : 8bit(1Byte)
・Data length : 100Byte
・Lamp control function : On



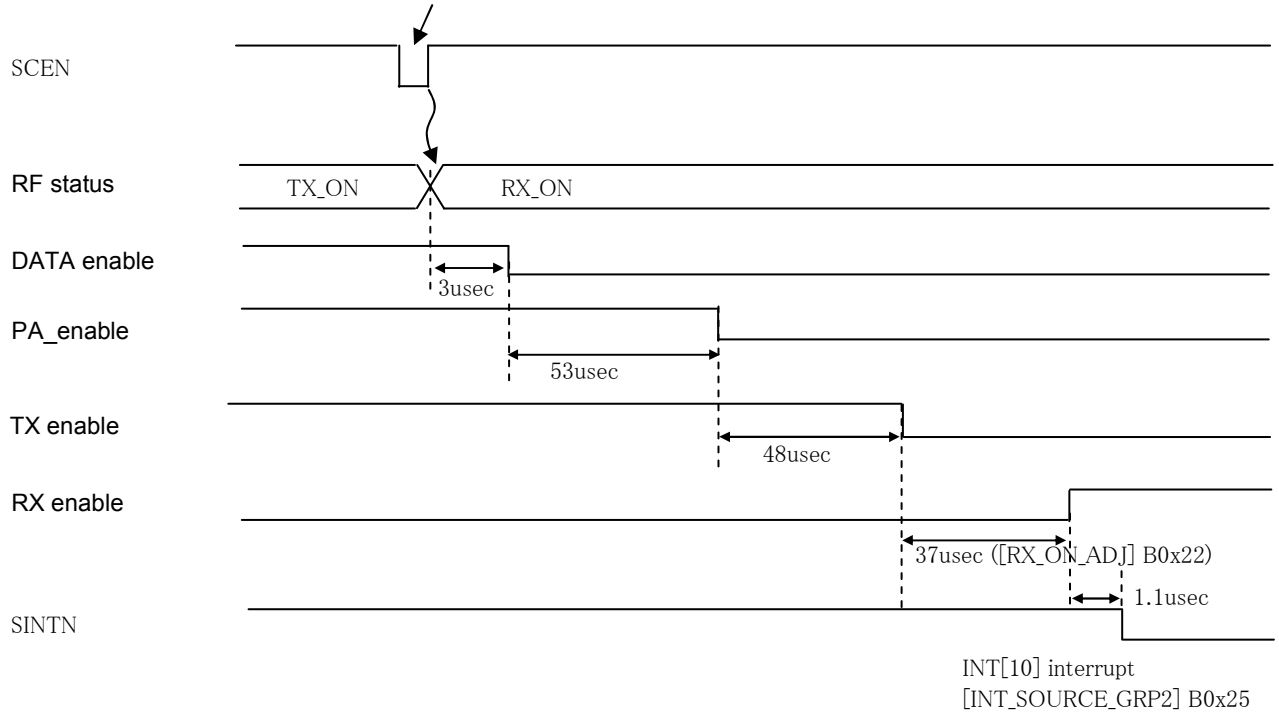
●RX mode (with CCA)

Conditions
・Symbol rate : 100kbps
・Preamble length : 4Byte
・SFD length : 2Byte
・Length : 2Byte
・CRC : 8bit(1Byte)
・Data length : 100Byte
・Lamp control function : On



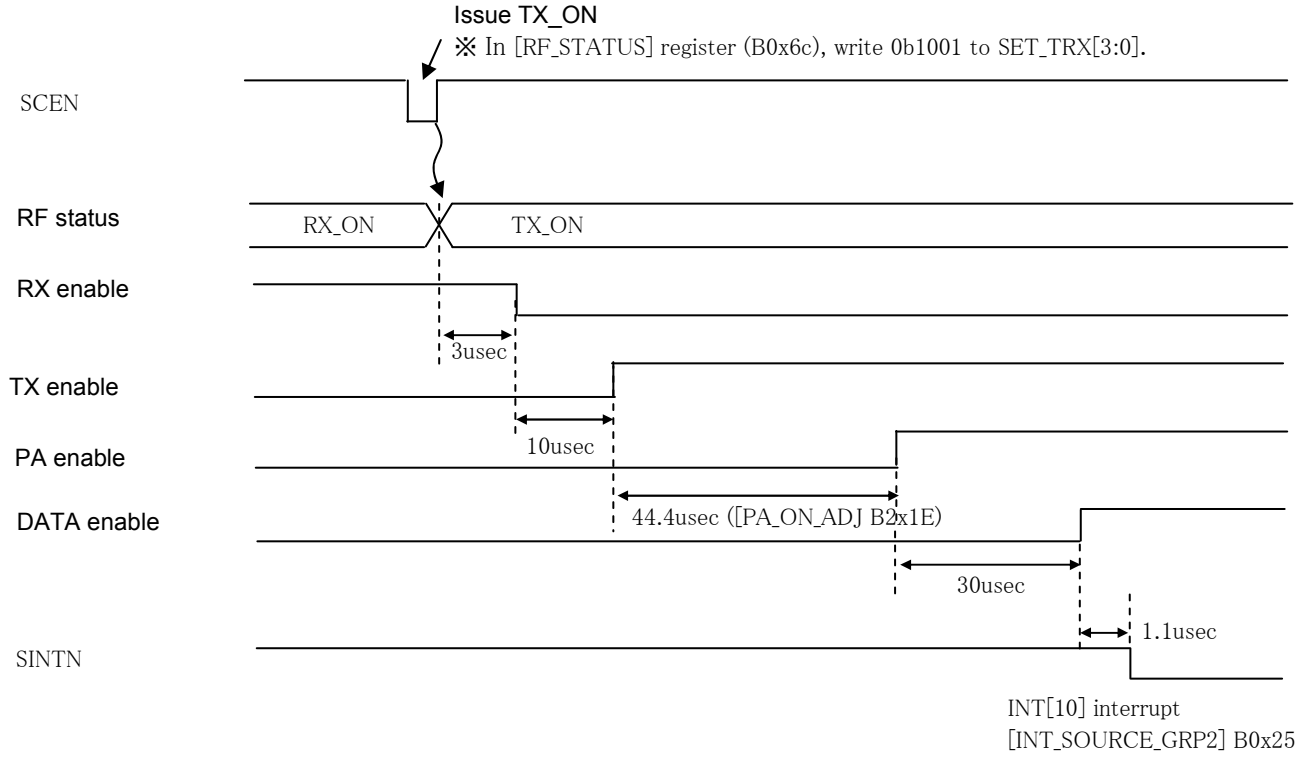
●TX mode => RX mode

Condition:
・Lamp control function : On



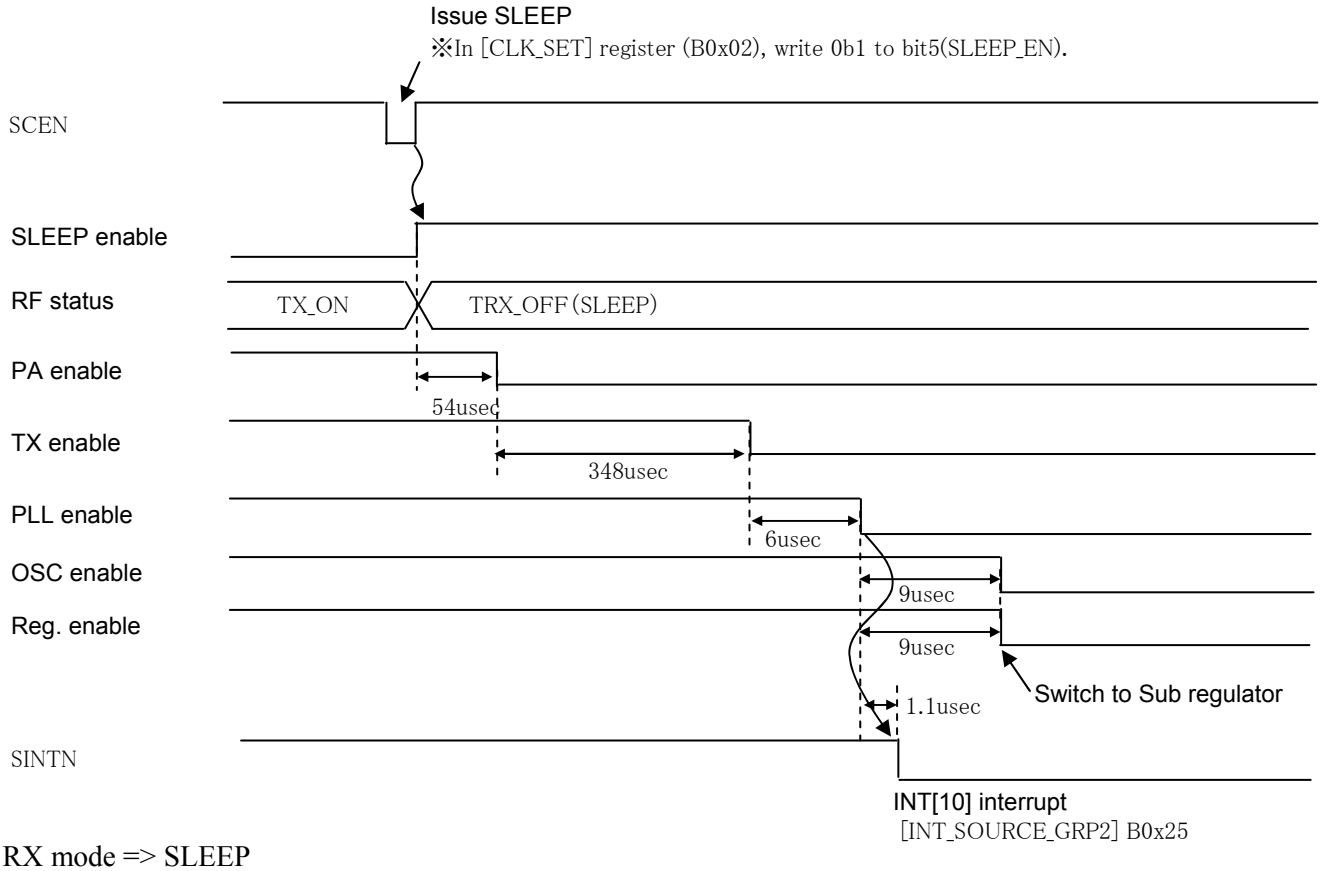
●RX mode => TX mode

Condition:
・Lamp control function : On



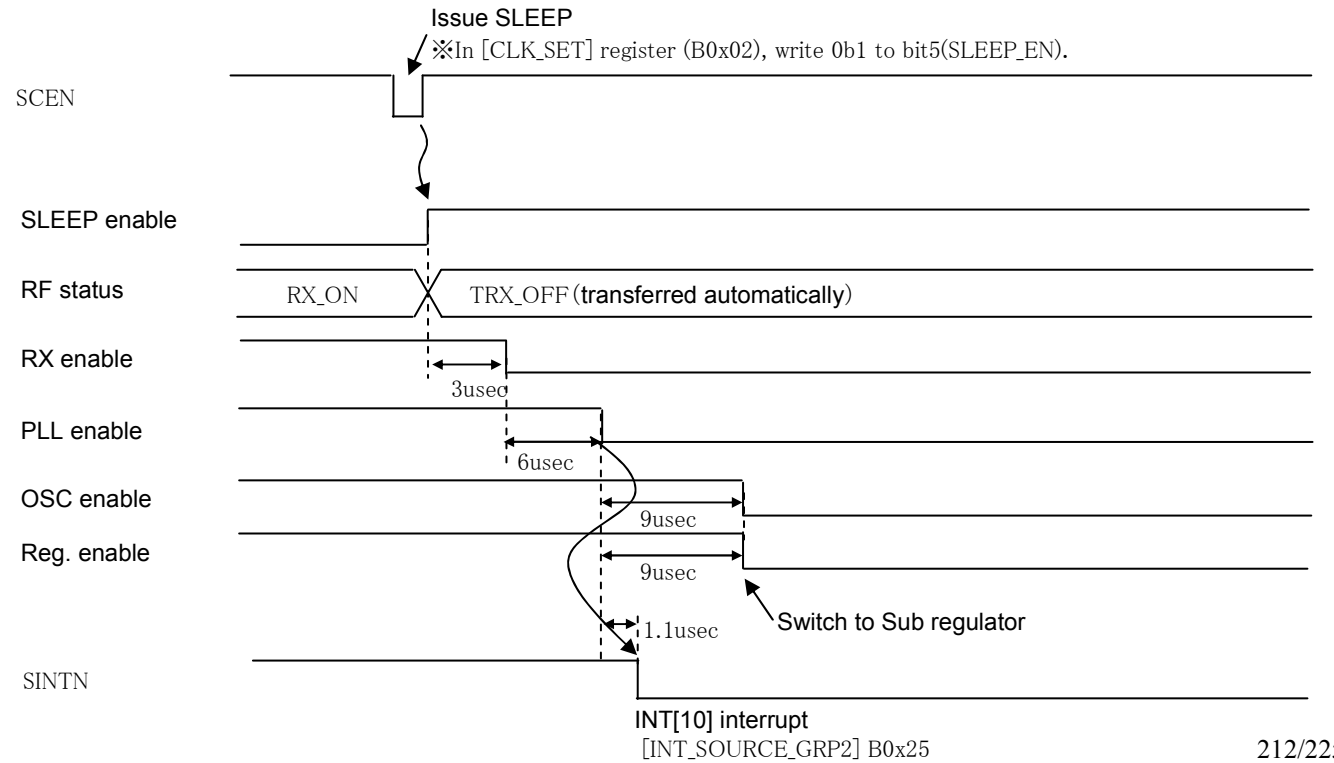
●TX mode => SLEEP

Condition:
・Lamp control function : On

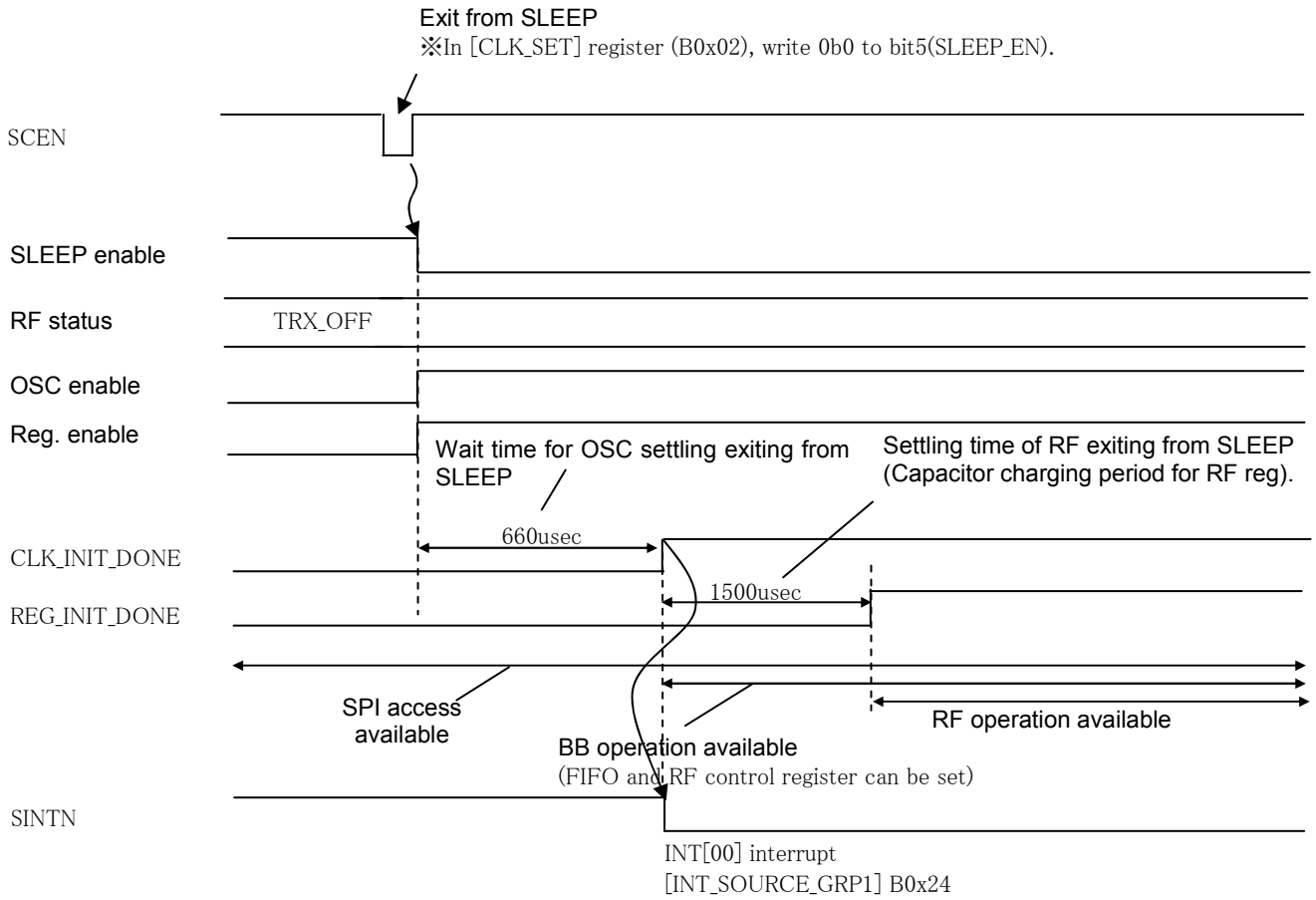


●RX mode => SLEEP

Condition:
・Lamp control function : On

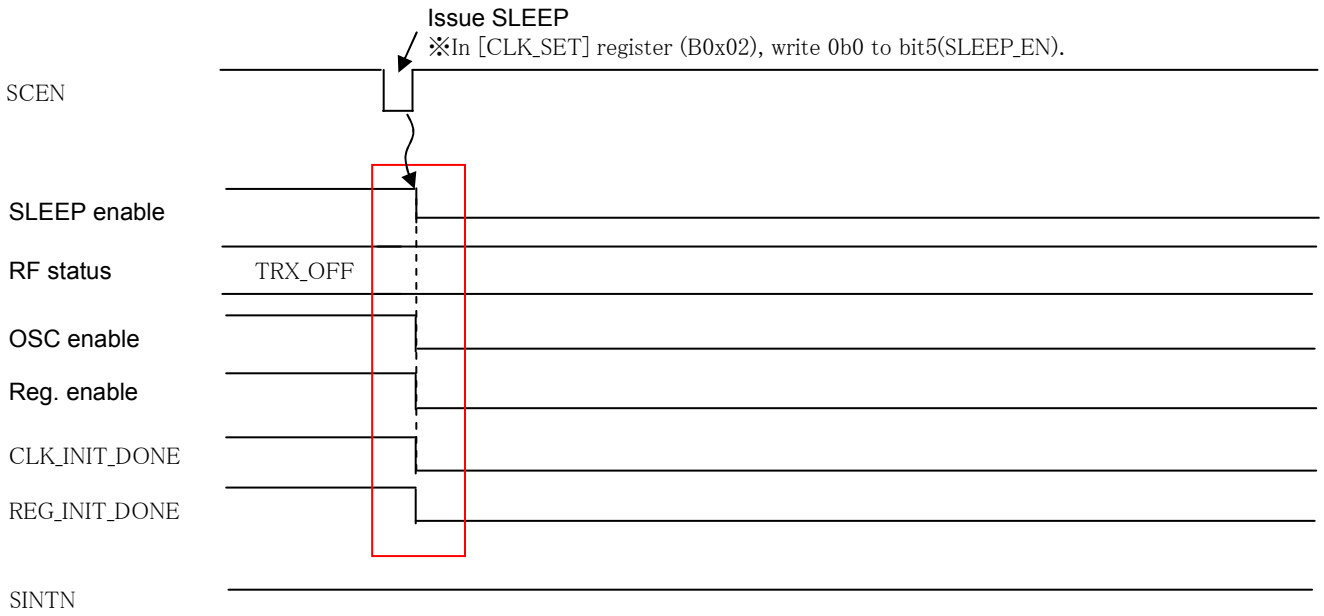


●SLEEP => IDLE



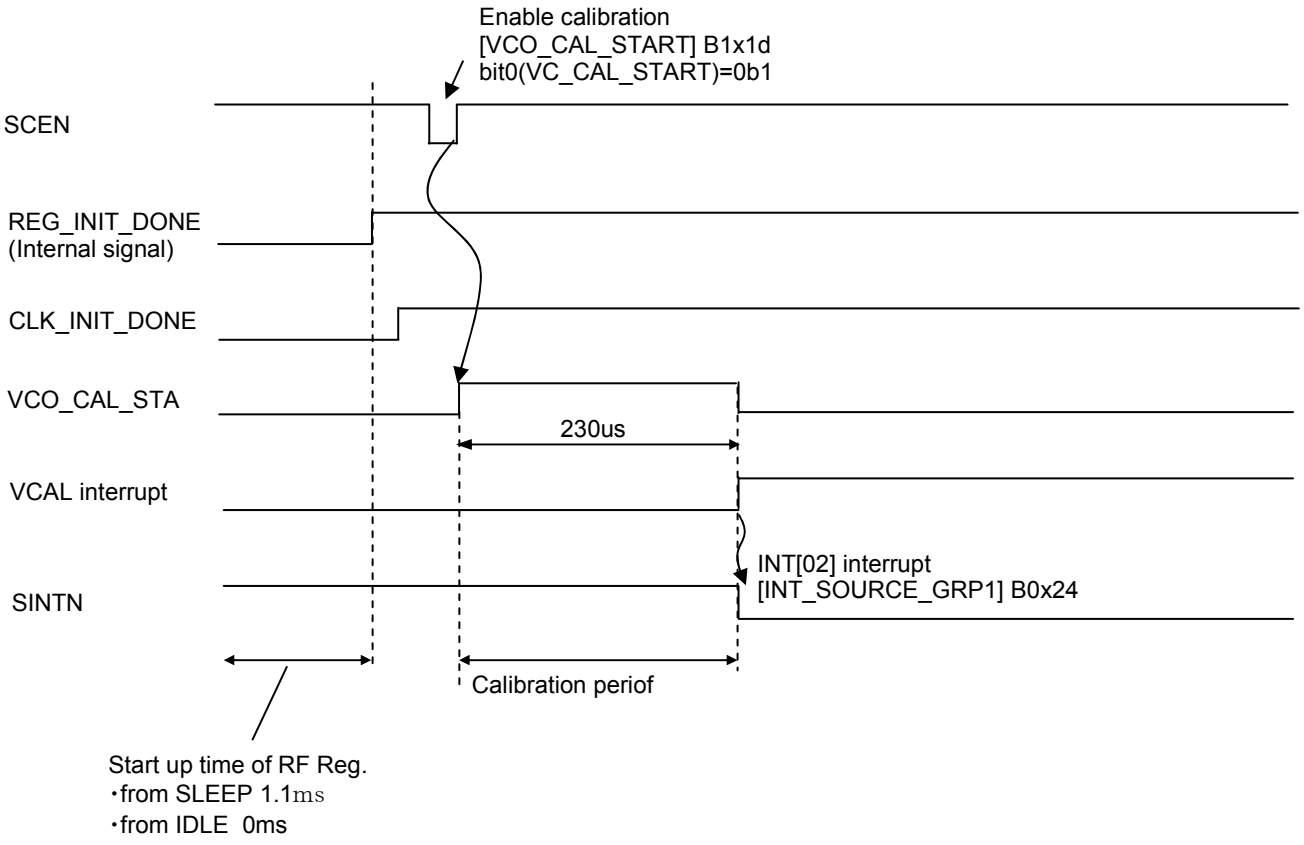
[Note] Input TCXO (clock) before issuing SLEEP release instruction when using TCXO. If TCXO is input after issuing SLEEP release instruction, the start time delays for a certain time.

●IDLE => SLEEP



[Note] If you want to stop clock when using TCXO, wait for 4us or longer after issuing SLEEP execution instruction before stopping TCXO (clock) input.

●VCO Calibration



■ABOUT FCC SUPPORT

ML7396A (915MHz band) complies with FCC PART 15. PART 15.249 is applied for a -1dBm or less output power, and PART 15.247 for +30dBm or less. PART 15.209 is applied for unnecessary spurious emission.
PART 15.247 requires the wideband modulation by the frequency hopping or digital modulation. For details on the frequency hopping and the wideband modulation, see "About frequency hopping" below and a separate sheet "ML7396 Family - Initial Setting Registers", respectively.

○About frequency hopping (FHSS: Frequency Hopping Spread Spectrum)
This LSI supports the spectral dispersion by the frequency hopping (FHSS: Frequency Hopping Spread Spectrum).
FCC (United States radio act) Part 15.247 regulates that 50 hopping channels or more are required if 20dB bandwidth is smaller than 250kHz and 25 channels or more otherwise. It also regulates that the occupation time for one channel is limited to 400msec at a maximum.
The following examples show how to control and set registers in order to comply with these regulations.
For details on register settings, also see the separate sheets "ML7396 Family - Initial Setting Registers" and "ML7396 Family - Frequency Table."

・To change the frequency from TX_ON
(0) Complete transmission (TX_ON)
(1) Transition to TRX_OFF or RX_ON (SET_TRX(Bank0:0x6C))
(2) Switch the frequency (CH0_F(Bank0:0x48,0x49,0x4a))
(3) Transition to TX_ON and transmit data (SET_TRX(Bank0:0x6C))
Repeat (0) to (3).

•To change the frequency from RX_ON
(0) Complete reception (RX_ON)
(1) Disable PLL unlock detection interrupt (INT_EN[25](Bank0:0x2D))
(2) Switch the frequency (CH0_F(Bank0:0x48,0x49,0x4a))
(3) Wait for 100usec PLL lock time
(4) Clear the PLL unlock detection interrupt (INT25(Bank0:0x27)), enable the interrupt (INT_EN[25](Bank0:0x2D))
(5) Receive data
Repeat (0) to (5).
* PLL unlock (INT25(Bank0:0x27)) may be detected when the frequency is switched.
(1)As shown in (1) to (4), it is recommended to disable the PLL unlock detection interrupt for 100usec after the frequency is switched.

The following examples show how to control the frequency hopping.

•Control example 1. The sender transmits a long term preamble, and the receiver scans channels for a preamble

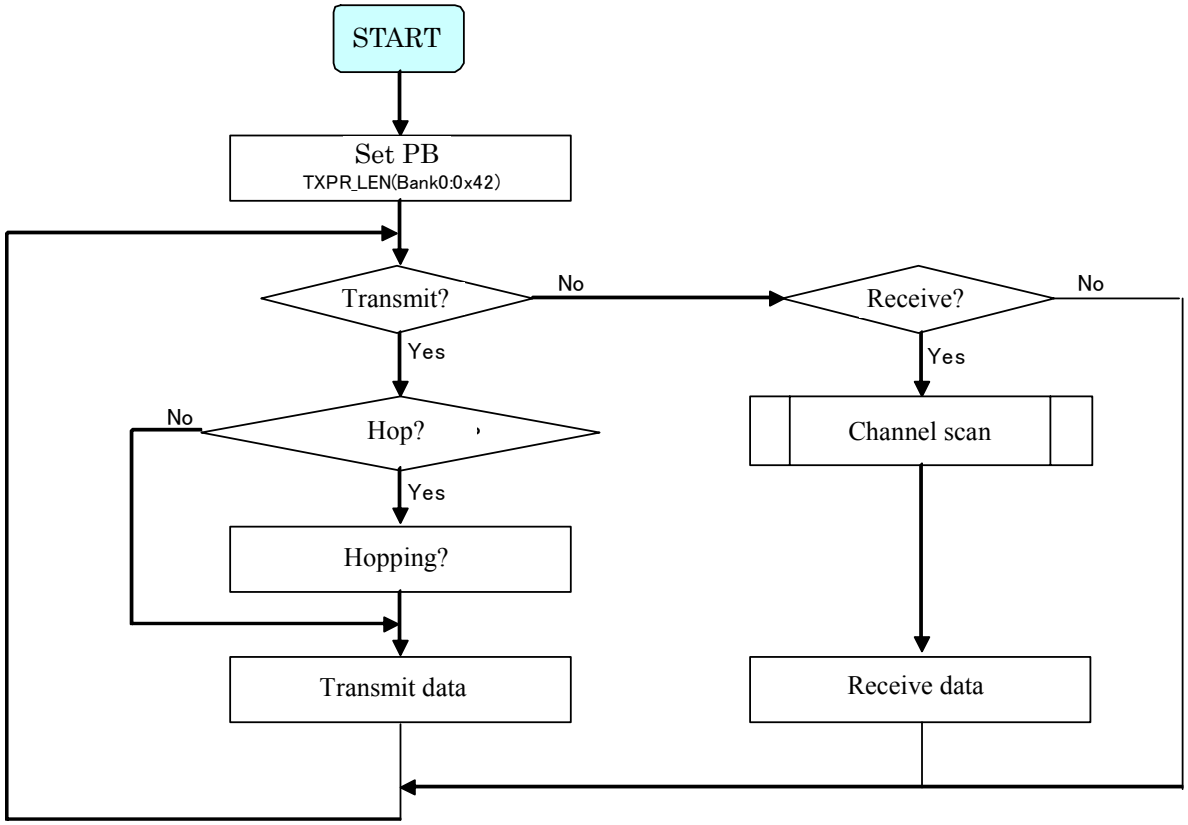
The sender hops the frequency according to any hopping regulation. The occupation time for one channel complies with the regulation which specifies 400ms at a maximum.
The receiver does not know which channel the sender uses to transmit a preamble, and so scans all channels for it (channel scan).
The sender needs to transmit a preamble for a longer period than the channel scan period on the receiver side. For details on the channel scan, see the flow chart of the channel scan shown later.
The preamble length can be set by TXPR_LEN(Bank0:0x42). (Max.255byte)
The time required for one channel scan is calculated by "preamble detection period (36bit / transmission rate) + PLL lock period (100usec)."
The following table shows the channel scan period for each transmission rate. See the following table to set an appropriate value for the preamble length.

Table.Channel scan period by transmission rate

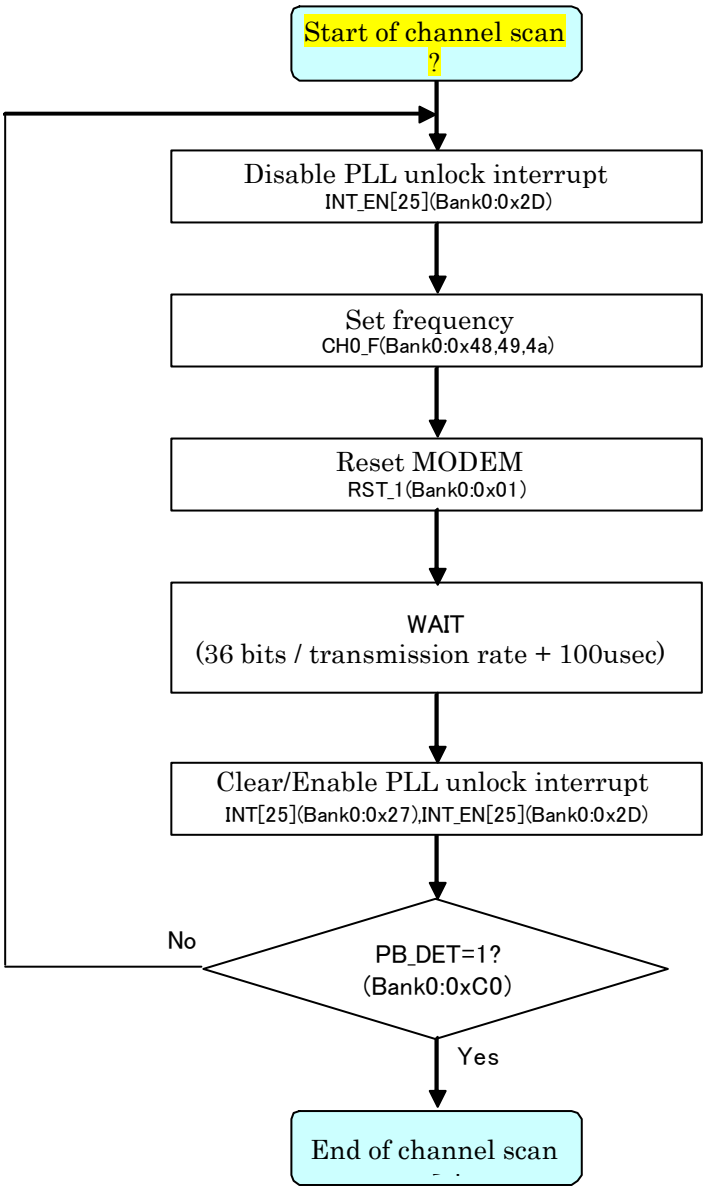
Transmission rate [kbps]	Transmit PB period (maximum) [ms]	Required period for one channel [ms]	Required period for all channels [ms]		Availability	
			25ch	50ch	25ch	50ch
10	204.0	3.70	92.5	185.0	○	○
20	102.0	1.90	47.5	95.0	○	○
40	51.0	1.00	25.0	50.0	○	○
50	40.8	0.82	20.5	41.0	○	×
100	20.4	0.46	11.5	23.0	○	×
150	13.6	0.34	8.5	17.0	○	×
200	10.2	0.28	7.0	14.0	○	×
400	5.1	0.19	4.8	9.5	○	×

* This table do not consider the time for register access.
* Under conditions where "Availability" is shown as "×," this control method cannot be applied because the period required for scanning all channels exceeds the send PB period.

Here is the flow chart of the control example 1.



Here is the flow chart of the channel scan.

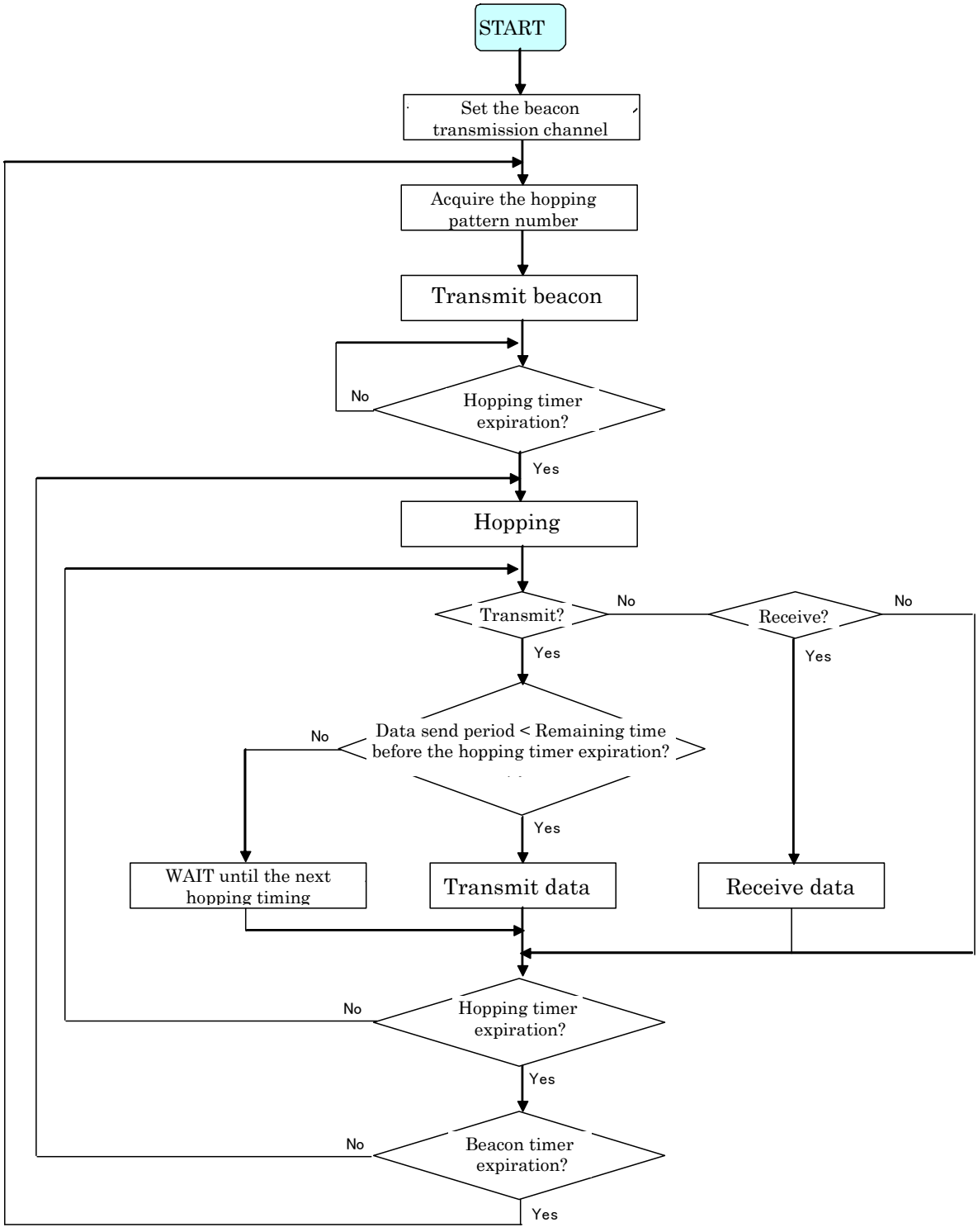


・Control example 2. Transmission and reception nodes synchronize with beacon and use the common hopping rule for hopping

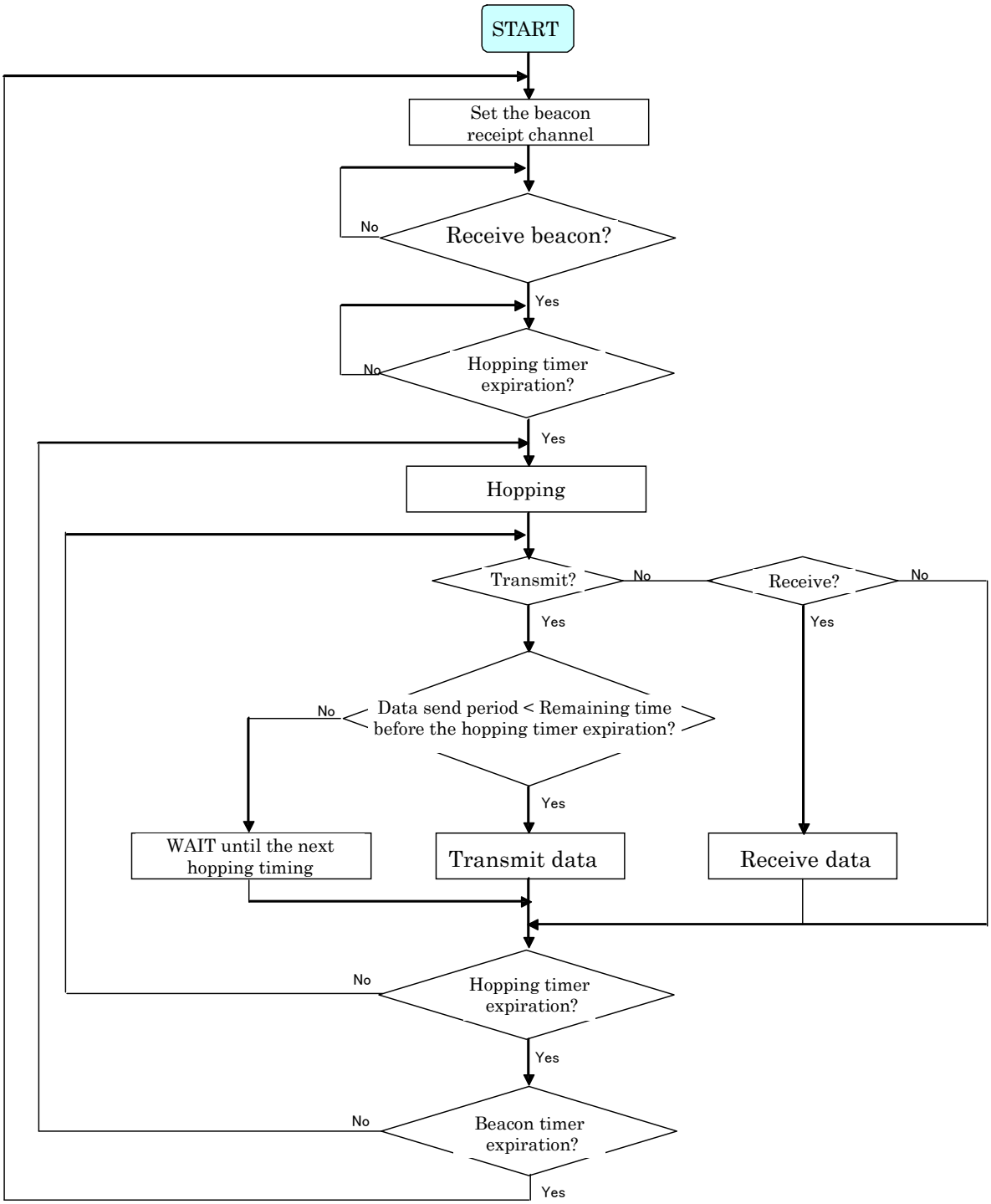
In this control example 2, the parent and child nodes use the same synchronized hopping rule for frequency hopping.
The parent node issues a beacon for synchronization regularly to synchronize the hopping pattern with the child node. The child node receives the beacon issued by the parent node regularly to synchronize the hopping pattern. To ensure synchronization, a fixed beacon frequency is used.
The child node waits for a beacon at the defined frequency. Once synchronized, the child and parent nodes use the common hopping pattern for frequency hopping. The hopping interval should be the beacon period divided by the number of hopping channels and 400ms at a maximum. The sender calculates the send period from the data length, making sure to avoid spanning hopping intervals.
The parent and child nodes should provide multiple common hopping patterns which have sequential numbers (pattern number) added in advance. The parent node includes the pattern number information in a beacon.
This hopping method is available regardless of the transmission rate, the diversity search setting, and the number of hopping channels.

Here is the flow chart of the control example 2.

[Parent node]



[Child node]

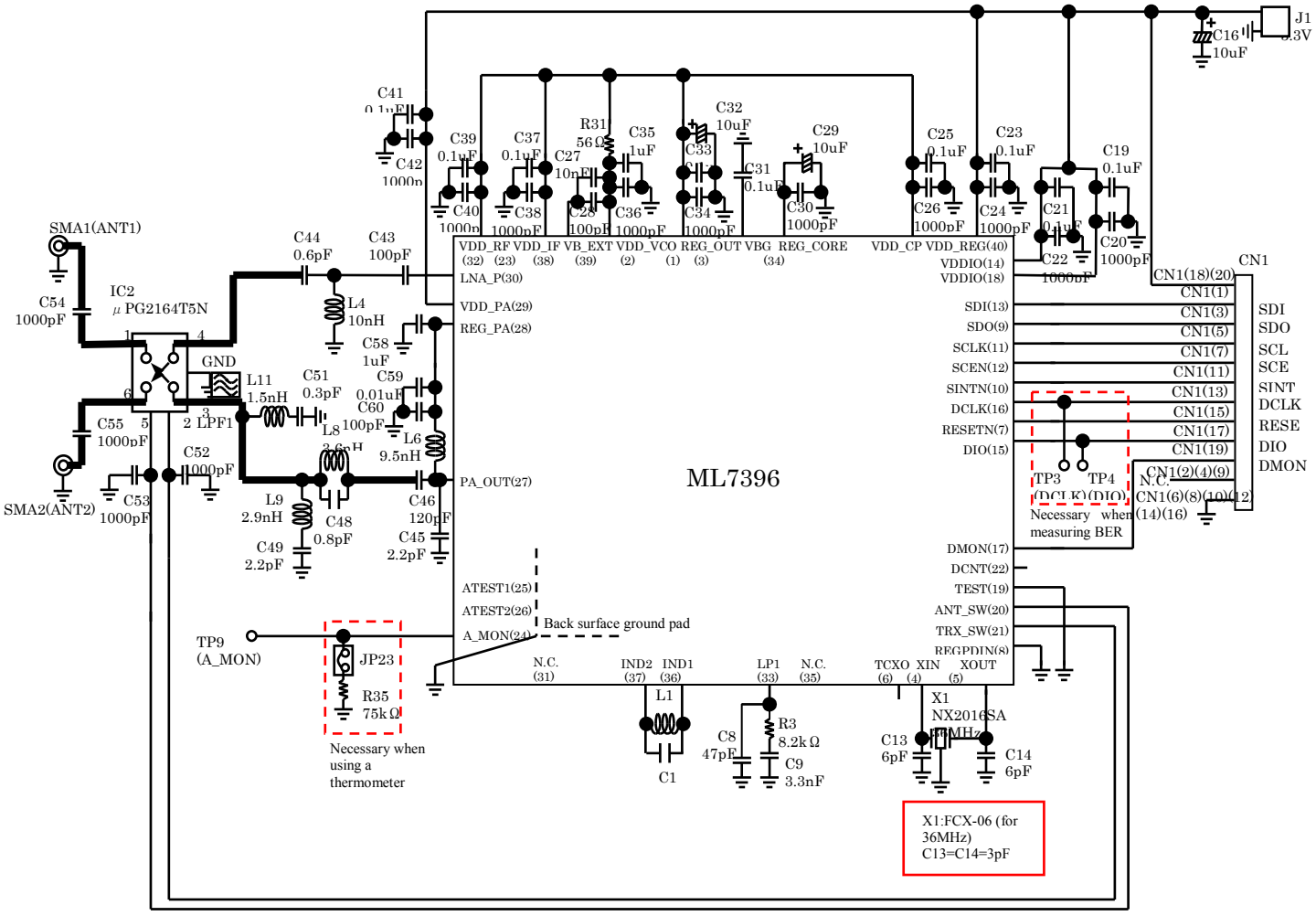

START
Set the beacon receipt channel
Receive beacon?
No
Yes
Hopping timer expiration?
No
Yes
Hopping
Transmit?
No
Receive?
No
Yes
Yes
Data send period < Remaining time before the hopping timer expiration?
No
Yes
WAIT until the next hopping timing
Transmit data
Receive data
Hopping timer expiration?
No
Yes
Beacon timer expiration?
No
Yes

■APPLICATION CIRCUIT EXAMPLE

Here is a circuit example for 915MHz/920MHz, 13dBm, and up to 200kbps.

The pin for the 3.3V power supply voltage should be a common connection with a bypass capacitor of 10uF inserted.

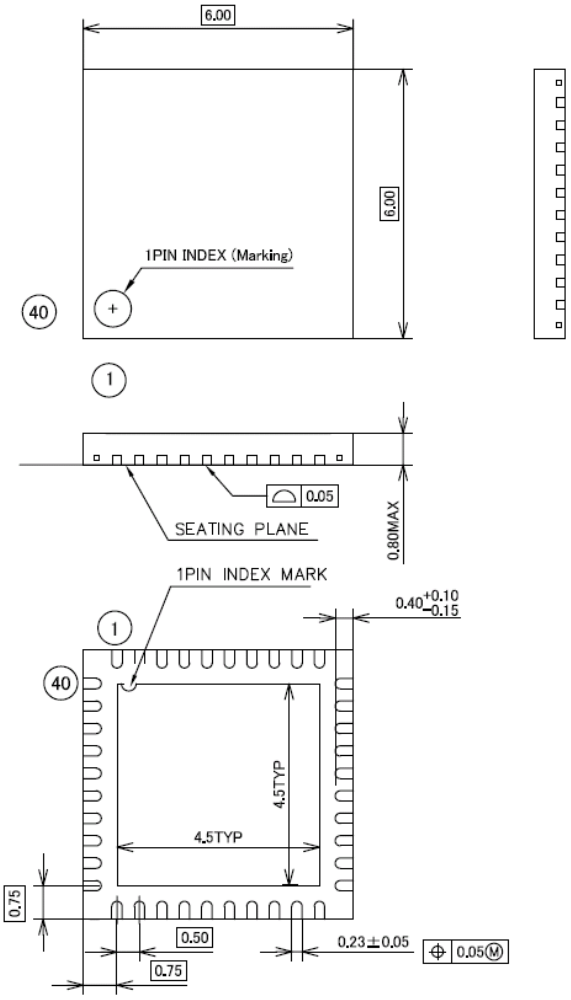
LQW15 from MURATA manufacturing co., ltd. is recommended.

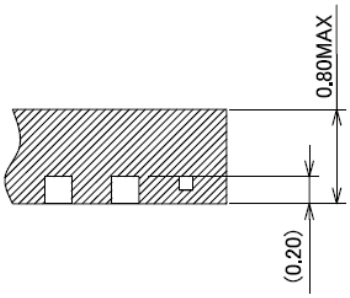


	915MHz	920MHz
L1	4.3nH	3.9nH
C1	3.9pF	4.3pF
LPF1	DEA1609 15LT-50 38A (TDK)	0Ω

Application circuit is shown as example; please contact sales representative or distributor for more details

■PACKAGE DIAGRAM





注）
1. 本寸法は、パッケージ反りを含む寸法である。
2. SEATING PLANEとは、パッケージを取り付ける面に対して、
パッケージが接触し合う面である。

NOTE
1. THESE DIMENSIONS INCLUDE PACKAGE WARPAGE.
2. THE SEATING PLANE IS THE SURFACE WHICH THE
PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

Remarks for surface mount type package

Surface mount type package is very sensitive affected by heating from reflow process, humidity during storaging Therefore, in case of reflow mouting process, please contact sales representative about product name, package name, number of pin, package code and required reflow process condition (reflow method, temperature, number of reflow process), storage condition.

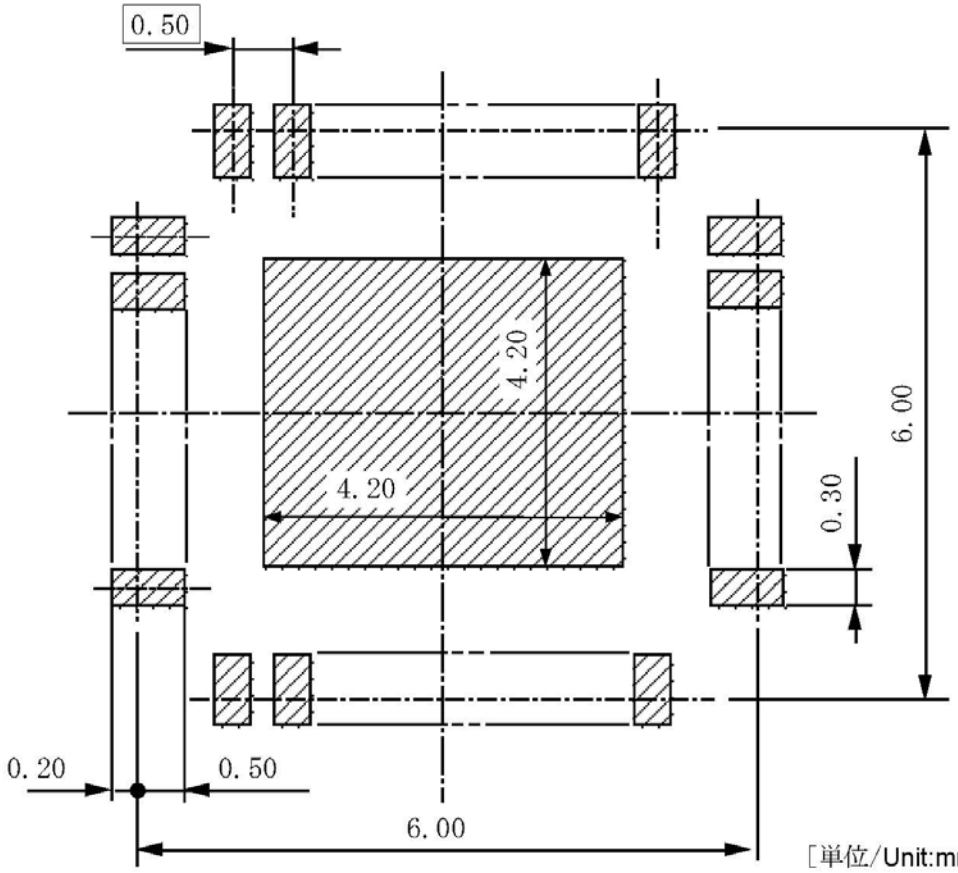
■REFERENCE FOOTPRINT PATTERN (RECOMMENDATION)

P-WQFN40-0606-0.50-63

参考図
for reference

半田付け部端子存在範囲図

Mounting area for package lead soldering to PC boards



実装基板のフットパターンの設計の際には、実装の容易さ、接続の信頼性、配線の引き回し、半田ブリッジ発生のないことなどを十分考慮してください。

フットパターンの最適な設計は基板材質、使用する半田ペースト種類、厚み、半田付け方法などによって変わってきます。従って、本パッケージの端子の存在し得る範囲を「半田付け部端子存在範囲図」として示しますので、フットパターン設計の参考資料としてください。

When laying out PC boards, it is important to design the foot pattern so as to give consideration to ease of mounting, bonding, positioning of parts,reliability, wiring,and elimination of solder bridges.

The optimum design for the foot pattern varies with the materials of the substrate,the sort and thickness of used soldering paste,and the way of soldering. Therefore when laying out the foot pattern on the PC boards, refer to this figure which mean the mounting area that the package leads are allowable for soldering to PC boards.

■REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7396A_B_E-01	2013.02.27	–	–	Initial release

■NOTES

No copying or reproduction of this document, in part or in whole, is permitted without the consent of LAPIS Semiconductor Co., Ltd.
The content specified herein is subject to change for improvement without notice.
The content specified herein is for the purpose of introducing LAPIS Semiconductor's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from LAPIS Semiconductor upon request.
Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.
Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, LAPIS Semiconductor shall bear no responsibility for such damage.
The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. LAPIS Semiconductor does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by LAPIS Semiconductor and other parties. LAPIS Semiconductor shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.
The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).
The Products specified in this document are not designed to be radiation tolerant.
While LAPIS Semiconductor always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.
Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. LAPIS Semiconductor shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.
The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). LAPIS Semiconductor shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.
If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.