ML7344C/E/J Preliminary

Sub-GHz(168MHz to 510MHz) band short range wireless transceiver IC

■GENERAL DESCRIPTION

ML7344C/E/J is a narrow band sub-GHz IC that integrates RF part, IF part, MODEM part and HOST interface part in single-chip. It supports various frequency band from 168MHz to 510MHz. ML7344C can output 100mW (20dBm) transimittion power and it suits for the smart-meter in Chinese market. ML7344E is suitable for Fmode (434MHz) or N mode (168MHz) of Wirelss Mbus system. ML7344J is suitable for security radio system type III or IV of the RCR STD-30 and specified low-power radio station in 426 MHz operation of the ARIB STD-T67.

■FEATURES

- Frequency Range: 168 – 510MHz
- ML7344C is able to use as communication unit of Q_GDW374.3 (China)
  ML7344E is able to use as F mode or N mode of the wirelss M-bus system.
  ML7344J is able to use as type III or IV security radio of RCR STD-30 and ARIB STD-T67 in 426 MHz operation. (Japan)
- High accurate modulation implemented by direct modulation scheme using fractional-N PLL.
- Multiple modulation scheme : GFSK/GMSK, FSK/MSK
- Configurable data ratres from 1.2kbps to 15 kbps
- Supports NRZ code, Manchester code and 3 out of 6 code.
- Programmable modulation frequency deviation
- Polarity conversion for TX and RX data bits
- On chip 26MHz oscillation circuit implemented (ML7344xC x=C, E or J)
  Supports 26MHz TCXO input. (ML7344xT, x=C, E or J)
  Support 26MHz SPXO (C-MOS level) input (ML7344xS x=C,E or J)
  Note: The ordering product name is different from supporting clock source.
- On chip RC 32kHz oscillation circuit.
- Oscillation frequecy tuning function implemented. (ML7344xC x=C, E or J)
- Frequency tuning function (frequency fine tuning by oscillation circuit and fractional-N PLL)
- Built in Power Amp (PA) and power control function
  Programmable from 100mW, 20mW and 10mW (ML7344C)
  Programable from 20mW,10mW and 1mW (ML7344E/J)
- Fine output power tuning function implemented. (Tune ±0.2dB)
- TX ramp control function implemented
- Support external PA
- Receive Signal Strength Indicator (RSSI) reporting function and threshold comparison function
- Built-in AFC function
- Synchronous serial peripheral interface (SPI)
- Auto wake-up and auto sleep function are implemented
- 2 genral purpose timers are implemented
- Test Pattern generation (PN9, CW, 0/1, all-1, all-0 pattern)

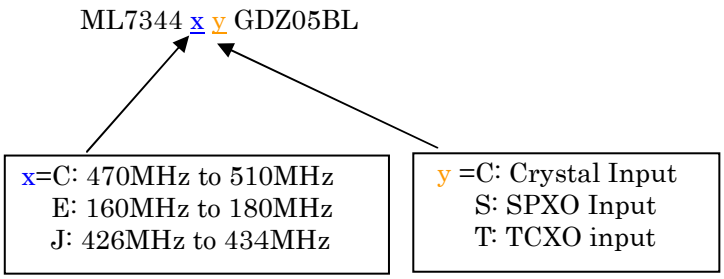
- Packet mode function
  - Support 2 wireless M-bus packet format. (Format A and B)
  - Support general packet format (Format C)
  - Max packet length 255 bytes（Format A and B）and 2047 bytes (Format C）
  - 64 byte TX and RX buffer are implemented
  - Preamble pattern detection function (Preamble length can be prgrammable between 1 to 4 Byte）
  - Programmable TX preamble length（Max 16383 Byte）
  - ID code or SFD detection function (Max 4 Byte x 2codes, available for TX and RX)
  - Progrmable CRC generate function for CRC32, CRC16 and CRC8
  - Whitenning function
  - Address filtering function
    Checking C-Fieled, M-Field and A field of wireless M-bus packet (EN13575-4:2011)

- Power supply voltage
  1.8V to 3.6V Outpur power is set at 1mW
  2.1V to 3.6V Output power is set at 10mW
  2.6V to 3.6V Output power is set at 20mW
  3.3V to 3.6V Output power is set at 100mW
- Operating temperature -40 to +85 deg.C
- Power consumption (operation at 426MHz)

Deep Sleep Mode:		0.1 uA (Typ)
Sleep Mode1		0.4 uA (Typ) (Maintain Register values)
Sleep Mode2		0.53 uA (Typ) (Maintain Register values and FIFO data)
Idle Mode		1.0 mA (Typ)
TX	100mW	73 mA (Typ.)
	20mW	28 mA (Typ.)
	10mW	26 mA (Typ.)
	1mW	6.8 mA (Typ.)
RX		6.2 mA (Typ.)

- Package
  32 pin WQFN 5.0mm x 5.0mm x 0.8mm
  Pb free, RoHS compliant

■ORDERING GUIDE



■BLOCK DIAGRAM

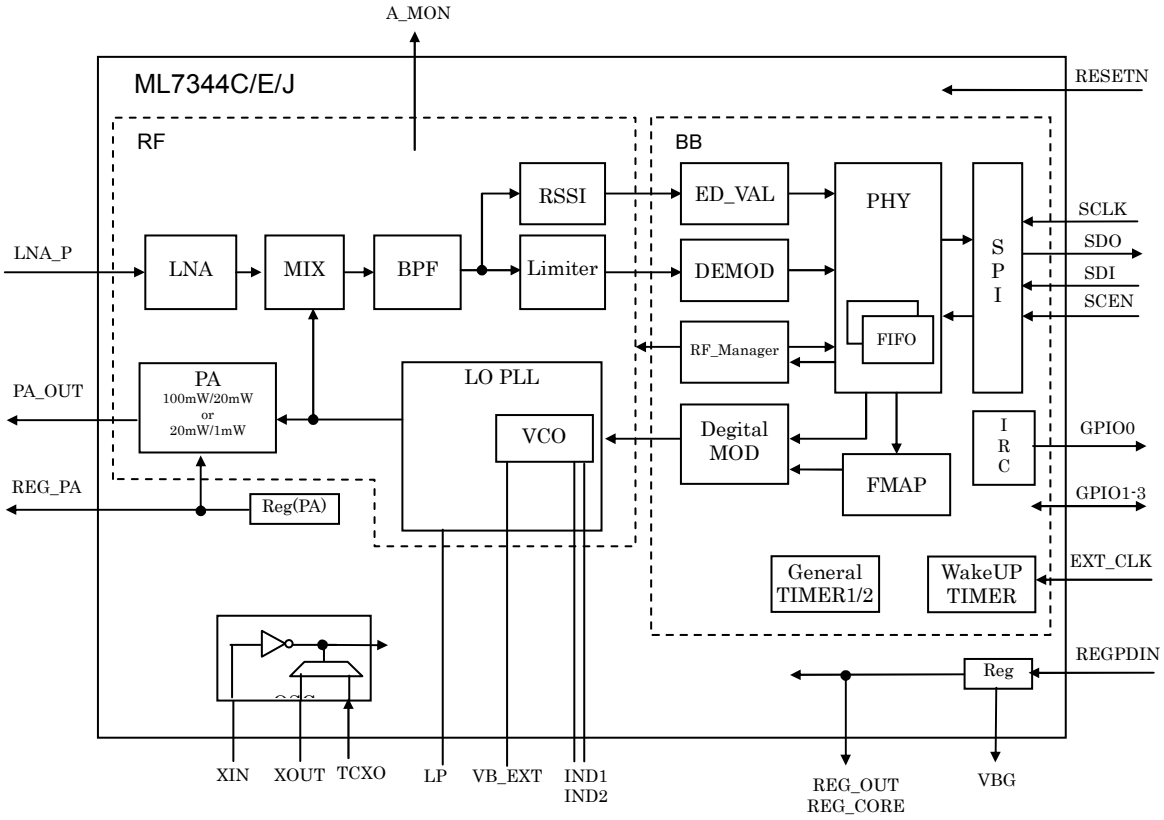


Fig.1 Block diagram

■PIN ASSIGNMENT

Package: 32pin WQFN

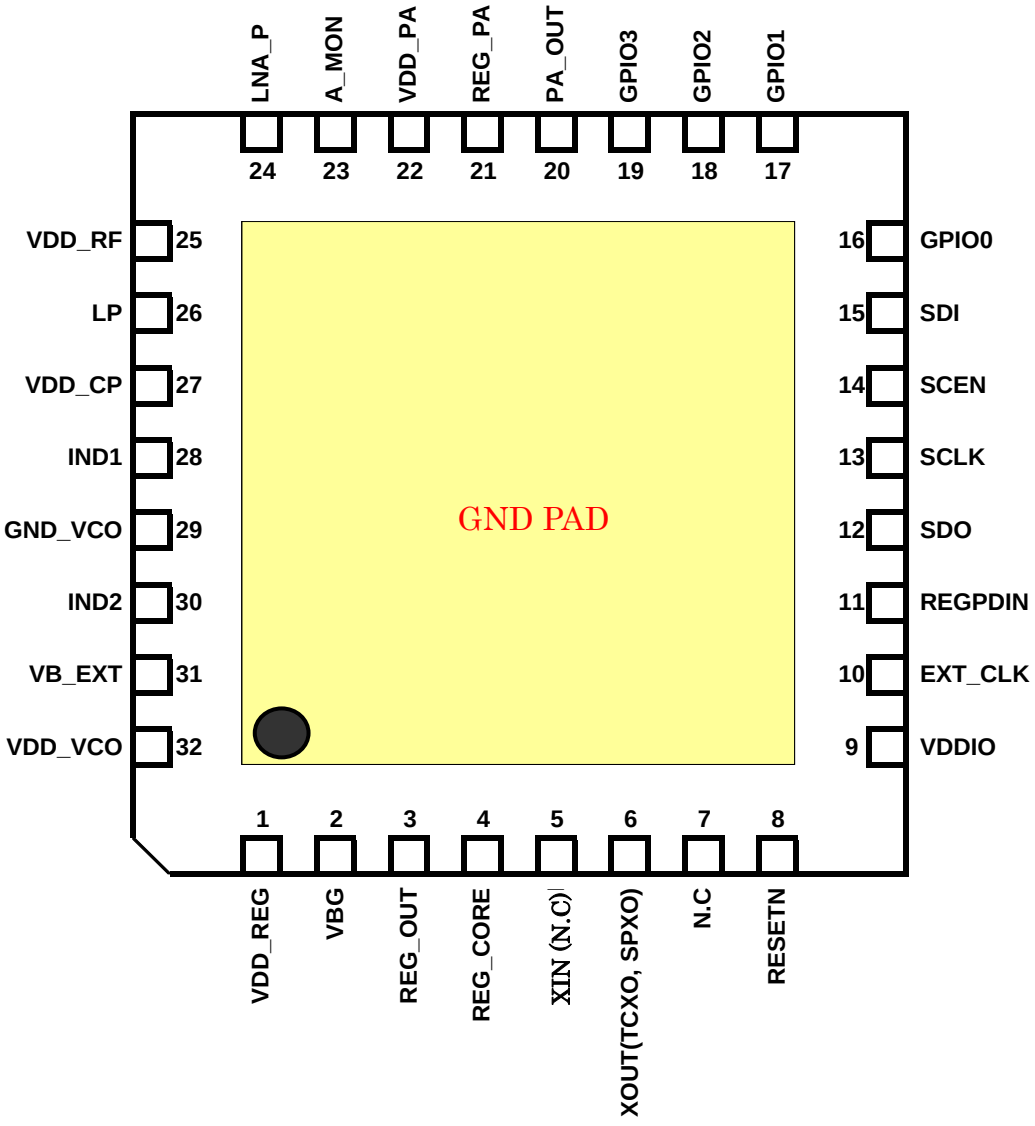


Fig.2 Pin Assignment

NOTE: Pattern shown in the centre of the chip is located at bottom side of the chip (GND PAD)

■PIN DEFINITIONS

Symbols

I_{RF} : RF input
O_{RF} : RF output
I_A : Analog input
IO_A : Analog input/output
I_{OS} : Oscillator input
O_{OS} : Oscillator output
I : Digital input
O : Digital output
Is : Schmitt trigger input
IO : Digital input/output

●RF part

Pin name	Pin No.	Direction	Active Level	State at reset	Detail function
PA_OUT	20	O_{RF}	-	O	RF antenna output
A_MON	23	IO_A		Hi-Z	Test pin. *1
LNA_P	24	I_{RF}	-	I	RF antenna input
LP	26	-	-	-	Pin for PLL loop filter
IND1	28	-	-	-/-	Pin for external inductor
IND2	30	-	-	-/-	Pin for external inductor
VB_EXT	31	-	-	-/-	Pin for a smoothing capacitor to internal bias for VCO circuit

*1 LAIPS semiconductor will use this pin for checking analog function.

●SPI interface

Pin name	Pin No.	Direction	Active Level	State at reset	Detail function
SDO	12	O	H or L	O/L	SPI data output or DCLK output (2^{nd}) *1
SCLK	13	Is	P or N	I	SPI clock input
SCEN	14	Is	L	I	SPI enable input L: Enable H: Disable
SDI	15	Is	H or L	I	SPI data input or DIO input/output (2^{nd}) *1

*1 When using as 2^{nd} functuon, please refer “DIO Function”.

●Regulator part

Pin name	Pin No.	Direction	Active Level	State at reset	Detail function
VBG *1	2	-	-	-	Pin for decoupling capacitor.
REG_OUT	3	-	-	-	Regulator output（typ.1.5V） Place a decoupling capacitor to this pin
REG_CORE *1	4	-	-	-	Monitor pin for power supply to digital core (typ.1.5V) Place a decoupling capacitor to this pin
REGPDIN	11	I	H	I	Power down pin for regulator L: When in normal use H: When in deep sleep mode
REG_PA *1	21	-	-	-	Regulator output for PA block Place a decoupling capacitor to this pin

*1 These pins will output 0V in the sleep mode

●Miscellaneous

Pin name	Pin No.	Direction	Active Level	State at reset	Detail function
XIN N.C *1	5	Ios -	P or N -	- -	26MHz crystal pin1 N.C. for ML7344xS and ML7344xT
XOUT TCXO *1 SPXO *1	6	Oos Ios I	P or N	- I I	26MHz crystal pin2 (TCXO, SPXO input pin)
NC	7	-	-	-	Non connect pin
RESETN	8	Is	L	I	Hardware reset L: Reset and when in deep sleep mode H: Operation
EXT_CLK	10	IO	P or N	I	Digital Input/Output pin *4 Primary function: external clock (32 kHz) input
GPIO0	16	IO	H or L O_D *2	O/H	Digital Input/Output pin *3 Primary function: Interrupt output
GPIO1	17	IO	H or L O_D *2	O/L	Digital Input/Output pin *3 Primary function: clock output
GPIO2	18	IO	H or L O_D *2	O/L	Digital Input/Output pin *3 Primary function: ANT_SW signal output
GPIO3	19	IO	H or L O_D *2	O/L	Digital Input/Output pin *3 Primary function: TRX_SW signal output

*1 Pin name will differ from the product as follows

Pin No.	ML7344xC	ML7344xS	ML7344xT
5	XIN	N.C.	N.C.
6	XOUT	SPXO	TCXO

*2 O_D means the open drain output.
*3 Usage of GPIOs, please refer [GPIO0_CTRL] register (Bank 0 0x4E) to [GPIO3_CTRL] register (Bank 0 0x51).
*4 Usage of EXT_CLK pin, please refer [EXTCLK_CTRL] register (Bank 0 0x52).

●Power Supply

Pin name	Pin No.	Direction	Active Level	Dir/state at reset	Detail function
VDD_REG	1	PWR	-	-	Power supply for regulator input (Input 1.8V to 3.6V)
VDDIO	9	PWR	-	-	Power supply for digital IOs (Input 1.8V to 3.6V)
VDD_PA	22	PWR	-	-	Power supply for PA block (Input level depends on Tx power)
VDD_RF	25	PWR	-	-	Power supply for RF blocks (Connect to REG_OUT pin. 1.5V)
VDD_CP	27	PWR	-	-	Power supply for Charge Pump block (Connect to REG_OUT pin. 1.5V)
VDD_VCO	32	PWR	-	-	Power supply for VCO block (Connect to REG_OUT pin. 1.5V)
GND_VCO	29	GND	-	-	GND for VCO block

●Unused pins

Followings are recommendation for unused pins

Pin Name	Pin No.	Recommendation
N.C.	5	OPEN (For ML7344xS and ML7344xT)
N.C.	7	GND (Design compatible with ML7406) Or OPEN
EXT_CLK	10	GND
A_MON	23	GND
GPIO0	16	OPEN
GPIO1	17	OPEN
GPIO2	18	OPEN
GPIO3	19	OPEN

*1 When in default setting, GPIO1 function becomes clock out. If not using clock output, it is necessary to stop clock out by set 0b000 to bit2-0 (GPIO1_IO_CFG[2:0]) of [GPIO1_CTRL] register (Bank 0 0x4F). Leave outputting the clock may cause the performance down on RX sensitivity.

■ELECTRICAL CHARACTERISTICS

●Absolute Maximum Ratings

Item	Symbol	Condition	Rating	Unit
Power Supply（I/O）(*1)	V_{DDIO}	Ta=-40 to 85℃ GND=0V	-0.3 to +4.6	V
Power Supply（RF）(*2)	V_{DDRF}		-0.3 to +2.0	V
Digital Input Voltage	V_{DIN}		-0.3 to V_{DDIO}+0.3	V
RF Input Voltage	V_{RFIN}		-1.0 to +2.0	V
Analog Input Voltage	V_{AIN}		-0.3 to V_{DDIO}+0.3	V
Analog Input Voltage2 (*3)	V_{AIN2}		-0.3 to V_{DDRF}+0.3	V
TCXO Input Voltage	V_{TCXO}		-0.3 to 1.75	V
Digital Output Voltage	V_{DO}		-0.3 to V_{DDIO}+0.3	V
RF Output Voltage	V_{RFO}		-0.3 to V_{DDRF}+1.9	V
Analog Output Voltage	V_{AO}		-0.3 to V_{DDIO}+0.3	V
Analog Output Voltage2 (*4)	V_{AO2}		-0.3 to V_{DDRF}+0.3	V
Digital Input Current	I_{DI}		-10 to +10	mA
Digital Output Current	I_{DO}		-8 to +8	mA
Power Dissipation	P_d	Ta=+25℃	1.2	W
Storage Temperature	T_{stg}	—	-55 to +150	deg.C

(*1) VDD_IO, VDD_REG, VDD_PA pins
(*2) VDD_RF, VDD_VCO, VDD_CP pins
(*3) XIN pin
(*4) XOUT pin

●Recommended Operating Conditions

Item	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply (I/O)	V_{DDIO}	VDD_IO, VDD_REG pins	1.8	3.3	3.6	V
Power Supply (PA)	V_{DDPA}	VDD_PA pin TX power = 1mW	1.8	3.3	3.6	V
		VDD_PA pin TX power = 10mW	2.1	3.3	3.6	V
		VDD_PA pin TX power = 20mW	2.6	3.3	3.6	V
		VDD_PA pin TX power = 100mW	3.3	-	3.6	V
Ambient Temperature	T_a	—	-40	+25	+85	deg.C
Rising time Digital Input	T_{IR}	Digital input pins (*1)	—	—	20	nsec
Falling time Digital Input	T_{IF}	Digital Input pins (*1)	—	—	20	nsec
Output loads Digital Ouput	C_{DL}	All Digital Output pins	—	—	20	pF
Master clock frequency	F_{MCK1}	(*2)	TBD	26	TBD	MHz
Master clock accuracy	A_{CMC1}	25kHz spacing (*3) ML7344J	-10		+10	ppm
	A_{CMC2}	200kHz spacing (*3) ML7344C	-30		+30	ppm
TCXO Input	V_{TCXO}	DC cut (ML7344xT)	0.8	-	1.5	Vpp
SPI clock frequency	F_{SCLK}	SCLK pin	0.032	2	16	MHz
SPI clock duty ratio	D_{SCLK}	SCLK pin	45	50	55	%
RF channel frequency	F_{RF}	ML7344C ML7344E ML7344J	470 160 315	— — —	510 180 450	MHz

(*1) Those pins with symbol I, Is at pin definition section
(*2) XIN and XOUT pin (ML7344xC), SPXO pin (ML7344xS), TCXO pin (ML7344xT)
(*3) This difinition is the specification of RF communication availability, not the system requirement.
Use the appropriate frequency accuracy under each specificaton requirement as below.

Specification	Required accuracy
RCR STD-30 type III (Japana)	±10 ppm
RCR STD-30 type IV (Japana)	±4 ppm
Wirelss M-bus N mode	TBD
Wireless M-bus F mode	±16 ppm

●Power Consumption

Item	Symbol	Conditions	Min	Typ (*2)	Max	Unit
Power Consumption (*1)	I_{DD_DSLP}	Deep Sleep mode	–	0.1	–	μA
	I_{DD_SLP1}	Sleep mode 1 (*3)	–	0.4	–	μA
	I_{DD_SLP2}	Sleep mode 2 (*3)	–	0.53	–	μA
	I_{DD_SLP3}	Sleep mode 3 (*3)	–	0.7	–	μA
	I_{DD_SLP4}	Sleep mode 4 (*3)	–	2.14	–	μA
	I_{DD_IDLE}	Idle mode	–	1.0	–	mA
	I_{DD_RX}	RF RX mode (*4)	–	6.2	–	mA
	I_{DD_TX1}	RF TX mode (1mW) (*4) For ML7344E/J	–	6.8	–	mA
	I_{DD_TX10}	RF TX mode (10mW) (*4)	–	26.0	–	mA
	I_{DD_TX20}	RF TX mode (20mW) (*4)	–	28.0	–	mA
	I_{DD_TX100}	RF TX mode (100mW) (*5) For ML7344C	–	73.0	–	mA

(*1) Power consumption is sum of current consumption of all power supply pins
(*2) “Typ” value is centre value under condition of VDDIO=3.3V, 25deg.C.
(*3) The definition od each sleep mode is shown in following table.

Mode.	Register	FIFO	RC Osc. (32kHz)	Low clock timer
Sleep mode 1	Not retain	Not retain	OFF	-
Sleep mode 2	Retain	retain	OFF	-
Sleep mode 3	Retain	Retain	Extenal Input	ON
Sleep mode 4	Retain	Retain	ON	ON

(*4) Under consition of data receiving speed at 9.6 kbps and 426 MHz operation.
(*5) Under consition of data receiving speed at 9.6 kbps and 490 MHz operation.

●DC Characteristics

Item	Symbol	Conditions	Min	Typ (*2)	Max	Unit
Voltage Input High	VIH1	Digital input/inout pins	V_{DDIO} x0.75	–	V_{DDIO}	V
	VIH2	XIN pin	1.35	–	1.5	V
Voltage Input Low	VIL1	Digital input/inout pins	0	–	V_{DDIO} x0.18	V
	VIL2	XIN pin	0	–	0.15	V
Threshold Voltage High level	VT+	Digital pins with shmitt trigger gate	–	1.2	V_{DDIO} x0.75	V
Threshold Voltage Low level	VT-	Digital pins with shmitt trigger gate	V_{DDIO} x0.18	0.8	–	V
Input Leakage Current	IIH1	Digital input pins	-1	–	1	µA
	IIH2	XIN pin	-0.3	–	0.3	µA
	IIL1	Digital input pins	-1	–	1	µA
	IIL2	XIN pin	-0.3	–	0.3	µA
Output Leakage Current for 3-state pins	IOZH	Digital inout pins	-1	–	1	µA
	IOZL	Digital inout pins	-1	–	1	µA
Voltage Ouput level H	VOH	IOH=-4mA	V_{DDIO} x0.8	–	V_{DDIO}	V
Voltage Ouput level L	VOL	IOL=4mA	0	–	0.3	V
Regulator output voltage	MAIN_REG	REG_CORE and REG_OUTpin When in mode other than sleep	1.4	1.5	1.6	V
	SUB_REG	REG_CORE pin When in sleep mode	0.95	1.3	1.65	V
Pin Capacitance	CIN	Input pins	–	6	–	pF
	COUT	Output pins	–	9	–	pF
	CRFIO	RF inout pins	–	9	–	pF
	CAI	Analog input pins	–	9	–	pF

●RF Characteristics

Data Rate : 1.2 kbps to 15 kbps
Modulation scheme : 2-GFSK/ 2-FSK
Channel spacing : 25kHz
Definisiton Point : ANT connector of ML7344 RF board.

【RF Frequency】

Item	Condition	Min	Typ	Max	Unit
ML7344C	LNA_P,PA_OUT pins	470	—	510	MHz
ML7344E		160	170	180	MHz
ML7344J		315	426	450	MHz

NOTE: 1) Support 168 MHz to 510 MHz by changing L and C components between IND1 and IND2 pins
2) Integer multiples of the master clock frequency and its around frequency can not be used.
Please refer section of "Programing Channel Frequency "

【TX】

Item	Condition	Min	Typ	Max	Unit
TX Power	100mW(20dBm) mode (ML7344C)	—	20	—	dBm
	20mW(13dBm) mode (common)	—	13	—	dBm
	10mW(10dBm) mode (common)	—	10	—	dBm
	1mW(0dBm) mode (ML7344E/J)	—	0	—	dBm
Frequency Deviation (Fdev) Range		0.025		400	kHz
Occupied bandwidth 9600 bps (PN9), Fdev=3 kHz	Band including 99% power	8.5	TBD	11.8	kHz
Adjacent Channel Power 9600bps (PN9), Fdev=3 kHz	Offset:25 kHz ±8 kHz band	—	—	-40	dBc
Spurious emission level	Offset :200 kHz (ML7344C) +17 dBm output RBW=3 kHZ	—	—	-54	dBm
	ML7344J +10dBm output 9600 bps (PN9). Fdev = 3 kHz Total power from 62.5 kHz to 162.5kHz offset	—	—	-26	dBm
	Harmonics (ML7344J) +10dBm output without LC trap filter 9600 bps (PN9). Fdev = 3 kHz	—	—	-5	dBm

【RX】

Item	Condition	Min	Typ	Max	Unit
Minimum RX sensitivity BER<0.1%	4.8 kbps, Fdev=3kHz	—	-117	—	dBm
	9.6 kbps, Fdev=3kHz	—	-115	—	dBm
Maximum input level		0	—	—	dBm
Adjacent channel rejection	±25 kHz	—	30	—	dB
Alternate channel rejection	±50 kHz	—	36	—	dB
Blocking (426MHz operation)	1 MHz offset	—	TBD	—	dB
	10 MHz offset	—	TBD	—	dB
Image response (426 MHz operatin)	After I/Q adjustment	—	30	—	dB
Minimum power detection level		—	-115	—	dBm
Power detection range		—	30	—	dB
Spurious Emission level	Compliant with FCC, ARIB, ETSI standard	—	—	-54	dBm

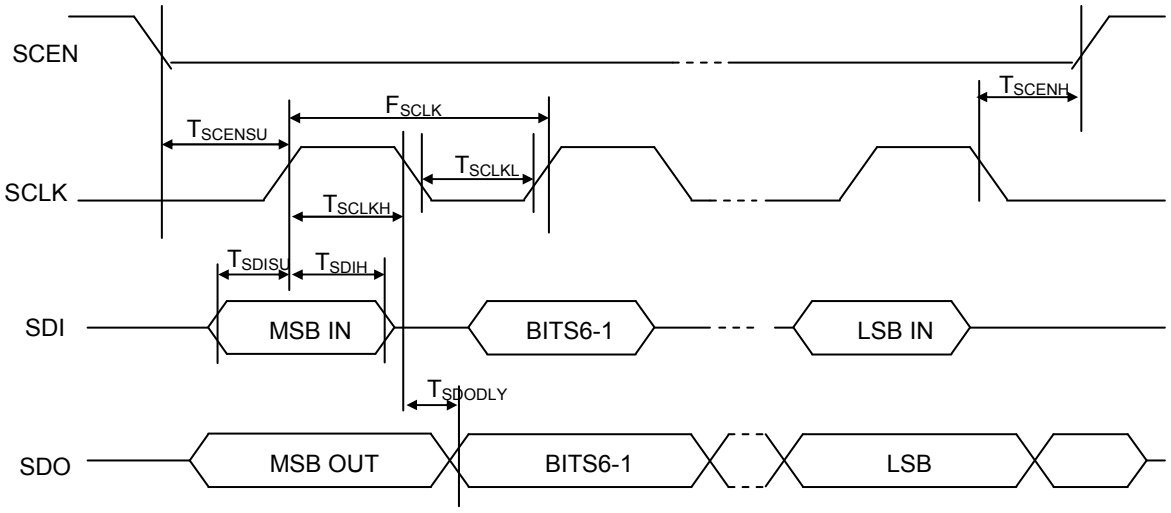
●RC Oscillator Characteritics

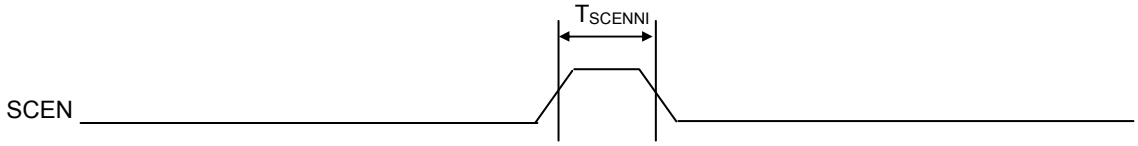
Item	Symbol	Condition	Min	Typ	Max	Unit
Oascillation Frequency	F_{RCOSC}		—	32	—	kHz

●SPI interface

Item	Symbol	Condition	Min	Typ	Max	Unit
SCLK clock frequency	FSCLK	Load capacitance CL=20pF	0.032	2	16	MHz
SCEN input setup time	TSCENSU		30	−	−	nsec
SCEN input hold time	TSCENH		30	−	−	nsec
SCLK high pulse width	TSCLKH		28	−	−	nsec
SCLK low pulse width	TSCLKL		28	−	−	nsec
SDI input setup time	TSDISU		5	−	−	nsec
SDI input hold time	TSDIH		15	−	−	nsec
SCEN negate time	TSCENNI		200	−	−	nsec
SDO output delay	TSDODLY		−	−	22	nsec

NOTE: All timing parameter is defined at voltage level of V_{DDIO} x 20% and V_{DDIO}.



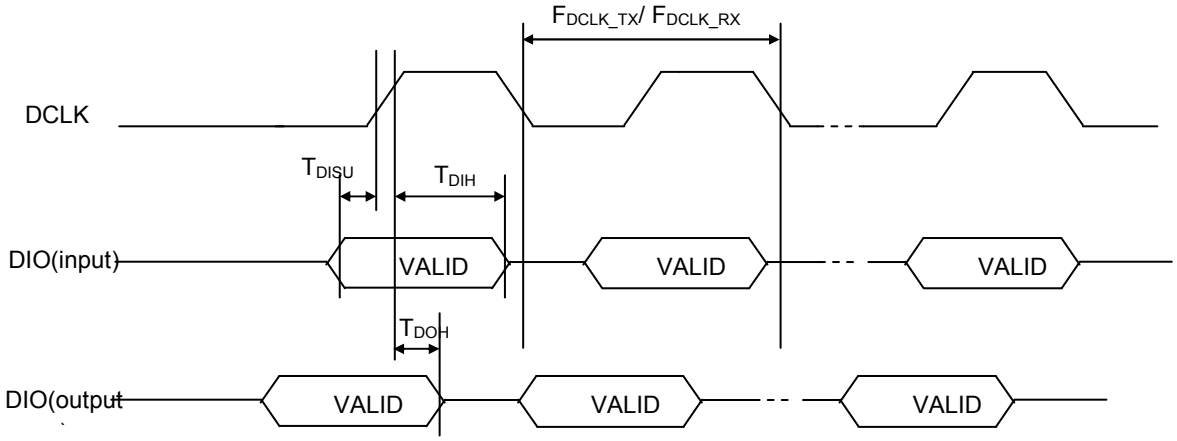


●DIO interface

Item	Symbol	Condition	Min	Typ	Max	Unit
DIO Input setup time	T_{DISU}	Load capacitance CL=20pF	1	—	—	μsec
DIO Input hold time	T_{DIH}		0	—	—	nsec
DIO Output hold time	T_{DOH}		20	—	—	nsec
DCLK clock frequency accuracy in Tx (*1)	F_{DCLK_TX}		(*3)	—	(*3)	kHz
DCLK clock frequency accuracy in Rx (*2)	F_{DCLK_RX}		-30	—	+30	%
DCLK clock output duty ratio (TX)	D_{DCLK_TX}		45	—	55	%
DCLK clock output duty ratio (RX)	D_{DCLK_RX}		30	—	70	%

(*1) DCLK clock frequency in TX mode will be varied depending on the variance of master clock frequency.
(*2) DCLK clock frequency in RX mode will be varied by reproduced clock and its jitter.
(*3) These values are equal to the accuracy of the master clock frequency

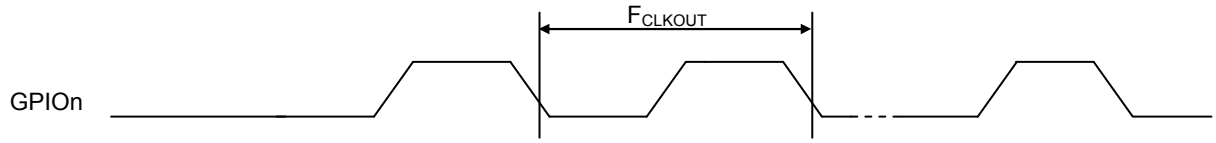
NOTE: All timing parameter is defined at voltage level of V_{DDIO} x 20% and V_{DDIO}.



●Clock output

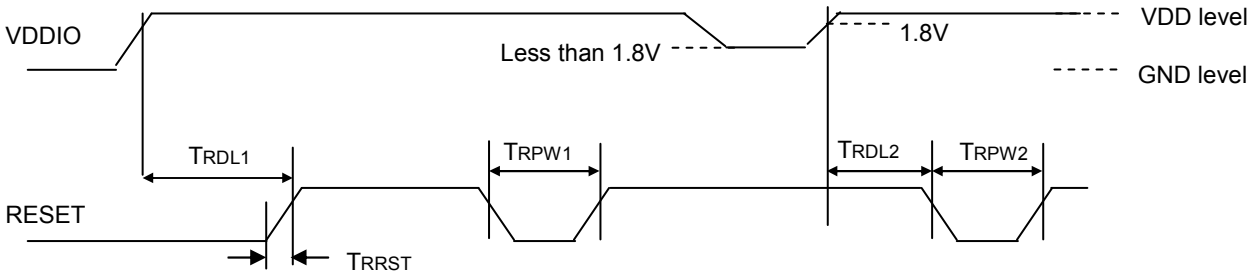
ML7344x has configurable clock output function. It is controlled by [MON_CNTRL] register (Bank 0 0x4D) and [GPIOn_CTRL] registers (n=0 to 3, Bank0 0x4E – 0x51). Default settign is the 3.33MHz clock is output from GPIO1.

Item	Symbol	Condition		Min	Typ	Max	Unit
Clock output frequency	F_{CLKOUT}	Load capacitance CL=20pF		0.0064	3.33	26	MHz
Clock output duty ratio	D_{CLKOUT}		8.66 MHz	33	-	67	%
			Other than 8.66 MJHz	48	50	52	%



●Reset

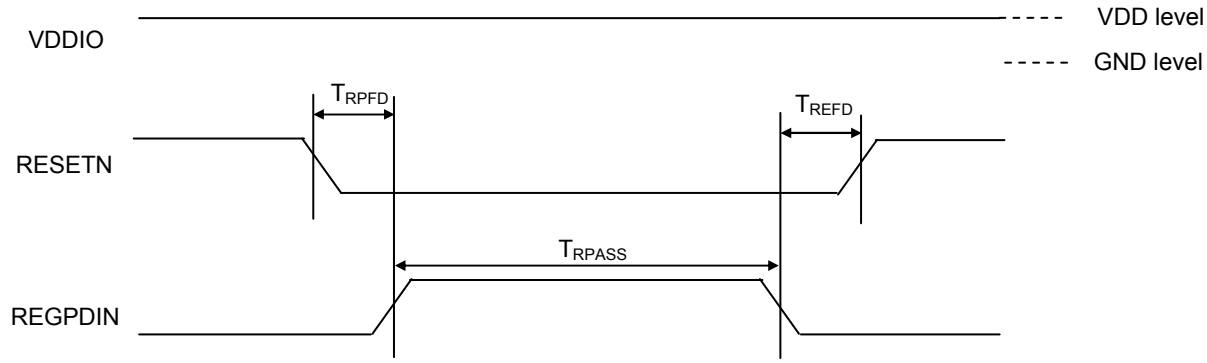
Item	Symbol	Condition	Min	Typ	Max	Unit
RESETN delay time （Power on）	T_{RDL1}	All power supply pins (After power on)	0.5	–	–	msec
RESETN assert time When starting from VDDIO=0V	T_{RPW1}		200	–	–	nsec
RESETN assert time When starting from VDDIO≠0V	T_{RPW2}	VDDIO > 1.8V should be required.	1.5	–	–	msec
RESETN delay time (When ML7344 start up from VDDIO≠0V)	T_{RDL2}	VDDIO > 1.8V	1	–	–	μsec
RESETN rising time	T_{RRST}		–	–	1	msec



Note: When ML7344 start up from VDDIO≠0V, RESETN pulse should be asserted after VDDIO becomes over 1.8V.

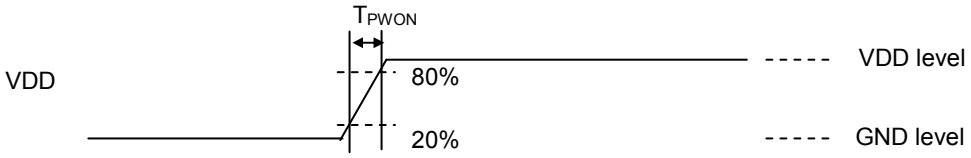
●Deep Sleep Mode

Item	Symbol	Condition	Min	Typ	Max	Unit
REGPDIN assert delay time	T_{RPFD}	VDDIO = "H"	0	–	–	μsec
REGPDIN assert time	T_{RPASS}		1.2	–	–	msec
RESETN release delay time	T_{REFD}		0.5	–	–	msec



●Power on sequence

Item	Symbol	Condition	Min	Typ	Max	Unit
Power on time differences	T_{PWON}	Power on state (All power supply pins)	–	–	5	msec



■REGISTERS

●Register map

It is consist of 3bank, BANK0, BANK1, BANK2 and BANK3. Each BANK has address space of 0x00 to 0x7F, 128 byte in total.

The space shown as gray highlighted part is not implemented in LSI or reserved bits. Reserved bits may be assigned closed function. So write default values to reserved bits, when write a register which contains reserved bits. Regarding reserved register, access is inhibited. BANK2 and BANK3 are closed BANK, then access is limited..

Transision between banks can be controlled by bit 3-0 (BANK[3:0]) of [BANK_SEL] register.

□ : Implemented as functionable register ▒ : Impelemted as reserved bits

BANK0

Address	Symbol (# test register)	Bit								Description
		7	6	5	4	3	2	1	0	
0x00	BANK_SEL									Register access destination (BANK) select
0x01	RST_SET	▒	▒			▒	▒			Software reset control
0x02	CLK_SET1		▒	▒						Clock configuration 1
0x03	CLK_SET2						▒	▒		Clock configuration 2
0x04	PKT_CTRL1						▒			Packet configuration 1
0x05	PKT_CTRL2	▒								Packet configuration 2
0x06	DRATE_SET									Specified DATA setting
0x07	DATA_SET1									Data configuration 1
0x08	DATA_SET2	▒	▒	▒						Data configuration 2
0x09	CH_SET									Enable TX/RX channel number setting
0x0A	RF_STATUS_CTRL	▒	▒							RF auto status transition control
0x0B	RF_STATUS									RF status setting
0x0C	DIO_SET					▒		▒		DIO mode configuration
0x0D	INT_SOURCE_GRP1									Interrupt status for INT07 to INT00
0x0E	INT_SOURCE_GRP2									Interrupt status for INT15 to INT8
0x0F	INT_SOURCE_GRP3									Interrupt status for INT23 to INT16
0x10	INT_EN_GRP1									Interrupt mask for INT07 to INT00
0x11	INT_EN_GRP2									Interrupt mask for INT15 to INT08
0x12	INT_EN_GRP3									Interrupt mask for INT23 to INT16
0x13	CRC_ERR_H	▒	▒	▒	▒	▒	▒	▒		17th CRC error notification for wireless M-bus paket
0x14	CRC_ERR_M									9th to 15th CRC error notification for wireless M-bus packet
0x15	CRC_ERR_L									1st to 8th CRC error notification for wireles M-bus packet
0x16	STATE_CLR		▒	▒		▒	▒			State clear control
0x17	TXFIFO_THRH		▒							Set threshold level for TX_FIFO full interruption
0x18	TXFIFO_THRL		▒							Set threshold level for TX_FIFO empty interruption and transmission threshold level for FAST_TX mode
0x19	RXFIFO_THRH		▒							Set threshold level for RX_FIFO full interruption
0x1A	RXFIFO_THRL		▒							Set threshold level for RX_FIFO empty interruption
0x1B	C_CHECK_CTRL			▒						Detection contol for the control field (C-field) in wireless M-bus Packet
0x1C	M_CHECK_CTRL	▒	▒	▒	▒					Detection control for the manufucture ID field (M-filed) in wireless M-bus packet
0x1D	A_CHECK_CTRL	▒	▒							Detection controk for the address field (A-Field) in wireless M-bus packet
0x1E	C_FIELD_CODE1									Set the pattern cofe #1 of the C-field in wireless M-bu packet.
0x1F	C_FIELD_CODE2									Set the pattern code #2 of the C-field in wireless M-bu packet.

BANK0 (continued)

Address	Symbol (# test register)	Bit								Description
		7	6	5	4	3	2	1	0	
0x20	C_FIELD_CODE3									Set the pattern code #3 of the C-field in wireless M-bu packet.
0x21	C_FIELD_CODE4									Set the pattern code #4 of the C-field in wireless M-bu packet.
0x22	C_FIELD_CODE5									Set the pattern code #5 of the C-field in wireless M-bu packet.
0x23	M_FIELD_CODE1									Set the 1st byte for pattern code #1 of the M-field in wireless M-bu packet.
0x24	M_FIELD_CODE2									Set the 1st byte for pattern code #2 of the M-field in wireless M-bu packet.
0x25	M_FIELD_CODE3									Set the 2nd byte for pattern code #1 of the M-field in wireless M-bu packet.
0x26	M_FIELD_CODE4									Set the 2nd byte for pattern code #2 of the M-field in wireless M-bu packet.
0x27	A_FIELD_CODE1									Set the 1st byte of the A-field in wireless M-bu packet.
0x28	A_FIELD_CODE2									Set the 2nd byte of the A-field in wireless M-bu packet.
0x29	A_FIELD_CODE3									Set the 3rd byte of the A-field in wireless M-bu packet.
0x2A	A_FIELD_CODE4									Set the 4th byte of the A-field in wireless M-bu packet.
0x2B	A_FIELD_CODE5									Set the 5th byte of the A-field in wireless M-bu packet.
0x2C	A_FIELD_CODE6									Set the 6th byte of the A-field in wireless M-bu packet.
0x2D	SLEEP/WU_SET									Control sleep and wake-up operation
0x2E	WUT_CLK_SET									Clock setting for wake-up timer
0x2F	WUT_INTERVAL_H									Set wake-up timer (upper byte)
0x30	WUT_INTERVAL_L									Set wake-up timer (lower byte)
0x31	WU_DURATION									Set wake-up duration
0x32	GT_SET									Set general purpose timer configuration
0x33	GT_CLK_SET									Set input clock for general purpose timers
0x34	GT1_TIMER									Set over-flow value to the general purpose timer #1
0x35	GT2_TIMER									Set over-flow value to the general purpose timer #2
0x36	CCA_IGNORE_LVL									Set ED threshold level to eclude CCA judgement
0x37	CCA_LVL									Set ED threshold level for CCA operation
0x38	CCA_ABORT									Set a time parameter to terminate CCA operation
0x39	CCA_CTRL									Control CCA operation and reporting CCA result
0x3A	ED_RSLT									Reporting ED level
0x3B	IDLE_WAIT_H									Set idle detection timer in CCA operation (upper bits)
0x3C	IDLE_WAIT_L									Set idle detection timer in CCA operation (lower bits)
0x3D	CCA_PROG_H									Report elapsed time as Idle during CCA operation (upper bits)
0x3E	CCA_PROG_L									Report elapsed time as Idle during CCA operation (lower bits)
0x3F,40	Reserved									Reserved
0x41	ED_CTRL									Control ED level detectection
0x42	TXPR_LEN_H									TX preamble length (upper byte)
0x43	TXPR_LEN_L									TX preamble length (lower byte)
0x44	POSTAMBLE_SET									Set postamble configuration
0x45	SYNC_CONDITION1									Set parameters for synchronization 1
0x46	SYNC_CONDITION2									Set parameters for synchronization 2
0x47	SYNC_CONDITION3									Set parameters for synchronization 3
0x48-4C	Reserved									Reserved
0x4D	MON_CTRL									Minotor function control
0x4E	GPIO0_CTRL									Set GPIO0 pin(pin #16) configuration
0x4F	GPIO1_CTRL									Set GPIO1 pin (pin #17) configuration

BANK0 (continued)

Address	Symbol (# test register)	Bit								Description
		7	6	5	4	3	2	1	0	
0x50	GPIO2_CTRL									Set GPIO2 pin (pin #18) configuration
0x51	GPIO3_CTRL									Set GPIO3 pin (pin #19) configuration
0x52	EXTCLK_CTRL									Set EXT_CLK pin (pin #10) configuration
0x53	SPI/EX_PA_CTRL									Set SDO pin (pin #12) and SDI pin (pin #15) configuration. External PA control setting
0x54	IF_FREQ_H									Set intermediate frequency (IF) (upper byte)
0x55	IF_FREQ_L									Set intermediate frequency (IF) (lower byte)
0x56-5D	Reserved									Reserved
0x5E	IFFADJ_H									Adjust DC offset for demdulator (upper 2 bits)
0x5F	IFFADJ_L									Adjust DC offset for demdulator (lower 8 bits)
0x60-61	Reserved									Reserved
0x62	OSC_ADJ1									Adjust load capacitance in oscillation circuit
0x63	OSC_ADJ2									Adjust load capacitance in oscillation circuit with fine step.
0x64	OSC_ADJ3									Adjust bias in oscillation circuit
0x65	OSC_ADJ4									Adjust bias in oscillation circuit when in fast start-up mode
0x66	RSSI_ADJ									Adjast RSSI value
0x67	PA_MODE									PA mode setting
0x68	PA_REG_FINE_ADJ									Adjast voltage regulator output for PA with fine step
0x69	PA_ADJ									Adjast PA gain
0x6A	PA_OVR_DET									Control over load detection of PA
0x6B	PA_OVR_TH_SEL									PA over load threshold level configuration
0x6C-6D	Reserved									Reserved
0x6E	VCO_CAL									Report current VCO calibration value
0x6F	VCO_CAL_START									VCO calibraltion control
0x70	CLK_CAL_SET									External clock calibraltion control
0x71	CLK_CAL_TIME									Set external clock caribration time
0x72	CLK_CAL_H									Report clock calibration result (upper byte)
0x73	CLK_CAL_L									Report clock calibration result (lower byte)
0x74	ADC_PA_DET									Report current PA oputput level
0x75	SLEEP_INT_CLR									All interruption status clear when in sleep mode
0x76	RF_TEST_MODE									RF tramsmission test pattern configuration
0x77	STM_STATE									Report current statius of internal state machine
0x78	FIFO_SET									Select FIFO to read
0x79	RX_FIFO_LAST									Report remaining size (bytes) of RX_FIFO
0x7A	TX_PKT_LEN_H									Set Tx packet length (upper byte)
0x7B	TX_PKT_LEN_L									Set Tx packet length (lower byte)
0x7C	WR_TX_FIFO									Write TX_FIFO data
0x7D	RX_PKT_LEN_H									Report Rx packet length (upper byte)
0x7E	RX_PKT_LEN_L									Report Rx packet length (lower byte)
0x7F	RD_FIFO									Read FIFO data

BANK1

Address	Symbol (# test register)	Bit								Description
		7	6	5	4	3	2	1	0	
0x00	BANK_SEL									Register access destination (BANK) select
0x01	CLK_OUT									Frequency setting of output clock from GPIOn
0x02	TX_RATE_H									Optional Tx data rate setting (upper 4 bits)
0x03	TX_RATE_L									Optional Tx data rate setting (lower 8 bits)
0x04	RX_RATE1_H									Optional Rx data rate setting, parameter #1 (upper 4 bits)
0x05	RX_RATE1_L									Optional Rx data rate setting, parameter #1 (lower 8 bits)
0x06	RX_RATE2									Optional Rx data rate setting, parametert #2
0x07	Reserved									Reserved
0x08	VCO_CAL									Clock frequency settinf for ADC
0x09,0A	Reserved									Reserved
0x0B	PLL_LOCK_DETECT									Parmater setting for PLL lcok detection
0x0C-0x12	Reserveed									Reserved
0x13	RSSI_MAG_ADJ									RSSI scale factor setting for ED values conversion
0x14	RSSI_VAL									ADC result output of RSSI
0x15	AFC/GC_CTRL									AFC parameter setting and gain control setting
0x16	CRC_POLY3									Polynomial parameter #3 of CRC generator
0x17	CRC_POLY2									Polynomial parameter #2 of CRC generator
0x18	CRC_POLY1									Polynomial parameter #1 of CRC generator
0x19	CRC_POLY0									Polynomial parameter #0 of CRC generator
0x1A	PLL_DIV_SET									Select PLL divider
0x1B	TXFREQ_I									I counter seeting for Tx frequency
0x1C	TXFREQ_FH									Tx frequency parameter (upper 4 bits)
0x1D	TXFREQ_FM									Tx frequency parameter (middle 8 bits)
0x1E	TXFREQ_FL									Tx frequency parameter (lower 8 bits)
0x1F	RXFREQ_I									I counter seeting for Rx frequency
0x20	RXFREQ_FH									Rx frequency parameter (upper 4 bits)
0x21	RXFREQ_FM									Rx frequency parameter (middle 8 bits)
0x22	RXFREQ_FL									Rx frequency parameter (lower 8 bits)
0x23	CH_SPACE_H									Frequency separation parameter (upper byte)
0x24	CH_SPACE_L									Frequency separation parameter (lower byte)
0x25	SYNC_WORD_LEN									Length parameter for sync word
0x26	SYNC_WORD_EN									Enable setting for sync word code
0x27	SYNC_WORD1_SET0									Sync word #1 [31:24] bits
0x28	SYNC_WORD1_SET1									Sync word #1[23:16] bits
0x29	SYNC_WORD1_SET2									Sync word #1 [15:8] bits
0x2A	SYNC_WORD1_SET3									Sync word #1 [7:0] bits
0x2B	SYNC_WORD2_SET0									Sync word #2 [31:24] bits
0x2C	SYNC_WORD2_SET1									Sync word #2[23:16] bits
0x2D	SYNC_WORD2_SET2									Sync word #2 [15:8] bits
0x2E	SYNC_WORD2_SET3									Sync word #2 [7:0] bits
0x2F	FSK_CTRL									Time resolution parameter for FSK modulation

BANK1 (continued)

Address	Symbol (# test register)	Bit								Description
		7	6	5	4	3	2	1	0	
0x30	GFSK_DEV_H									Frequency deviation parameter for GFSK modulation (upper 6 bits)
0x31	GFSK_DEV_L									Frequency deviation parameter for GFSK modulation (lower 8 bits)
0x32	FSK_DEV0_H/GFIL0									1st set of frequency deviation for FSK modulation (upper 6bit) / Gaussian filter parameter #0
0x33	FSK_DEV0_L/GFIL1									1st set of frequency deviation for FSK modulation (lower 8bit) / Gaussian filter parameter #1
0x34	FSK_DEV1_H/GFIL2									2nd set of frequency deviation for FSK modulation (upper 6bit) / Gaussian filter parameter #2
0x35	FSK_DEV1_L/GFIL3									2nd set of frequency deviation for FSK modulation (lower 8bit) / Gaussian filter parameter #3
0x36	FSK_DEV2_H/GFIL4									3rd set of frequency deviation for FSK modulation (upper 6bit) / Gaussian filter parameter #4
0x37	FSK_DEV2_L/GFIL5									3rd set of frequency deviation for FSK modulation (lower 8bit) / Gaussian filter parameter #5
0x38	FSK_DEV3_H/GFIL6									4th set of frequency deviation for FSK modulation (upper 6bit) / Gaussian filter parameter #4
0x39	FSK_DEV3_L									4th set of frequency deviation for FSK modulation (lower 8bit)
0x3A	FSK_DEV4_H									5th set of frequency deviation for FSK modulation (upper 6bit)
0x3B	FSK_DEV4_L									5th set of frequency deviation for FSK modulation (lower 8bit)
0x3C	FSK_TIM_ADJ4									Timing parmeter for 4th frequency deviation of FSK modulation
0x3D	FSK_TIM_ADJ3									Timing parameter for 3rd frequency deviation of FSK modulation
0x3E	FSK_TIM_ADJ2									Timing parmeter for 2nd frequency deviation of FSK modulation
0x3F	FSK_TIM_ADJ1									Timing parameter for 1st frequency deviation of FSK modulation
0x40	FSK_TIM_ADJ0									Timing parameter for unmodulated carrier wave of FSK modulation
0x41-4C	Reserved									Reserved
0x4D	VCO_CAL_MIN_I									I counter seeting for VCO minimum operating
0x4E	VCO_CAL_MIN_FH									VCO minimum operating requency parameter (upper 4 bits)
0x4F	VCO_CAL_MIN_FM									VCO minimum operating frequency parameter (middle 8 bits)

BANK1 (continued)

Address	Symbol (# test register)	Bit								Description
		7	6	5	4	3	2	1	0	
0x50	VCO_CAL_MIN_FL									VCO minimum operating frequency parameter (lower 8 bits)
0x51	VCO_CAL_MAX_N									Set VCO maximum operating frequency
0x52	TXVCAL_MIN									Report calibration result or set calibration value of VCO minimum frequency in transmission mode
0x53	TXVCAL_MAX									Report calibration result or set calibration value of VCO maximum frequency in transmission mode
0x54	RXVCAL_MIN									Report calibration result or set calibration value of VCO minimum frequency in receiving mode
0x55	RXVCAL_MAX									Report calibration result or set calibration value of VCO maximum frequency in receiving mode
0x56	DEMOD_SET0									Demodulator setting #0
0x57	DEMOD_SET1									Demodulator setting #1
0x58	DEMOD_SET2									Demodulator setting #2
0x59	DEMOD_SET3									Demodulator setting #3
0x5A	DEMOD_SET4									Demodulator setting #4
0x5B	DEMOD_SET5									Demodulator setting #5
0x5C	DEMOD_SET6									Demodulator setting #6
0x5D	DEMOD_SET7									Demodulator setting #7
0x5E	DEMOD_SET8									Demodulator setting #8
0x5F	DEMOD_SET9									Demodulator setting #9
0x60	DEMOD_SET10									Demodulator setting #10
0x61	DEMOD_SET11									Demodulator setting #11
0x62	ADDR_CHK_CTR_H									Report number of receving packets with address miss-match (upper 3bits)
0x63	ADDR_CHK_CTR_L									Report number of receving packets with address miss-match (lower 8bits)
0x64	WHT_INIT_H									Set initial pattern of data-whitening (ipper 1 bit)
0x65	WHT_INIT_L									Set initial pattern of data-whitening (lower 8 bists)
0x66	WHT_CFG									Select data-whitening polynomial
0x67-7E	Reserved									Reserved
0x7F	ID_CODE									ID code

■Function description

T.B.D

■Flow Charts

T.B.D

■Timing Chart

T.B.D

■Package diagram

T.B.D

■REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL7344C/E/J-01	Oct. 11, 2012	–	–	Preliminary release

NOTES

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