Single-chip built-in FET type Switching Regulator Series

High-Accuracy Frequency Flexible Step-down Switching Regulator

BD9006F/HFP, BD9007F/HFP

●Overview

The high-accuracy frequency flexible step-down switching regulator is a switching regulator with built-in POWER MOS FET, which withstands high pressure. The operational frequency is freely configurable with external resistance. It features a wide input voltage range (7V~35V) and a high frequency accuracy of ±5% (BD9006F/HFP, f=200~500kHz), Furthermore, an external synchronization input pin enables synchronous operation with external clock.

●Features

1) Minimal external components
2) Wide input voltage range: 7V～35V
3) Frequency voltage accuracy: ±5%(BD9006F/HFP, f=200～500kHz)
   ±20%(BD9007F/HFP)
4) Built-in P-ch POWER MOS FET
5) Output voltage setting enabled with external resistor: 0.8V～VIN
6) Reference voltage accuracy: 0.8V±2%
7) Wide operating temperature range: -40℃～+105℃
8) Low dropout: 100% ON duty cycle
9) Standby mode supply current: 0μA (Typ.)
10) Oscillation frequency variable with external resistor: 50～500kHz
11) External synchronization enabled
12) Soft start function: soft start time fixed to 5ms (Typ.)
13) Built-in overcurrent protection circuit
14) Built-in thermal shutdown protection circuit
15) High-power HRP7 package mounted (BD9006HFP,BD9007HFP)
    Compact SOP8 package mounted (BD9006F,BD9007F)

●Applications

All fields of industrial equipment, such as Flat TV, printer, DVD, car audio, car navigation, and communication such as ETC, AV, and OA.

●Product lineup

Item	BD9006F/HFP	BD9007F/HFP
Output Current	2A	2A
Input Range	7V～35V	7V～35V
Oscillation Frequency Range	50～500kHz	50～500kHz
Oscillation Frequency Accuracy	±5%	±20%
External Synchronous Function	Provided	Provided
Standby Function	Provided	Provided
Operating Temperature	-40℃～+105℃	-40℃～+105℃
Package	SOP8/HRP7	SOP8/HRP7

●Absolute Maximum Ratings (Ta=25°C)

Parameter		Symbol	Limits	Unit
Power Supply Voltage		V_{IN}	36	V
Output Switch Pin Voltage		V_{SW}	V_{IN}	V
Output Switch Current		I_{SW}	2 ＊1	A
EN/SYNC Pin Voltage		$V_{EN/SYNC}$	V_{IN}	V
RT, FB, INV Pin Voltage		V_{RT},V_{FB},V_{INV}	7	
Power Dissipation	HRP7	Pd	5.5 ＊2	W
	SOP8		0.69 ＊3	W
Operating Temperature Range		Topr	-40～+105	℃
Storage Temperature Range		Tstg	-55～+150	℃
Maximum Junction Temperature		Tjmax	150	℃

＊1 Should not exceed Pd-value.
＊2 Reduce by 44mW/℃ over 25℃,when mounted on 2-layerPCB of 70×70×1.6mm^3
(PCB incorporates thermal via. Copper foil area on the reverse side of PCB: 10.5×10.5mm^2
Copper foil area on the reverse side of PCB: 70×70mm^2
＊3 Reduce by 5.52mW/℃ over 25℃,when mounted on 2-layer PCB of 70×70×1.6mm^3

●Recommended Operating Range

Parameter	BD9006F/HFP	BD9007F/HFP	Unit
Operating Power Supply Voltage	7～35	7～35	V
Output Switch Current	～2	～2	A
Output Voltage (min pulse width)	250	250	ns
Oscillation Frequency	50～500	50～500	kHz
Oscillation Frequency set Resistance	27～360	27～360	kΩ

●Possible Operating Range

Parameter	BD9006F/HFP	BD9007F/HFP	Unit
Operating Power Supply Voltage	5～35	5～35	V

●Electrical Characteristics

◎BD9006F/HFP (Unless otherwise specified, Ta=25℃, V_{IN}=13.2V, $V_{EN/SYNC}$=5V)

Parameter	Symbol	Spec Values			Unit	Conditions
		Min.	Typ.	Max.		
Standby Circuit Current	I_{STB}	-	0	10	μA	$V_{EN/SYNC}$=0V
Circuit Current	I_Q	-	4	6.5	mA	I_O=0A,RT=51kΩ,V_{INV}=0.7V
【SW Block】						
POWER MOS FET ON Resistance	R_{ON}	-	0.3	0.6	Ω	I_{SW}=50mA
Operating Output Current Of Overcurrent Protection	I_{OLIMIT}	2	4	-	A	
Output Leak Current	I_{OLEAK}	-	0	30	μA	V_{IN}=35V, $V_{EN/SYNC}$=0V
【Error Amp Block】						
Reference Voltage 1	V_{REF1}	0.784	0.800	0.816	V	V_{FB}=V_{INV}
Reference Voltage 2	V_{REF2}	0.780	0.800	0.820	V	V_{IN}=10～16V,V_{FB}=V_{INV}
Reference Voltage Input Regulation	ΔVREF	-	0.5	-	%	
Input Bias Current	IB	-1	-	-	μA	V_{INV}=0.6V
Maximum FB Voltage	V_{FBH}	2.2	2.4	-	V	V_{INV}=0V
Minimum FB Voltage	V_{FBL}	-	0.5	0.6	V	V_{INV}=2V
FB Sink Current	I_{FBSINK}	-0.47	-1.16	-2.45	mA	V_{FB}=1V,V_{INV}=1V
FB Source Current	$I_{FBSOURCE}$	1	5	15	mA	V_{FB}=1V,V_{INV}=0.6V
Soft Start Time	T_{SS}	3	5	9	mS	Ta=-40～105℃
【Oscillator Block】						
Oscillation Frequency	F_{OSC}	285	300	315	kHz	R_T=51kΩ
Frequency Input Regulation	ΔFOSC	-	0.5	-	%	V_{IN}=10～16V
【Enable/Sync Input Block】						
Output ON Voltage	V_{ENON}	2.6	-	-	V	$V_{EN/SYNC}$ Sweep Up, Ta=-40～105℃
Output OFF Voltage	V_{ENOFF}	-	-	0.8	V	$V_{EN/SYNC}$ Sweep Down, Ta=-40～105℃
Sink Current	$I_{EN/SYNC}$	-	35	90	μA	
External Sync Frequency	F_{SYNC}	495	500	505	kHz	RT=51kΩ, EN/SYNC=500kHz,Duty 50%

＊Not designed to be radiation resistant.

◎BD9007F/HFP (Unless otherwise specified, Ta=25℃, V_{IN}=13.2V, $V_{EN/SYNC}$=5V)

Parameter	Symbol	Spec Values			Unit	Conditions
		Min.	Typ.	Max.		
Standby Circuit Current	I_{STB}	-	0	10	μA	$V_{EN/SYNC}$=0V
Circuit Current	I_Q	-	4	6.5	mA	I_O=0A,RT=51kΩ,V_{INV}=0.7V
【SW Block】						
POWER MOS FET ON Resistance	R_{ON}	-	0.3	0.6	Ω	I_{SW}=50mA
Operating Output Current Of Overcurrent Protection	I_{OLIMIT}	2	4	-	A	
Output Leak Current	I_{OLEAK}	-	0	30	μA	V_{IN}=35V, $V_{EN/SYNC}$=0V
【Error Amp Block】						
Reference Voltage 1	V_{REF1}	0.784	0.800	0.816	V	V_{FB}=V_{INV}
Reference Voltage 2	V_{REF2}	0.780	0.800	0.820	V	V_{IN}=10～16V,V_{FB}=V_{INV}
Reference Voltage Input Regulation	ΔVREF	-	0.5	-	%	
Input Bias Current	IB	-1	-	-	μA	V_{INV}=0.6V
Maximum FB Voltage	V_{FBH}	2.2	2.4	-	V	V_{INV}=0V
Minimum FB Voltage	V_{FBL}	-	0.5	0.6	V	V_{INV}=2V
FB Sink Current	I_{FBSINK}	-0.47	-1.16	-2.45	mA	V_{FB}=1V,V_{INV}=1V
FB Source Current	$I_{FBSOURCE}$	1	5	15	mA	V_{FB}=1V,V_{INV}=0.6V
Soft Start Time	T_{SS}	3	5	9	mS	Ta=-40～105℃
【Oscillator Block】						
Oscillation Frequency	F_{OSC}	240	300	360	kHz	R_T=51kΩ
Frequency Input Regulation	ΔFOSC	-	0.5	-	%	V_{IN}=10～16V
【Enable/Sync Input Block】						
Output ON Voltage	V_{ENON}	2.6	-	-	V	$V_{EN/SYNC}$ Sweep Up, Ta=-40～105℃
Output OFF Voltage	V_{ENOFF}	-	-	0.8	V	$V_{EN/SYNC}$ Sweep Down, Ta=-40～105℃
Sink Current	$I_{EN/SYNC}$	-	35	90	μA	
External Sync Frequency	F_{SYNC}	495	500	505	kHz	RT=51kΩ, EN/SYNC=500kHz,Duty 50%

＊Not designed to be radiation resistant.

●Reference Data

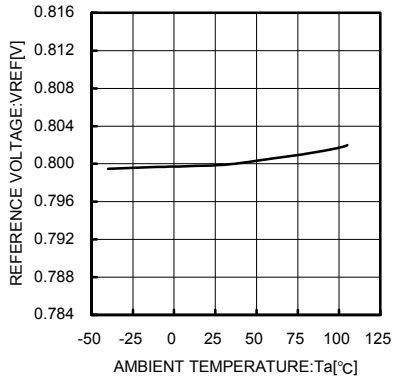


Fig.1 Output reference voltage vs. Ambient temperature (All series)

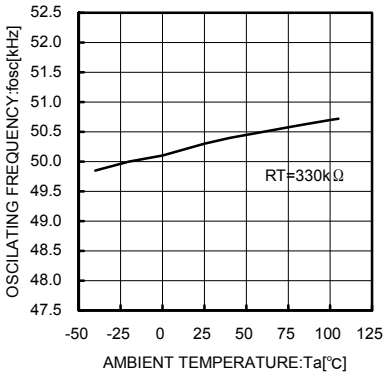


Fig.2 Frequency vs. Ambient temperature (All series)

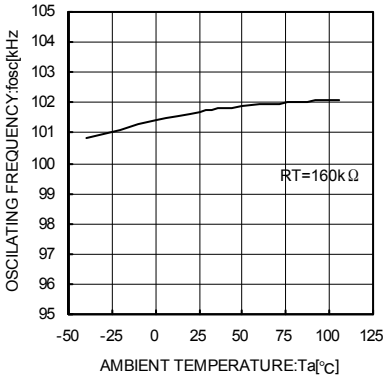


Fig.3 Frequency vs. Ambient temperature (All series)

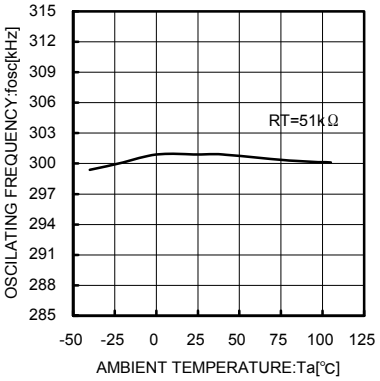


Fig.4 Frequency vs. Ambient temperature (All series)

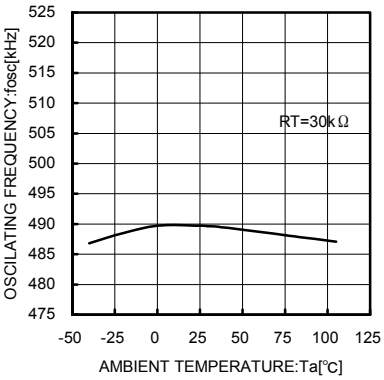


Fig.5 Frequency vs. Ambient temperature (All series)

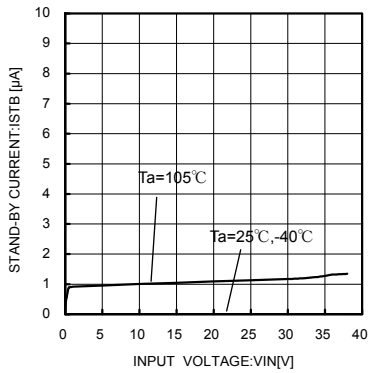


Fig.6 Standby Current (All series)

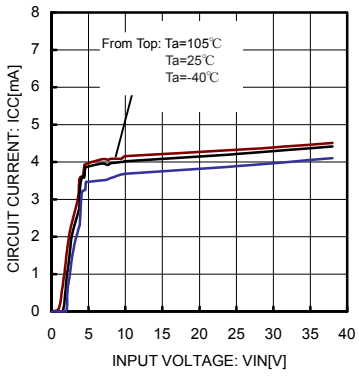


Fig.7 Circuit Current (All series)

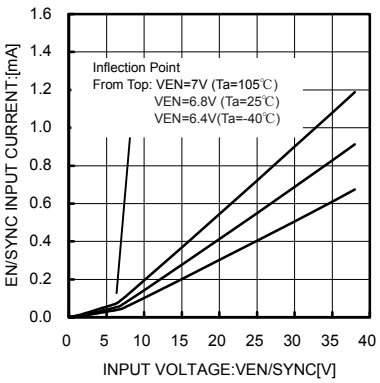


Fig.8 EN/SYNC Input Current (All series)

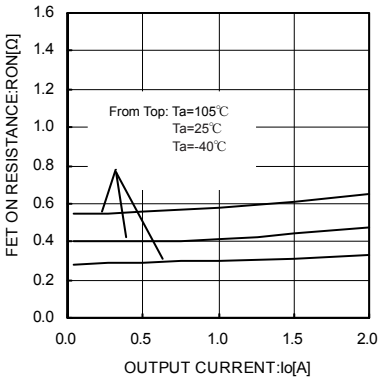


Fig.9 ON Resistance VIN=7V (All series)

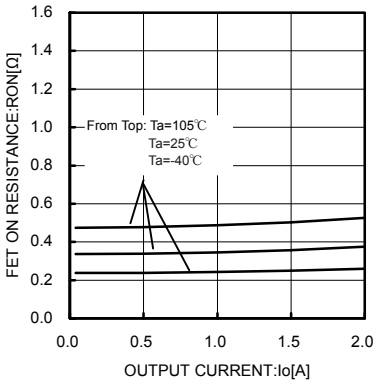


Fig.10 ON Resistance VIN=13.2V (All series)

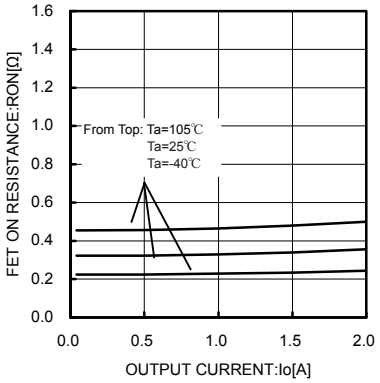


Fig.11 ON Resistance VIN=35V (All series)

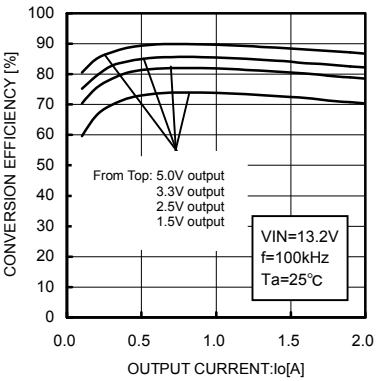


Fig.12 Efficiency f=100kHz (All series)

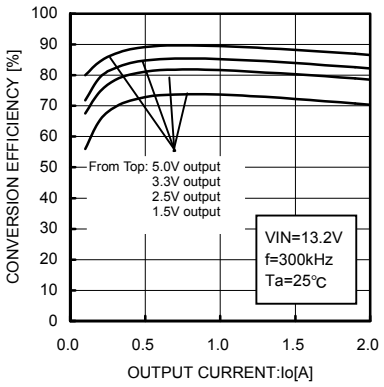


Fig.13 Efficiency f=300kHz (All series)

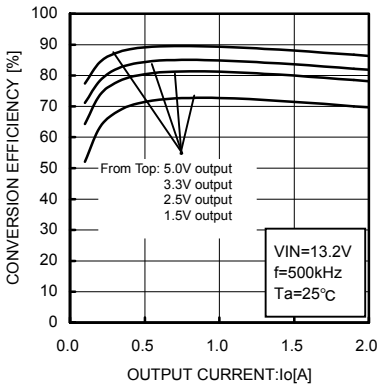


Fig.14 Efficiency f=500kHz (All series)

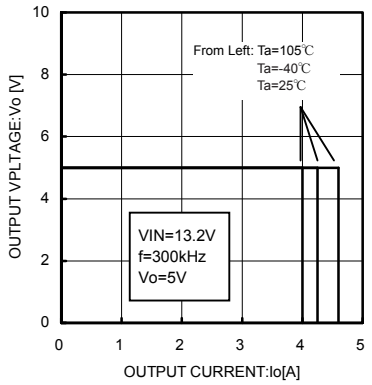


Fig.15 Over-current Protection Operation Current (All series)

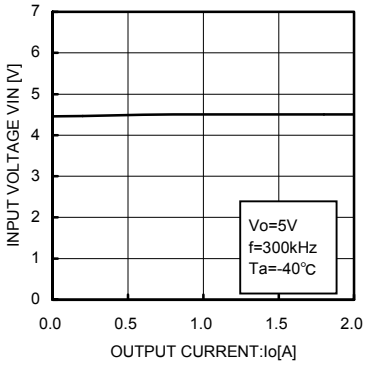


Fig.16 The lowest voltage of possible operation (All series)

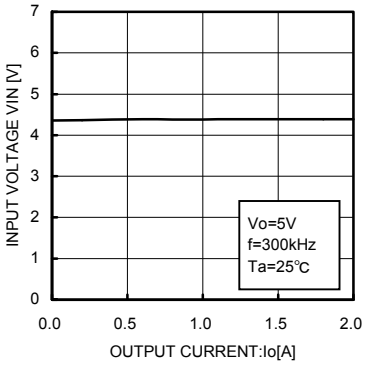


Fig.17 The lowest voltage of possible operation (All series)

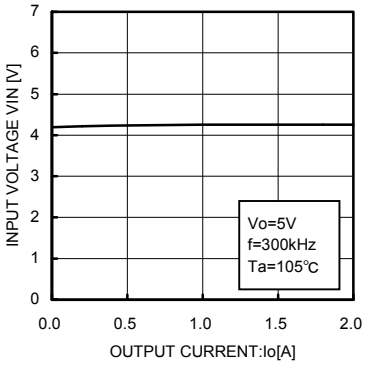


Fig.18 The lowest voltage of possible operation (All series)

●Block Diagrams / Application circuit / PIN assignment

(BD9006F/BD9007F)

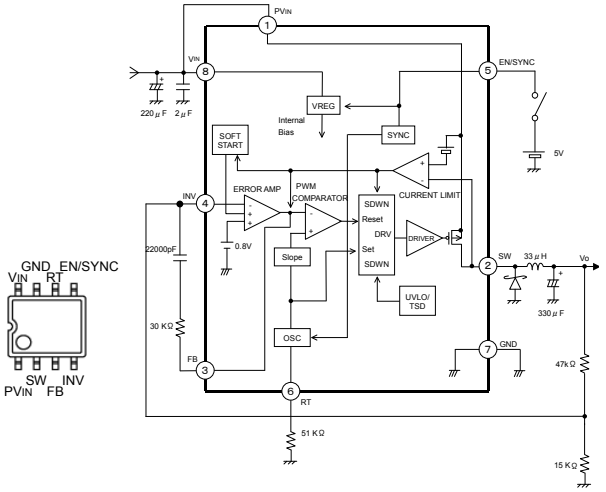


Fig.19

(BD9006HFP/BD9007HFP)

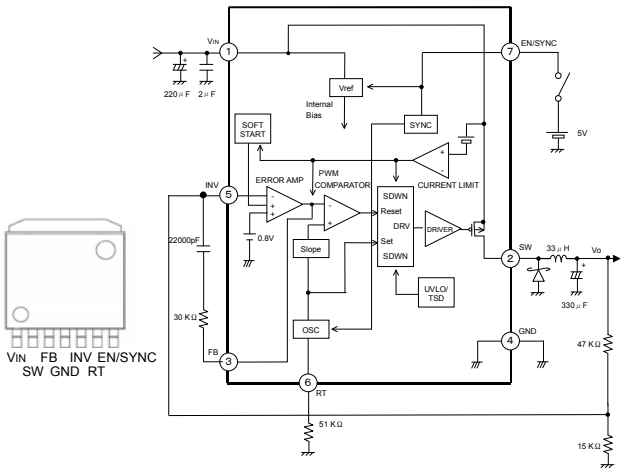


Fig.20

No.	Pin name	Function
1	PVIN	Power system power supply input
2	SW	Output
3	FB	Error Amp output
4	INV	Output voltage feedback
5	EN/SYNC	Enable/Synchronizing pulse input
6	RT	Frequency setting resistor connection
7	GND	Ground
8	VIN	Power supply input

No.	Pin name	Function
1	VIN	Power supply input
2	SW	Output
3	FB	Error Amp output
4	GND	Ground
5	INV	Output voltage feedback
6	RT	Frequency setting resistor connection
7	EN/SYNC	Enable/Synchronizing pulse input
FIN	-	Ground

∗VIN and PVIN must be shorted before use

●Description of operations

・ERROR AMP

The ERROR AMP block is an error amplifier used to input the reference voltage (0.8V Typ.) and the INV pin voltage. The output FB pin controls the switching duty and output voltage Vo. These INV and FB pins are externally mounted to facilitate phase compensation. Inserting a capacitor and resistor between these pins enables adjustment of phase margin. (Refer to recommended examples on pages 11~13.)

・SOFT START

The SOFT START block provides a function to prevent the overshoot of the output voltage Vo through gradually increasing the normal rotation input of the error amplifier when power supply turns ON to gradually increase the switching Duty. The soft start time is set to 5msec (Typ.).

・SYNC

By making the “EN/SYNC” terminal less than 0.8V, the circuit can be shut down.

Furthermore, by applying pulse with higher frequency than the configured oscillation frequency to the “EN/SYNC” terminal, external sync is possible. (Sync possible with double the configured frequency-configured frequency or 500kHz)

・OSC(Oscillator)

This circuit generates the pulse wave to be input to the slope, and by connecting resistance to “RT”, 50~500kHz oscillating frequency can be configured. (Refer to p.11 Fig.24)

・slope

This block generates saw tooth waves from the clock generated by the OSC. The generated saw tooth waves are sent to PWM COMPARATOR.

・PWM COMPARATOR

The PWM COMPARATOR block is a comparator to make comparison between the FB pin and internal saw tooth wave and output a switching pulse.

The switching pulse duty varies with the FB value. (min Duty width : 250ns.)

・TSD (Thermal Shut Down)

In order to prevent thermal destruction/thermal runaway of the IC, the TSD block will turn OFF the output when the chip temperature reaches approximately 150℃ or more. When the chip temperature falls to a specified level, the output will be reset. However, since the TSD is designed to protect the IC, the chip junction temperature should be provided with the thermal shutdown detection temperature of less than approximately.150℃.

・CURRENT LIMIT

While the output POWER P-ch MOS FET is ON, if the voltage between drain and source (ON resistance×load current) exceeds the reference voltage internally set with the IC, this block will turn OFF the output to latch. The overcurrent protection detection values have been set as shown below:

BD9006F/HFP, BD9007F/HFP ・・・ 4A (Typ.)

Furthermore, since this overcurrent protection is an automatically reset, after the output is turned OFF and latched, the latch will be reset with the RESET signal output by each oscillation frequency.

However, this protection circuit is only effective in preventing destruction from sudden accident. It does not support for the continuous operation of the protection circuit (e.g. if a load, which significantly exceeds the output current capacitance, is normally connected). Furthermore, since the overcurrent protection detection value has negative temperature characteristics, consider thermal design.

●Timing Chart

(All series)

・Basic Operation

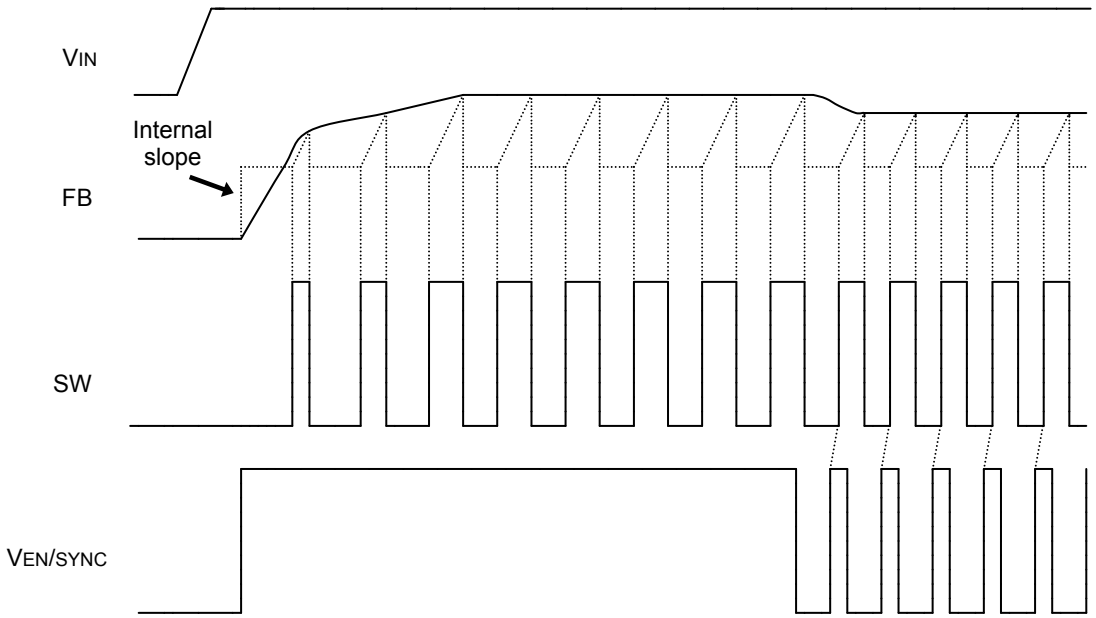


Fig.21

●External synchronizing function

In order to activate the external synchronizing function, connect the frequency setting resistor to the RT pin and then input a synchronizing signal to the EN/SYNC pin. As the synchronizing signal, input a pulse wave higher than a frequency determined with the setting resistor (RT).

However, the external sync frequency should be configured at less than double the configured frequency.

(ex.) When the configured frequency is 100kHz, the external sync frequency should be less than 200kHz.

Furthermore, the pulse wave's LOW voltage should be under 0.8V and the HIGH voltage over 2.6V (when the HIGH voltage is over 6V the EN/SYNC input current increases [see p.4 Fig.8]), the through rate of stand-up (and stand-down) under 20V/μS.

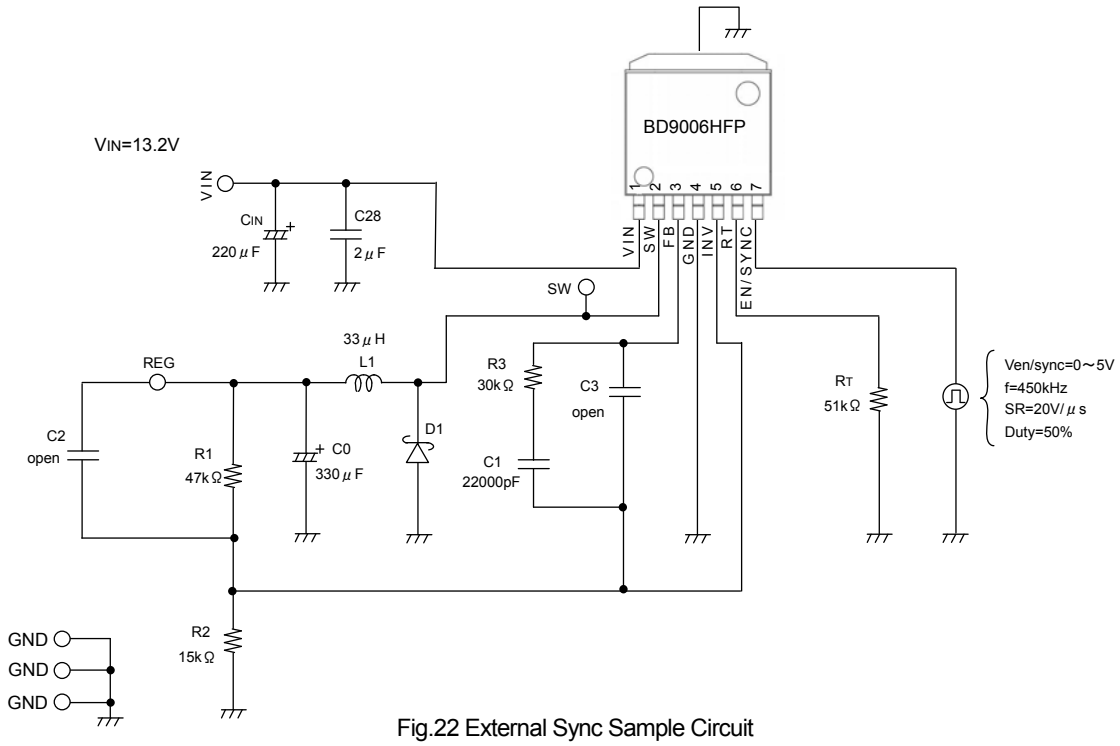


Fig.22 External Sync Sample Circuit
(Vo=3.3V, Io=1A, f=300kHz, EN/SYNC=450kHz)

●Description of external components

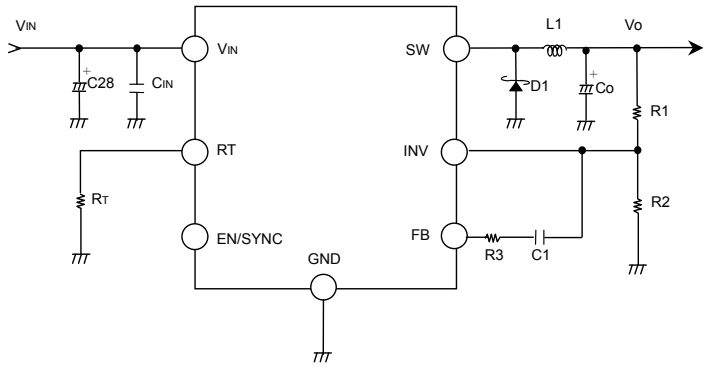


Fig.23

Design Procedure	Sample Calculations
Vo=Output voltage, VIN (Max.)=Maximum input voltage Io (Max.)=Maximum load current, f=Oscillation frequency	When Vo=3.3V, VIN (Typ.)=13.2V Io(Max.)=1A and f=300kHz
1. Setting or output voltage Output voltage can be obtained by the formula shown below: Vo=0.8×(1+R1/R2) Use the formula to select the R1 and R2. Furthermore, set the R2 to 30kΩ or less. Select the current passing through the R1 and R2 to be small enough for the output current.	When VO=3.3V and R2=15kΩ 3.3=0.8×(1+R1/15kΩ) R1=46.875kΩ≒47kΩ R1=47kΩ
2. Selection of coil (L1) The value of the coil can be obtained by the formula shown below: L1=(VIN-Vo)×Vo / (VIN×f×ΔIo) ΔIo: Output ripple current ΔIo should typically be approximately 20 to 30% of Io. If this coil is not set to the optimum value, normal (continuous) Oscillation may not be achieved. Furthermore, set the value of the coil with an adequate margin so that the peak current passing through the coil will not exceed the rated current of the coil.	When VIN=13.2V, Vo=3.3V, Io=1A and f=300kHz, L1=(13.2-3.3)×3.3/{13.2×300k×(1×0.3)} =27.5μH≒33μH L1=33μH
3. Selection of output capacitor (Co) The output capacitor can be determined according to the output ripple voltage ΔVo(p-p) required. Obtain the required ESR value by the formula shown below and then select the capacitance. ΔIL=(VIN-Vo)×Vo/(L×f×VIN) ΔVpp=ΔIL×ESR+(ΔIL×Vo)/(2×Co×f×VIN) Set the rating of the capacitor with an adequate margin to the output voltage. Also, set the maximum allowable ripple current with an adequate margin to ΔIL. Furthermore, the output rise time should be shorter than the soft start time. Select the output capacitor having a value smaller than that obtained by the formula shown below. $C_{MAX} = \frac{3.0m \times (I_{LIMIT} - Io(Max))}{Vo}$ ILIMIT : 2A (BD9006F/HFP, BD9007F/HFP) If this capacitances is not optimum, faulty startup may result. (※3.0m is soft start time(min).)	VIN=13.2V, Vo=3.3V, L=33μH, f=300kHz ΔIL=(13.2-3.3)×3.3/(33×10^{-6}×300×10^{3}×13.2) =0.25 ΔIL=0.25A When ILIMIT: 2A, Io(Max)=1A, Vo=3.3V CMAX =3.0m×(2-1)/3.3 ≒910μ CMAX=910μF

Design Method	Sample Calculations
4. Selection of diode (D1) Set diode rating with an adequate margin to the maximum load current. Also, make setting of the rated inverse voltage with an adequate margin to the maximum input voltage. A diode with a low forward voltage and short reverse recovery time will provide high efficiency.	When V_{IN}(max.)=35V Io=(max.)2A Diode ratings must include: Current over 2A Withstand minimum 35V
5. Selection of input capacitor (C_{IN}, C28) Two capacitors, ceramic capacitor C_{IN} and bypass capacitor C28 should be inserted between the V_{IN} and GND. Be sure to insert a ceramic capacitor of 2 to 10μF for the C_{IN}. The capacitor C28 should have a low ESR and a significantly large ripple current. The ripple current I_{RMS} can be obtained by the following formula: $I_{RMS}=Io\times\sqrt{Vo\times(V_{IN}-Vo)/V_{IN}^2}$ Select capacitors that can accept this ripple current. If the capacitance of C_{IN} and C28 is not optimum, the IC may malfunction.	When V_{IN}=13.2V, Vo=3.3V and Io=1A: $I_{RMS}=1\times\sqrt{3.3\times(13.2-3.3)/(13.2)^2}$ I_{RMS}=0.433A
6. Setting of oscillating frequency Referring Fig.24 on the following page, select R for the oscillating frequency to be used.	When f=300kHz From p.11 Fig.24, a resistance of R_T=51kΩ is selected. R_T=51kΩ
7. Setting of phase compensation (R3 and C1) The phase margin can be set through inserting a capacitor or a capacitor and resistor between the INV pin and the FB pin. Each set value varies with the output coil, capacitance, I/O voltage, and load. Therefore, set the phase compensation to the optimum value according to these conditions. (For details, refer to Application circuit on page.11～) If this setting is not optimum, output oscillation may result.	※Please contact us if there are any questions regarding phase compensation configuration.

※The set values listed above are all reference values. On the actual mounting of the IC, the characteristics may vary with the routing of wirings and the types of parts in use. In the connection, it is recommended to thoroughly verify these values on the actual system prior to use.

●Directions for pattern layout of PCB

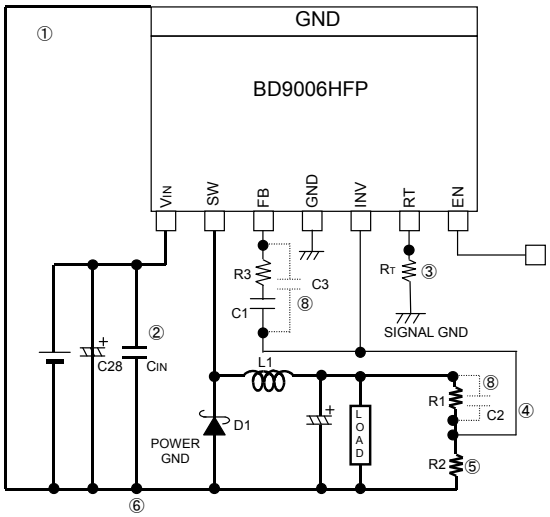


Fig.24

① Arrange the wirings shown by heavy lines as short as possible in a broad pattern.
② Locate the input ceramic capacitor C_{IN} as close to the V_{IN}-GND pin as possible.
③ Locate the R_T as close to the GND pin as possible.
④ Locate the R1 and R2 as close to the INV pin as possible, and provide the shortest wiring from the R1 and R2 to the INV pin.
⑤ Locate the R1 and R2 as far away from the L1 as possible.
⑥ Separate POWER GND (Schottky diode, I/O capacitor's GND) and SIGNAL GND (R_T, GND), so that SW noise doesn't have an effect on SIGNAL GND at all.
⑦ Design the POWER wire line as wide and short as possible.
⑧ Additional pattern for C2 and C3 expand compensation flexibility.

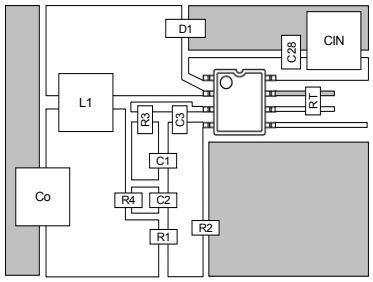


Fig.25 BD9006F Reference Layout Pattern

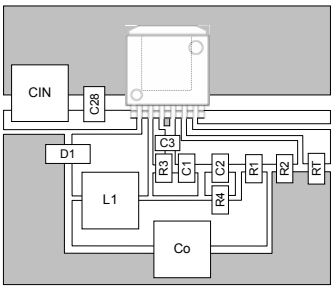


Fig.26 BD9006HFP Reference Layout Pattern

※As shown above ,design the GND pattern as large as possible within inner layer.
※Gray zones indicate GND.

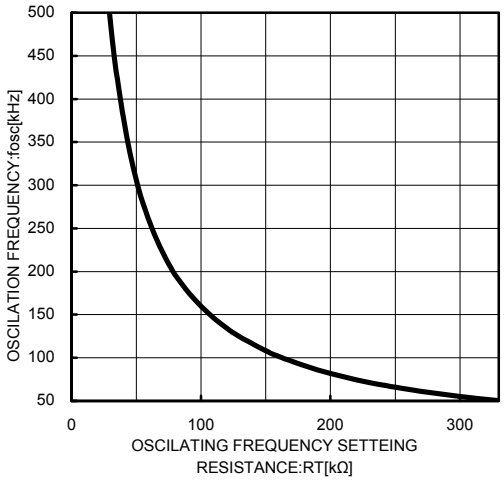


Fig.27 R_T Resistance Values vs. Oscillating Frequency

RT[kΩ]	fosc[kHz]	RT[kΩ]	fosc[kHz]
27	537	100	160
30	489	110	146
33	449	120	134
36	415	130	124
39	386	150	108
43	353	160	102
47	324	180	91
51	300	200	82
56	275	220	75
62	250	240	69
68	229	270	61
75	209	300	55
82	192	330	50
91	174	360	46

※The values in the graph for oscillating frequency are Typical values, and variance of±5% for BD9006F/HFP and ±20% for BD9007F/HFP should be considered.

●Phase Compensation setting procedure

1. Application stability conditions

The following section describes the stability conditions of the negative feedback system.

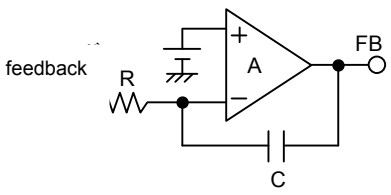
Since the DC/DC converter application is sampled according to the switching frequency, GBW (frequency at 0-dB gain) of the overall system should be set to 1/10 or less of the switching frequency. The following section summarizes the targeted characteristics of this application.

・At a 1 (0-dB) gain, the phase delay is 150˚ or less (i.e. the phase margin is 30˚ or more).
・The GBW for this occasion is 1/10 or less of the switching frequency.

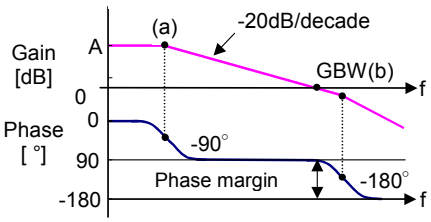
Responsiveness is determined with restrictions on the GBW. To improve responsiveness, higher switching frequency should be provided.

Replace a secondary phase delay (-180˚) with a secondary phase lead by inserting two-phase leads, to ensure the stability through the phase compensation. Furthermore, the GBW (i.e., frequency at 0-dB gain) is determined according to phase compensation capacitance provided for the error amplifier. Consequently, in order to reduce the GBW, increase the capacitance value.

(1) Typical integrator (low pass filter)



(2) Open loop characteristics of integrator



Point (a) $fa=\frac{1}{2\pi RCA}$ [Hz]

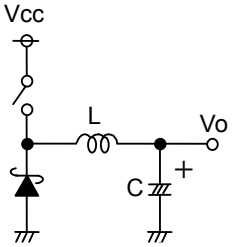
Point (b) $fb=GBW=\frac{1}{2\pi RC}$ [Hz]

s ror amplifier is provided with (1) or (2) phase compensation, the low pass filter is applied. In the case of the DC/DC c lication, the R becomes a parallel resistance of the feedback resistance.

2. For output capacitors having high ESR, such as electrolyte capacitor

For output capacitors that have high ESR (i.e., several Ω), the phase compensation setting procedure becomes comparatively simple. Since the DC/DC converter application has a LC resonant circuit attached to the output, a -180° phase-delay occurs in that area. If ESR component is present, however a +90° phase-lead occurs to shift the phase delay to -90°. Since the phase delay should be set within 150°, it is a very effective method but tends to increase the ripple component of the output voltage.

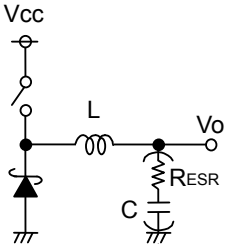
(1) LC resonant circuit



$$fr = \frac{1}{2\pi\sqrt{LC}} \text{ [Hz]}$$

At this resonance point, a-180° phase-delay occurs.

(2) With ESR provided



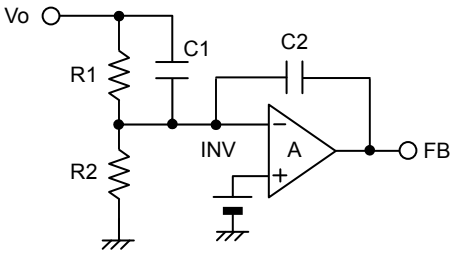
$$fr = \frac{1}{2\pi\sqrt{LC}} \text{ [Hz]: Resonance}$$

$$f_{ESR} = \frac{1}{2\pi R_{ESR}C} \text{ [Hz]: Phase lead}$$

A -90° phase-delay occurs.

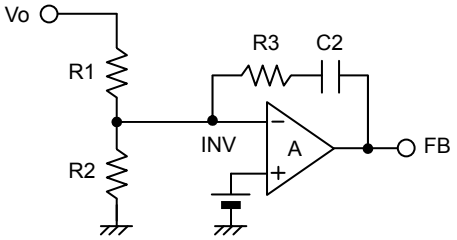
According to changes in phase characteristics, due to the ESR, only one phase lead should be inserted. For this phase lead, select either of the methods shows below:

(3) Insert Feedback Resistance in the C.



$$\text{Phase lead } fz = \frac{1}{2\pi C1R1} \text{ [Hz]}$$

(4) Insert the R3 in integrator.



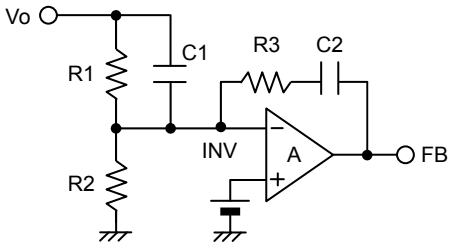
$$\text{Phase lead } fz = \frac{1}{2\pi C2R3} \text{ [Hz]}$$

To cancel the LC resonance, the frequency to insert the phase lead should be set close to the LC resonant frequency.
The setting above have is estimated. Consequently, the setting may be adjusted on the actual system. Furthermore, since these characteristics vary with the layout of PCB loading conditions, precise calculations should be made on the actual system.

3. For output capacitors having low ESR, such as low impedance electrolyte capacitor or OS-CON

In order to use capacitors with low ESR (i.e., several tens of mΩ), two phase-leads should be inserted so that a -180°phase-delay, due to LC resonance, will be compensated. The following section shows a typical phase compensation procedure.

(1) Phase compensation with secondary phase lead



$$\text{Phase lead : } fz1 = \frac{1}{2\pi R1C1} \text{ [Hz]}$$

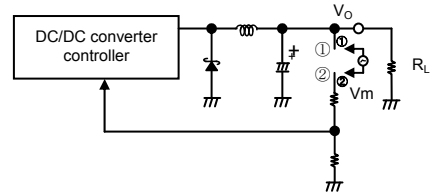
$$\text{Phase lead : } fz2 = \frac{1}{2\pi R3C2} \text{ [Hz]}$$

$$\text{LC resonant frequency : } fr = \frac{1}{2\pi\sqrt{LC}} \text{ [Hz]}$$

To set phase lead frequency, insert both of the phase leads close to the LC resonant frequency. According to empirical rule, setting the phase lead frequency fZ2 with R3 and C2 lower than the LC resonant frequency fr, and the phase lead frequency fZ1 with the R1 and C1 higher than the LC resonant frequency fr, will provide stable application conditions.

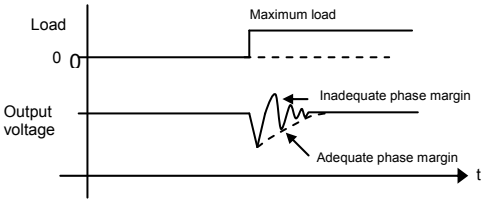
<Reference> Measurement of open loop of the DC/DC converter

To measure the open loop of the DC/DC converter, use the gain phase analyzer or FRA to measure the frequency characteristics.



<Procedure>

1. Check to ensure output causes no oscillation at the maximum load in closed loop.
2. Isolate ① and ② and insert Vm (with amplitude of approximately. 100mVpp).
3. Measure (probe) the oscillation of ① to that of ②.



Furthermore, the phase margin can also be measured with the load responsiveness. Measure variations in the output voltage when instantaneously changing the load from no load to the maximum load. Even though ringing phenomenon is caused, due to low phase margin, no ringing takes place. Phase margin is provided. However, no specific phase margin can be probed.

※Please contact us if you have any questions regarding phase compensation.

●Heat Loss

For thermal design, be sure to operate the IC within the following conditions.
(Since the temperatures described hereunder are all guaranteed temperature, take margin into account.)

1. The ambient temperature Ta is to be 105℃ or less.
2. The chip junction temperature Tj is to be 150℃ or less.

The chip junction temperature Tj can be considered in the following two patterns:

To obtain Tj from the IC surface temperature Tc in actual use state,

$Tj = Tc + \theta j-c \times W$

< Reference value > θj−c : HRP7 7℃/W
SOP8 32.5℃/W

To obtain Tj from the ambient temperature Ta

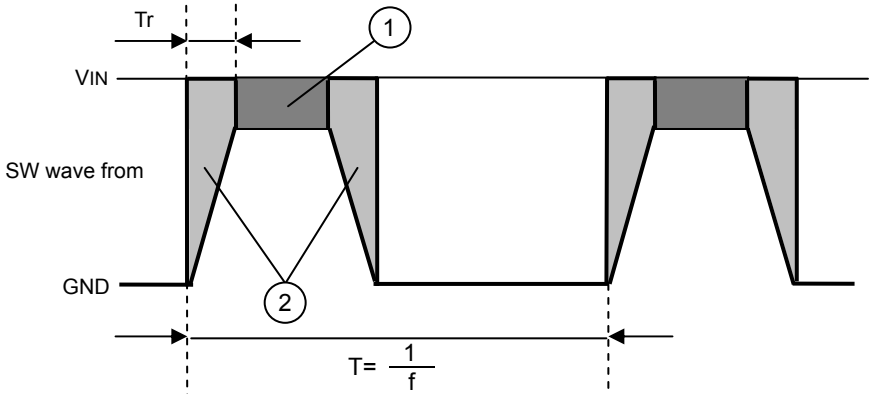
$Tj = Ta + \theta j-a \times W$

< Reference. value > θj−a : HRP7 89.3℃/W Single piece of IC
54.3℃/W 2-layer PCB (Copper foil area on the front side of PCB: 15×15mm^2)
22.7℃/W 2-layer PCB (Copper foil area on the front side of PCB: 70×70mm^2)
PCB size: 70×70×1.6mm^3
(PCB incorporates thermal via.)
Copper foil area on the front side of PCB: 10.5×10.5mm^2
SOP8 222.2℃/W Single piece of IC
181.8℃/W 1-layer PCB
PCB size: 70×70×1.6mm^3

The heat loss W of the IC can be obtained by the formula shown below:

$$W = Ron \times Io^2 \times \frac{Vo}{VIN} + VIN \times Icc + Tr \times VIN \times Io \times f$$

Ron: ON resistance of IC (refer to page.4) Io: Load current
Vo: Output voltage VIN: Input voltage Icc: Circuit current (refer to page.3)
Tr: Switching rise/fall time (approximately 20nsec)
f: Oscillation frequency



① $Ron \times Io^2$

② $2 \times \frac{1}{2} \times Tr \times \frac{1}{T} \times VIN \times Io$

$= Tr \times VIN \times Io \times f$

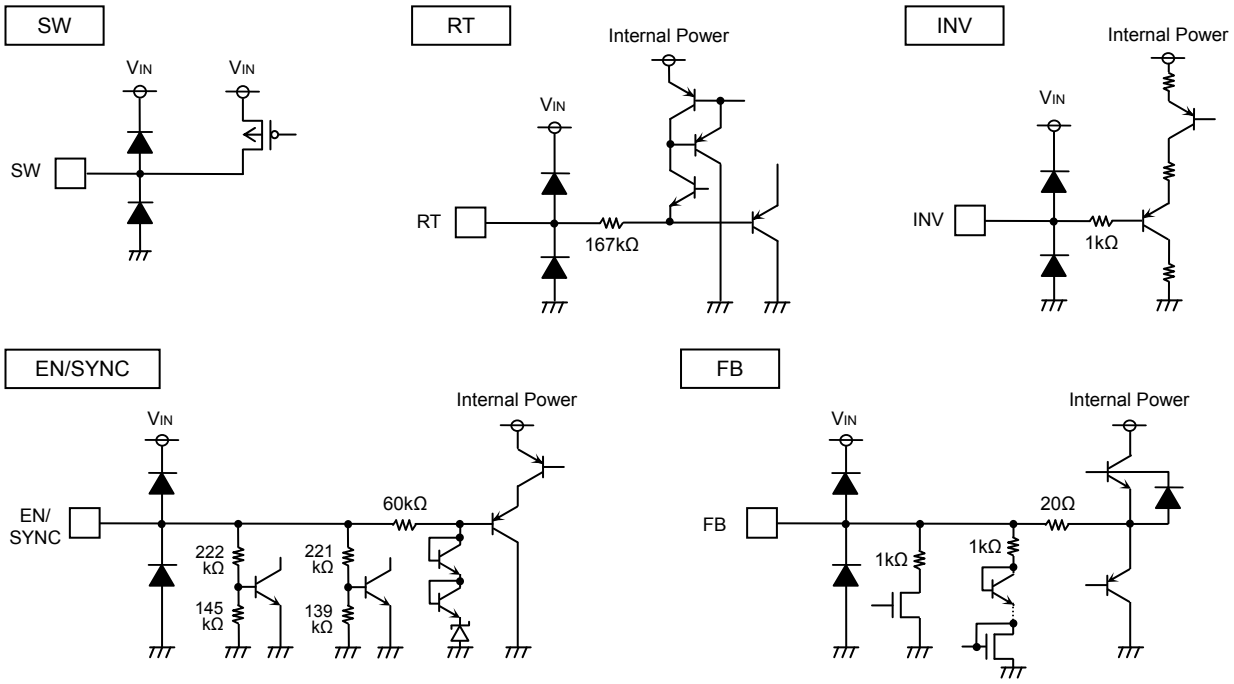


Fig.28 Equivalent circuit

●Cautions on use

1. Absolute maximum ratings

If excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2. GND potential

Ground-GND potential should maintain at the minimum ground voltage level. Furthermore, no terminals should be lower than the GND potential voltage including electric transients.

3. Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4. Inter-pin shorts and mounting errors

When attaching to the set substrate, pay special attention to the direction and proper placement of the IC. If the IC is attached incorrectly, it may be destroyed.

Furthermore, when using the IC with VIN and EN/SYNC terminals shorted, and the 5-pin (SOP8 package) or 7-pin (HRP7 package) EN/SYNC terminal and 6-pin RT terminal are shorted, the IC may also be damaged when VIN>7V.

5. Operation in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6. Inspection with set printed circuit board

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to, or removing it from a jig or fixture, during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting and storing the IC.

7. IC pin input (Fig. 26)

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

・When GND>pin A and GND>pin B, the P-N junction operates as a parasitic diode.

・When pin B >GND>pin A, the P-N junction operates as a parasitic transistor. Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

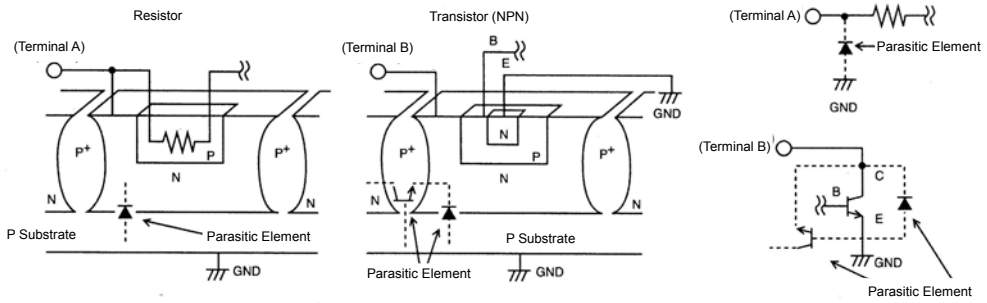


Fig.29 Typical simple construction of monolithic IC

8. GND wiring pattern

It is recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB, so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause on fluctuations in voltages of the small-signal GND. Prevent fluctuations in the GND wiring pattern of external parts.

9. Temperature protection (thermal shut down) circuit

This IC has a built-in temperature protection circuit to prevent the thermal destruction of the IC. As described above, be sure to use this IC within the power dissipation range. Should a condition exceeding the power dissipation range continue, the chip temperature Tj will rise to activate the temperature protection circuit, thus turning OFF the output power element. Then, when the tip temperature Tj falls, the circuit will be automatically reset. Furthermore, if the temperature protection circuit is activated under the condition exceeding the absolute maximum ratings, do not attempt to use the temperature protection circuit for set design.

10. On the application shown below, if there is a mode in which V_{IN} and each pin potential are inverted, for example, if the V_{IN} is short-circuited to the Ground with external diode charged, internal circuits may be damaged. To avoid damage, it is recommended to insert a backflow prevention diode in the series with V_{IN} or a bypass diode between each pin and V_{IN}.

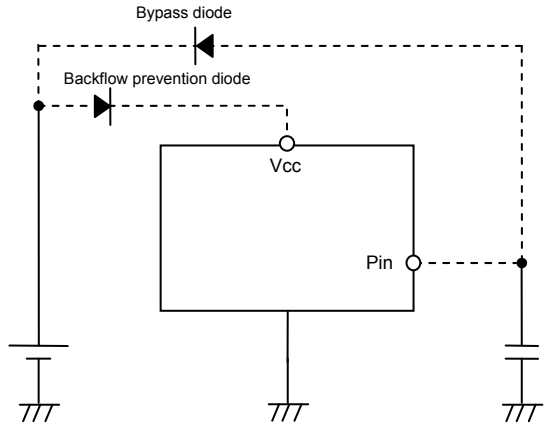
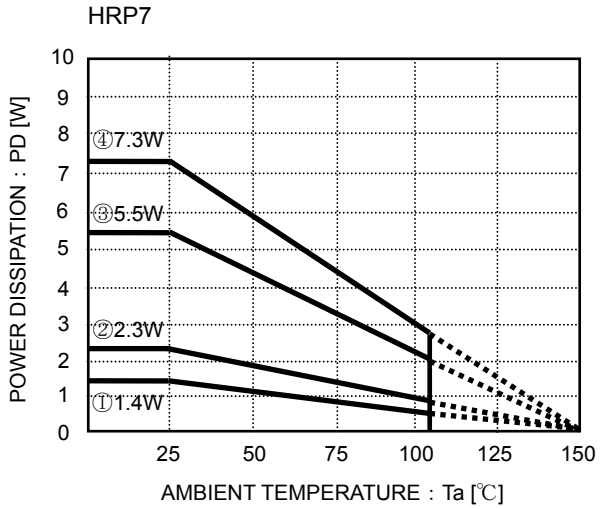


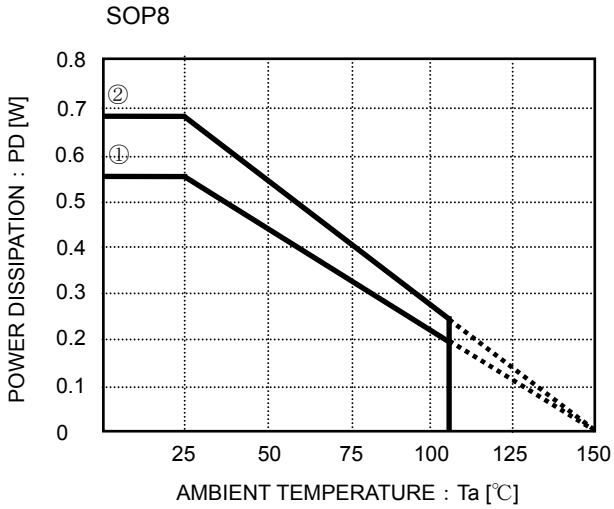
Fig.30

●Thermal reduction characteristics



① Single piece of IC
PCB Size: 70×70×1.6mm^3 (PCB incorporates thermal via)
Copper foil area on the front side of PCB: 10.5×10.5mm^2
② 2-layer PCB (Copper foil area on the reverse side of PCB: 15×15mm^2)
③ 2-layer PCB (Copper foil area on the reverse side of PCB: 70×70mm^2)
④ 4-layer PCB (Copper foil area on the reverse side of PCB: 70×70mm^2)

Fig.31



① Single piece of IC
② When mounted on ROHM standard PCB
(Glass epoxy PCB of 70mm×70mm×1.6mm)

Fig.32

●Ordering Name Selection

B	D	9	0	0	6	H	F	P	-	T	R

Rohm Model Name

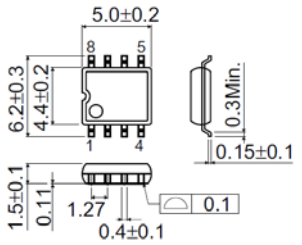
Item Number
9006=36V/2A
9007=36V/2A

Package Type
F=SOP8
HFP=HRP7

Taping Style Name
E2=Reel type embossed taping (SOP8)
TR=Reel type embossed taping (HRP7)

SOP8

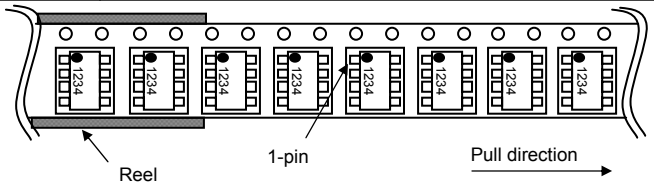
<External View>



(Unit:mm)

<Packaging Specifications>

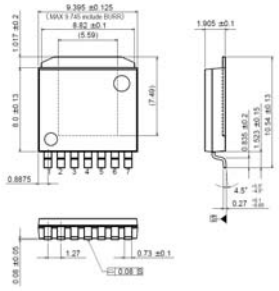
Package Presentation	Embossed taping
Pc per Pkg	2500pcs
Packing	E2 (Direction of 1-pin of product when reel in left hand and right hand pulling tape.)



※Orders must be made in pairs of reels.

HRP7

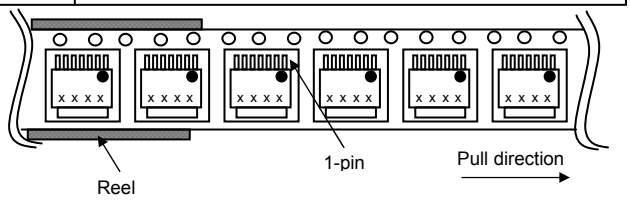
<External View>



(Unit:mm)

<Packaging Specifications>

Package Presentation	Embossed taping
Pc per pkg	2000pcs
Packing	TR (Direction of 1-pin of product when reel in left hand and right hand pulling tape.)



※Orders must be made in pairs of reels.

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