PC8265A
PowerPC based Communications Processor
PowerQUICC II

Datasheet

Features

- PC603e® Microprocessor (Embedded PowerPC Core) at 133 - 300 MHz
  - 280 MIPS at 200 MHz (Dhrystone 2.1)
  - 520 MIPS at 300 MHz (Dhrystone 2.1)
  - High-performance, Superscalar Microprocessor
  - Disable CPU Mode
  - Improved Low-power Core
  - 16-Kbyte Data and 16-Kbyte Instruction Cache, Four-way Set Associative
  - Memory Management Unit (MMU)
  - Floating Point Unit (FPU)
  - Common On-chip Processor (COP)
- Two Bus Architectures: One 64-bit PowerPC and One 32-bit PCI or Local Bus
- System Integration Unit (SIU)
  - Memory Controller, Including Two Dedicated SDRAM Machines
  - PCI up to 66 MHz
  - Hardware Bus Monitor and Software Watchdog Timer
  - IEEE® 1149.1 JTAG Test Access Port
- High-performance Communications Processor Module (CPM)
  - CPM Frequency Up to 200 MHz
  - PowerPC and CPM May Run at Different Frequencies
  - Parallel I/O Registers
  - On-board 32 KBytes of Dual-port RAM
  - Two Multi-channel Controllers (MCCs) Each Supporting 128 Full-duplex, 64-Kbps, HDLC Lines
  - Virtual DMA Functionality
  - 3 FCCs Supporting:
    - Up to 155 Mbps ATM SAR, Maximum of Two (AAL0, AAL1, AAL2, AAL5)
    - 10/100 Mbps Ethernet, Up to Three (IEEE 802.3X with Flow Control)
    - 45 Mbps HDLC/Transparent (Up to Three)
- Two UTOPIA Level-2 Master/Slave Ports, Both with Multi-PHY Support. One Can Support 8/16 bit Data
- Three MII Interfaces
- Eight TDM Interfaces (T1/E1), Two TDM Ports Can Be Glueless to T3/E3
- Power Consumption: 2.5W at 300 MHz

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1. Description

The PC8265A PowerQUICC II™ is a versatile communications processor that integrates on one chip, a high-performance PowerPC (PC603e) RISC microprocessor, a highly flexible system integration unit, and many communications peripheral controllers that can be used in a variety of applications, particularly in communications and networking systems.

The core is an embedded variant of the PC603e microprocessor, specifically referred to later in this document as the EC603e, with 16 Kbytes of instruction cache and 16 Kbytes of data cache and floating-point unit (FPU). The system interface unit (SIU) consists of a flexible memory controller that interfaces to almost any user-defined memory system, a 60x-to-PCI bus bridge and many other peripherals, making this device a complete system on a chip.

The communications processor module (CPM) includes all the peripherals found in the PC860, with the addition of three high-performance communication channels that support new emerging protocols (for example, 155-Mbps ATM and Fast Ethernet).

Equipped with dedicated hardware, the PC8265A can handle up to 256 full-duplex, time-division, multiplexed logical channels.

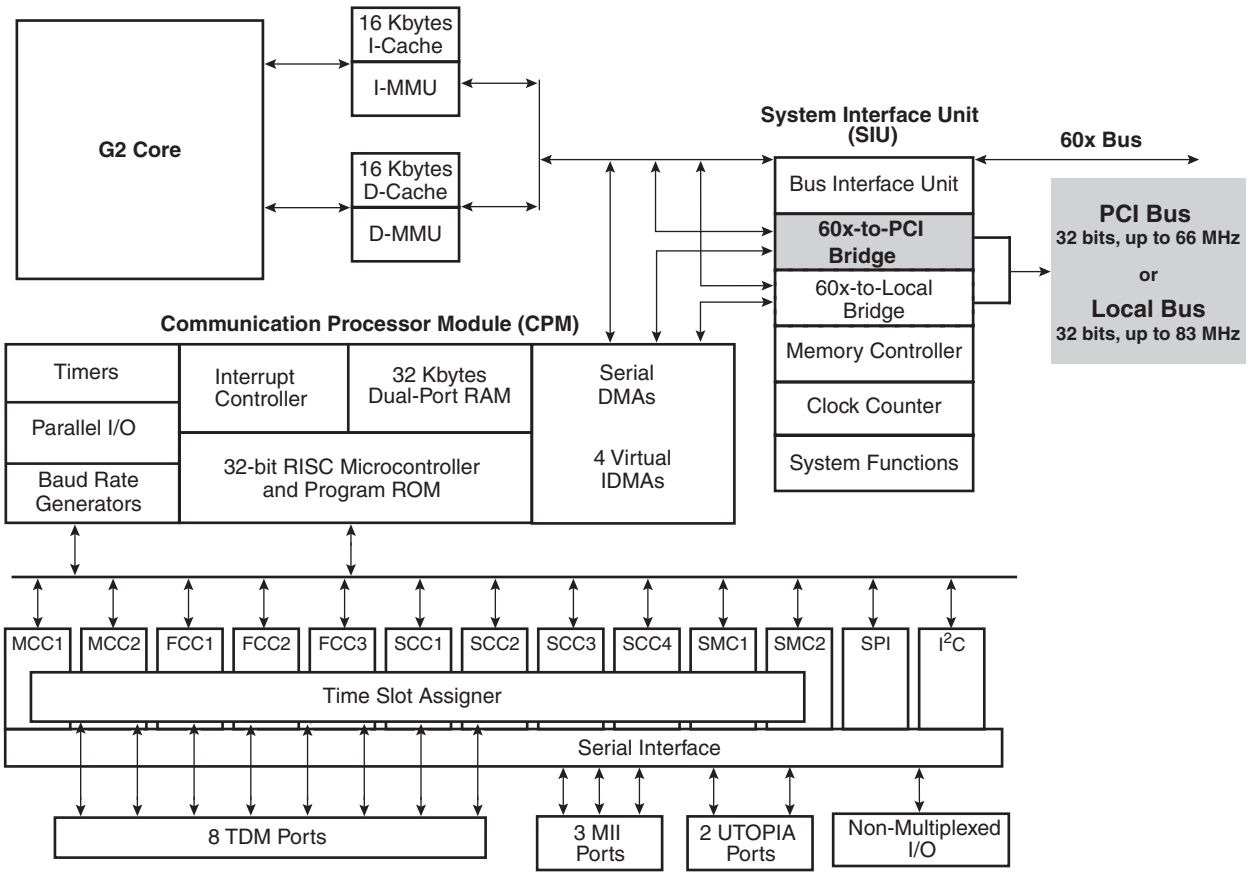
1.1 Screening Quality Packaging

This product is manufactured in full compliance with:

- Upscreening based upon e2v standards
- Military temperature range (T_{amb} = -55°C, T_J = +125°C)
- 480-ball Tape Ball Grid Array package (TBGA 37.5 × 37.5 mm)

2. PC8265A Architecture General Overview

Figure 2-1. Block Diagram



3. Features Overview

The major features of the PC8265A family are as follows:

- Dual-issue integer core

  A core version of the EC603e microprocessor

  System core microprocessor supporting frequencies of 150 – 300 MHz

  Separate 16-Kbyte data and instruction caches:

  – Four-way set associative
  – Physically addressed
  – LRU replacement algorithm

  PowerPC architecture-compliant memory management unit (MMU)

  Common on-chip processor (COP) test interface

  High-performance (6.6 - 7.65 SPEC95 benchmark at 300 MHz; 1.68 MIPs/MHz without inlining and 1.90 Dhrystones MIPS/MHz with inlining)

  Supports bus snooping for data cache coherency

Floating-point unit (FPU)

- Separate power supply for internal logic and for I/O
- Separate PLLs for G2 core and for the CPM

  G2 core and CPM can run at different frequencies for power/performance optimization

  Internal core/bus clock multiplier that provides 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios

  Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
- 64-bit data and 32-bit address 60x bus

  Bus supports multiple master designs

  Supports single- and four-beat burst transfers

  64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller

  Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus

  Single-master bus, supports external slaves

  Eight-beat burst transfers

  32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge

  Programmable host bridge and agent

  32-bit data bus, 66 MHz, 3.3V

  Synchronous and asynchronous 60x and PCI clock modes

  All internal address space available to external PCI host

  DMA for memory block transfers

  PCI-to-60x address remapping
- System interface unit (SIU)

  Clock synthesizer

  Reset controller

  Real-time clock (RTC) register

  Periodic interrupt timer

  Hardware bus monitor and software watchdog timer

  IEEE 1149.1 JTAG test access port
- Twelve-bank memory controller

  Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals

  Byte write enables and selectable parity generation

  32-bit address decoder with programmable bank size

Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine

Byte selects of 64 bus width (60x) and byte selects for 32 bus width (local)

Dedicated interface logic for SDRAM

- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)

Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support of communications protocols

Interfaces to G2 core through an on-chip 32-Kbyte dual-port RAM and DMA controller

Serial DMA channels for receive and transmit on all serial channels

Parallel I/O registers with open-drain and interrupt capability

Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers

Three fast communications controllers supporting the following protocols:

– 10/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through a media independent interface (MII)
– ATM – Full-duplex SAR protocols at 155 Mbps, through UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 16 K external connections
– Transparent
– HDLC – Up to T3 rates (clear channel)

Two multichannel controllers (MCCs)

– Each MCC handles 128 serial, full-duplex, 64-Kbps data channels. Each MCC can be split into four subgroups of 32 channels each
– Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC

Four serial communications controllers (SCCs) identical to those on the PC860, supporting the digital portions of the following protocols:

– Ethernet/IEEE 802.3 CDMA/CS
– HDLC/SDLC and HDLC bus
– Universal asynchronous receiver transmitter (UART)
– Synchronous UART
– Binary synchronous (BISYNC) communications
– Transparent

Two serial management controllers (SMCs), identical to those of the PC860

– Provides management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
– Transparent
– UART (low-speed operation)

One serial peripheral interface identical to the PC860 SPI

One inter-integrated circuit (I2C) controller (identical to the PC860 I2 C controller)

  - Microwire compatible
  - Multiple-master, single-master, and slave modes

  Up to eight TDM interfaces

  - Supports two groups of four TDM channels for a total of eight TDMs
  - 2,048 bytes of SI RAM
  - Bit or byte resolution
  - Independent transmit and receive routing, frame synchronization
  - Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale™ interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces

  Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels

  Four independent 16-bit timers that can be interconnected as two 32-bit timers

- CPM

  32-Kbyte dual-port RAM

  Additional MCC host commands

- CPM multiplexing

  FCC2 can also be connected to the TC layer

- PCI bridge

  PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz

  On-chip arbitration

  Support for PCI to 60x memory and 60x memory to PCI streaming

  PCI Host Bridge or Peripheral capabilities

  Includes 4 DMA channels for the following transfers:

  - PCI-to-60x to 60x-to-PCI
  - 60x-to-PCI to PCI-to-60x
  - PCI-to-60x to PCI-to-60x
  - 60x-to-PCI to 60x-to-PCI

  Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the PC8265A) required by the PCI standard as well as message and doorbell registers

  Supports the I2O standard

  Hot-Swap friendly (supports the Hot Swap Specification as defined by PICMG 2.1 R1.0 August 3, 1998)

  Support for 66 MHz, 3.3V specification

  60x-PCI bus core logic which uses a buffer pool to allocate buffers for each port

  Makes use of the local bus signals, so there is no need for additional pins

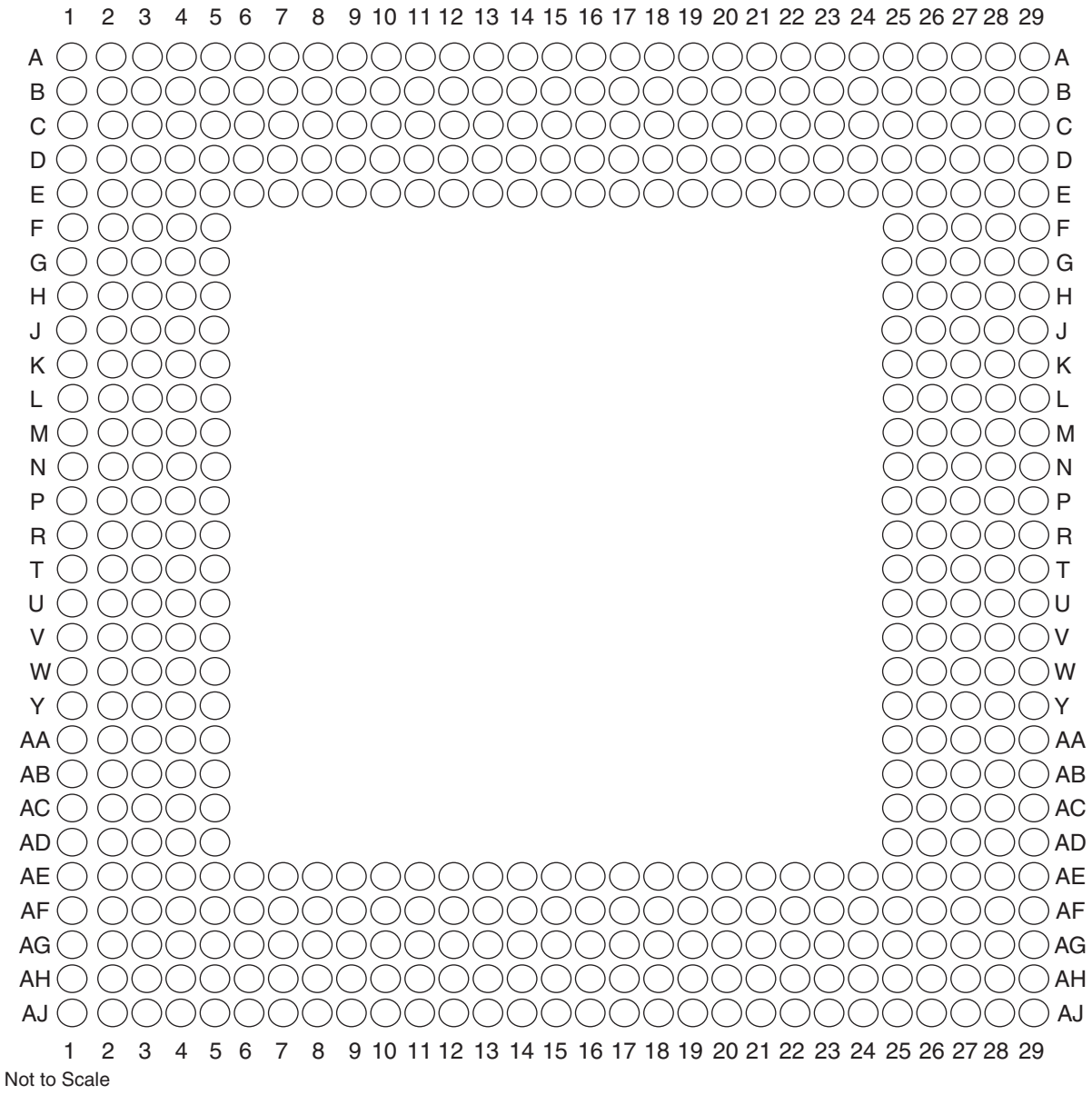
4. Pinout

This section provides the pin assignments and pinout list for the PC8265A.

4.1 Pin Assignments

Figure 4-1 shows the pinout of the PC8265A's 480 TBGA package as viewed from the top surface.

Figure 4-1. Pinout of the 480 TBGA Package as Viewed from the Top Surface



Not to Scale

Figure 4-2 shows the side profile of the TBGA package to indicate the direction of the top surface view.

Figure 4-2. Side View of the TBGA Package

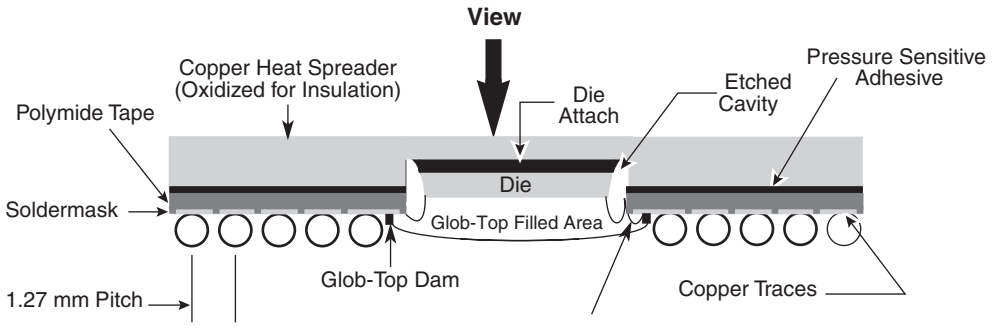


Table 4-1 shows the pinout list of the PC8265A. Table 4-2 on page 21 defines conventions and acronyms used in Table 4-1.

Table 4-1. Pinout List

Pin Name	Ball
$\overline{BR}$	W5
$\overline{BG}$	F4
$\overline{ABB}$ $\overline{IRQ2}$	E2
$\overline{TS}$	E3
A0	G1
A1	H5
A2	H2
A3	H1
A4	J5
A5	J4
A6	J3
A7	J2
A8	J1
A9	K4
A10	K3
A11	K2
A12	K1
A13	L5
A14	L4
A15	L3
A16	L2
A17	L1

Table 4-1. Pinout List (Continued)

Pin Name	Ball
A18	M5
A19	N5
A20	N4
A21	N3
A22	N2
A23	N1
A24	P4
A25	P3
A26	P2
A27	P1
A28	R1
A29	R3
A30	R5
A31	R4
TT0	F1
TT1	G4
TT2	G3
TT3	G2
TT4	F2
$\overline{\text{TBST}}$	D3
TSIZ0	C1
TSIZ1	E4
TSIZ2	D2
TSIZ3	F5
$\overline{\text{AACK}}$	F3
$\overline{\text{ARTRY}}$	E1
$\overline{\text{DBG}}$	V1
DBB $\overline{\text{IRQ3}}$	V2
D0	B20
D1	A18
D2	A16
D3	A13
D4	E12
D5	D9
D6	A6

Table 4-1. Pinout List (Continued)

Pin Name	Ball
D7	B5
D8	A20
D9	E17
D10	B15
D11	B13
D12	A11
D13	E9
D14	B7
D15	B4
D16	D19
D17	D17
D18	D15
D19	C13
D20	B11
D21	A8
D22	A5
D23	C5
D24	C19
D25	C17
D26	C15
D27	D13
D28	C11
D29	B8
D30	A4
D31	E6
D32	E18
D33	B17
D34	A15
D35	A12
D36	D11
D37	C8
D38	E7
D39	A3
D40	D18
D41	A17

Table 4-1. Pinout List (Continued)

Pin Name	Ball
D42	A14
D43	B12
D44	A10
D45	D8
D46	B6
D47	C4
D48	C18
D49	E16
D50	B14
D51	C12
D52	B10
D53	A7
D54	C6
D55	D5
D56	B18
D57	B16
D58	E14
D59	D12
D60	C10
D61	E8
D62	D6
D63	C2
DP0/$\overline{\text{RSRV}}$/$\overline{\text{EXT\_BR2}}$	B22
$\overline{\text{IRQ1}}$/DP1/$\overline{\text{EXT\_BG2}}$	A22
$\overline{\text{IRQ2}}$/DP2/$\overline{\text{TLBISYNC}}$/$\overline{\text{EXT\_DBG2}}$	E21
$\overline{\text{IRQ3}}$/DP3/$\overline{\text{CKSTP\_OUT}}$/$\overline{\text{EXT\_BR3}}$	D21
$\overline{\text{IRQ4}}$/DP4/$\overline{\text{CORE\_SRESET}}$/EXT_BG3	C21
$\overline{\text{IRQ5}}$/DP5/$\overline{\text{TBEN}}$/EXT_DBG3	B21
$\overline{\text{IRQ6}}$/DP6/CSE0	A21
$\overline{\text{IRQ7}}$/DP7/CSE1	E20
$\overline{\text{PSDVAL}}$	V3
$\overline{\text{TA}}$	C22
$\overline{\text{TEA}}$	V5
$\overline{\text{GBL}}$ $\overline{\text{IRQ1}}$	W1
$\overline{\text{CI}}$/BADDR29/$\overline{\text{IRQ2}}$	U2

Table 4-1. Pinout List (Continued)

Pin Name	Ball
$\overline{\text{WT}}$/BADDR30/$\overline{\text{IRQ3}}$	U3
$\overline{\text{L2\_HIT}}$/$\overline{\text{IRQ4}}$	Y4
$\overline{\text{CPU\_BG}}$/BADDR31/$\overline{\text{IRQ5}}$	U4
$\overline{\text{CPU\_DBG}}$	R2
$\overline{\text{CPU\_BR}}$	Y3
$\overline{\text{CS0}}$	F25
$\overline{\text{CS1}}$	C29
$\overline{\text{CS2}}$	E27
$\overline{\text{CS3}}$	E28
$\overline{\text{CS4}}$	F26
$\overline{\text{CS5}}$	F27
$\overline{\text{CS6}}$	F28
$\overline{\text{CS7}}$	G25
$\overline{\text{CS8}}$	D29
$\overline{\text{CS9}}$	E29
$\overline{\text{CS10/BCTL1}}$	F29
$\overline{\text{CS11}}$/AP0	G28
BADDR27	T5
BADDR28	U1
ALE	T2
$\overline{\text{BCTL0}}$	A27
$\overline{\text{PWE0/PSDDQM0/PBS0}}$	C25
$\overline{\text{PWE1/PSDDQM1/PBS1}}$	E24
$\overline{\text{PWE2/PSDDQM2/PBS2}}$	D24
$\overline{\text{PWE3/PSDDQM3/PBS3}}$	C24
$\overline{\text{PWE4/PSDDQM4/PBS4}}$	B26
$\overline{\text{PWE5/PSDDQM5/PBS5}}$	A26
$\overline{\text{PWE6/PSDDQM6/PBS6}}$	B25
$\overline{\text{PWE7/PSDDQM7/PBS7}}$	A25
PSDA10/PGPL0	E23
$\overline{\text{PSDWE}}$/PGPL1	B24
$\overline{\text{POE}}$/$\overline{\text{PSDRAS}}$/PGPL2	A24
$\overline{\text{PSDCAS}}$/PGPL3	B23
$\overline{\text{PGTA}}$/PUPMWAIT/PGPL4/$\overline{\text{PPBS}}$	A23
PSDAMUX/PGPL5	D22

Table 4-1. Pinout List (Continued)

Pin Name	Ball
$\overline{\text{LWE0}}$/LSDDQM0/$\overline{\text{LBS0}}$/PCI_CFG0	H28
$\overline{\text{LWE1}}$/LSDDQM1/$\overline{\text{LBS1}}$/PCI_CFG1	H27
$\overline{\text{LWE2}}$/LSDDQM2/$\overline{\text{LBS2}}$/PCI_CFG2	H26
$\overline{\text{LWE3}}$/LSDDQM3/$\overline{\text{LBS3}}$/PCI_CFG3	G29
LSDA10/LGPL0/PCI_MODCKH0	D27
$\overline{\text{LSDWE}}$/LGPL1/PCI_MODCKH1	C28
$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$/LGPL2/PCI_MODCKH2	E26
$\overline{\text{LSDCAS}}$/LGPL3/PCI_MODCKH3	D25
$\overline{\text{LGTA}}$/LUPMWAIT/LGPL4/$\overline{\text{LPBS}}$	C26
LGPL5/LSDAMUX/PCI_MODCK	B27
$\overline{\text{LWR}}$	D28
L_A14/PAR	N27
L_A15/$\overline{\text{FRAME}}$/$\overline{\text{SMI}}$	T29
L_A16/$\overline{\text{TRDY}}$	R27
L_A17/$\overline{\text{IRDY}}$/$\overline{\text{CKSTP\_OUT}}$	R26
L_A18/$\overline{\text{STOP}}$	R29
L_A19/$\overline{\text{DEVSEL}}$	R28
L_A20/IDSEL	W29
L_A21/$\overline{\text{PERR}}$	P28
L_A22/$\overline{\text{SERR}}$	N26
L_A23/$\overline{\text{REQ0}}$	AA27
L_A24/$\overline{\text{REQ1}}$/HSEJSW	P29
L_A25/$\overline{\text{GNT0}}$	AA26
L_A26/$\overline{\text{GNT1}}$/HSLED	N25
L_A27/$\overline{\text{GNT2}}$/$\overline{\text{HSENUM}}$	AA25
L_A28/$\overline{\text{RST/CORE\_SRESET}}$	AB29
L_A29/$\overline{\text{INTA}}$	AB28
L_A30/$\overline{\text{REQ2}}$	P25
L_A31/DLLOUT	AB27
LCL_D0/AD0	H29
LCL_D1/AD1	J29
LCL_D2/AD2	J28
LCL_D3/AD3	J27
LCL_D4/AD4	J26
LCL_D5/AD5	J25

Table 4-1. Pinout List (Continued)

Pin Name	Ball
LCL_D6/AD6	K25
LCL_D7/AD7	L29
LCL_D8/AD8	L27
LCL_D9/AD9	L26
LCL_D10/AD10	L25
LCL_D11/AD11	M29
LCL_D12/AD12	M28
LCL_D13/AD13	M27
LCL_D14/AD14	M26
LCL_D15/AD15	N29
LCL_D16/AD16	T25
LCL_D17/AD17	U27
LCL_D18/AD18	U26
LCL_D19/AD19	U25
LCL_D20/AD20	V29
LCL_D21/AD21	V28
LCL_D22/AD22	V27
LCL_D23/AD23	V26
LCL_D24/AD24	W27
LCL_D25/AD25	W26
LCL_D26/AD26	W25
LCL_D27/AD27	Y29
LCL_D28/AD28	Y28
LCL_D29/AD29	Y25
LCL_D30/AD30	AA29
LCL_D31/AD31	AA28
LCL_DP0/C0/$\overline{BE0}$	L28
LCL_DP1/C1/$\overline{BE1}$	N28
LCL_DP2/C2/$\overline{BE2}$	T28
LCL_DP3/C3/$\overline{BE3}$	W28
$\overline{IRQ0/NMI\_OUT}$	T1
$\overline{IRQ7/INT\_OUT/APE}$	D1
$\overline{TRST}$	AH3
TCK	AG5
TMS	AJ3

Table 4-1. Pinout List (Continued)

Pin Name	Ball
TDI	AE6
TDO	AF5
$\overline{\text{TRIS}}$	AB4
$\overline{\text{PORESET}}$	AG6
$\overline{\text{HRESET}}$	AH5
$\overline{\text{SRESET}}$	AF6
$\overline{\text{QREQ}}$	AA3
$\overline{\text{RSTCONF}}$	AJ4
MODCK1/AP1/TC0/BNKSEL0	W2
MODCK2/AP2/TC1/BNKSEL1	W3
MODCK3/AP3/TC2/BNKSEL2	W4
XFC	AB2
CLKIN1	AH4
PA0/$\overline{\text{RESTART1}}$/DREQ3/FCC2_UTM_TXADDR2	AC29[2]
PA1/$\overline{\text{REJECT1}}$/FCC2_UTM_TXADDR1/$\overline{\text{DONE3}}$	AC25[2]
PA2/CLK20/FCC2_UTM_TXADDR0/$\overline{\text{DACK3}}$	AE28[2]
PA3/CLK19/FCC2_UTM_RXADDR0/$\overline{\text{DACK4}}$/ L1RXD1A2	AG29[2]
PA4/$\overline{\text{REJECT2}}$/FCC2_UTM_RXADDR1/$\overline{\text{DONE4}}$	AG28[2]
PA5/$\overline{\text{RESTART2}}$/DREQ4/FCC2_UTM_RXADDR2	AG26[2]
PA6/L1RSYNCA1	AE24[2]
PA7/SMSYN2/L1TSYNCA1/L1GNTA1	AH25[2]
PA8/SMRXD2/L1RXD0A1/L1RXDA1	AF23[2]
PA9/SMTXD2/L1TXD0A1	AH23[2]
PA10/FCC1_UT8_RXD0/FCC1_UT16_RXD8/MSNUM 5	AE22[2]
PA11/FCC1_UT8_RXD1/FCC1_UT16_RXD9/MSNUM 4	AH22[2]
PA12/FCC1_UT8_RXD2/FCC1_UT16_RXD10/MSNU M3	AJ21[2]
PA13/FCC1_UT8_RXD3/FCC1_UT16_RXD11/MSNU M2	AH20[2]
PA14/FCC1_UT8_RXD4/FCC1_UT16_RXD12/FCC1_ RXD3	AG19[2]
PA15/FCC1_UT8_RXD5/FCC1_UT16_RXD13/FCC1_ RXD2	AF18[2]
PA16/FCC1_UT8_RXD6/FCC1_UT16_RXD14/FCC1_ RXD1	AF17[2]

Table 4-1. Pinout List (Continued)

Pin Name	Ball
PA17/FCC1_UT8_RXD7/FCC1_UT16_RXD15 FCC1_RXD0/FCC1_RXD	AE16(2)
PA18/FCC1_UT8_TXD7/FCC1_UT16_TXD15/FCC1_TXD0/FCC1_TXD	AJ16(2)
PA19/FCC1_UT8_TXD6/FCC1_UT16_TXD14/FCC1_TXD1	AG15(2)
PA20/FCC1_UT8_TXD5/FCC1_UT16_TXD13/FCC1_TXD2	AJ13(2)
PA21/FCC1_UT8_TXD4/FCC1_UT16_TXD12/FCC1_TXD3	AE13(2)
PA22/FCC1_UT8_TXD3/FCC1_UT16_TXD11	AF12(2)
PA23/FCC1_UT8_TXD2/FCC1_UT16_TXD10	AG11(2)
PA24/FCC1_UT8_TXD1/FCC1_UT16_TXD9/MSNUM 1	AH9(2)
PA25/FCC1_UT8_TXD0/FCC1_UT16_TXD8/MSNUM 0	AJ8(2)
PA26/FCC1_UTM_RXCLAV/FCC1_UTS_RXCLAV/FCC1_MII_RX_ER	AH7(2)
PA27/FCC1_UT_RXSOC/FCC1_MII_RX_DV	AF7(2)
PA28/$\overline{\text{FCC1\_UTM\_RXENB}}$/$\overline{\text{FCC1\_UTS\_RXENB}}$/FCC1_MII_TX_EN	AD5(2)
PA29/FCC1_UT_TXSOC/FCC1_MII_TX_ER	AF1(2)
PA30/FCC1_UTM_TXCLAV/FCC1_UTS_TXCLAV FCC1_MII_CRS/$\overline{\text{FCC1\_RTS}}$	AD3(2)
PA31/$\overline{\text{FCC1\_UTM\_TXENB}}$/$\overline{\text{FCC1\_UTS\_TXENB}}$ FCC1_MII_COL	AB5(2)
PB4/FCC3_TXD3/FCC2_UT8_RXD0 L1RSYNCA2/$\overline{\text{FCC3\_RTS}}$	AD28(2)
PB5/FCC3_TXD2/FCC2_UT8_RXD1/L1TSYNCA2 L1GNTA2	AD26(2)
PB6/FCC3_TXD1/FCC2_UT8_RXD2/L1RXDA2 L1RXD0A2	AD25(2)
PB7/FCC3_TXD0/FCC3_TXD/FCC2_UT8_RXD3 L1TXDA2/L1TXD0A2	AE26(2)
PB8/FCC2_UT8_TXD3/FCC3_RXD0/FCC3_RXD TXD3/L1RSYNCD1	AH27(2)
PB9/FCC2_UT8_TXD2/FCC3_RXD1/L1TXD2A2 L1TSYNCD1/L1GNTD1	AG24(2)
PB10/FCC2_UT8_TXD1/FCC3_RXD2/L1RXDD1	AH24(2)
PB11/FCC3_RXD3/FCC2_UT8_TXD0/L1TXDD1	AJ24(2)

Table 4-1. Pinout List (Continued)

Pin Name	Ball
PB12/FCC3_MII_CRS/L1CLKOB1/L1RSYNCC1 TXD2	AG22[2]
PB13/FCC3_MII_COL/$\overline{\text{L1RQB1}}$/L1TSYNCC1/L1GNTC1/L1TXD1A2	AH21[2]
PB14/FCC3_MII_TX_EN/RXD3/L1RXDC1	AG20[2]
PB15/FCC3_MII_TX_ER/RXD2/L1TXDC1	AF19[2]
PB16/FCC3_MII_RX_ER/L1CLKOA1/CLK18	AJ18[2]
PB17/FCC3_MII_RX_DV/L1RQA1/CLK17	AJ17[2]
PB18/FCC2_UT8_RXD4/FCC2_RXD3 L1CLKOD2/L1RXD2A2	AE14[2]
PB19/FCC2_UT8_RXD5/FCC2_RXD2 L1RQD2/L1RXD3A2	AF13[2]
PB20/FCC2_UT8_RXD6/FCC2_RXD1 L1RSYNCD2/L1TXD1A1	AG12[2]
PB21/FCC2_UT8_RXD7/FCC2_RXD0 FCC2_RXD/L1TSYNCD2/L1GNTD2/L1TXD2A1	AH11[2]
PB22/FCC2_UT8_TXD7/FCC2_TXD0 FCC2_TXD/L1RXD1A1/L1RXDD2	AH16[2]
PB23/FCC2_UT8_TXD6/FCC2_TXD1 L1RXD2A1/L1TXDD2	AE15[2]
PB24/FCC2_UT8_TXD5/FCC2_TXD2 L1RXD3A1/L1RSYNCC2	AJ9[2]
PB25/FCC2_UT8_TXD4/FCC2_TXD3 L1TSYNCC2/L1GNTC2/L1TXD3A1	AE9[2]
PB26/FCC2_MII_CRS/FCC2_UT8_TXD1/L1RXDC2	AJ7[2]
PB27/FCC2_MII_COL/FCC2_UT8_TXD0/L1TXDC2	AH6[2]
PB28/FCC2_MII_RX_ER/$\overline{\text{FCC2\_RTS}}$ L1TSYNCB2/L1GNTB2/TXD1	AE3[2]
PB29/FCC2_UTM_RXCLAV FCC2_UTS_RXCLAV L1RSYNCB2/FCC2_MII_TX_EN	AE2[2]
PB30/FCC2_MII_RX_DV/FCC2_UT_TXSOC L1RXDB2	AC5[2]
PB31/FCC2_MII_TX_ER/FCC2_UT_RXSOC L1TXDB2	AC4[2]
PC0/DREQ1/BRGO7/$\overline{\text{SMSYN2}}$/L1CLKOA2	AB26[2]
PC1/DREQ2/BRGO6/$\overline{\text{L1RQA2}}$	AD29[2]
PC2/$\overline{\text{FCC3\_CD}}$/FCC2_UT8_TXD3/$\overline{\text{DONE2}}$	AE29[2]

Table 4-1. Pinout List (Continued)

Pin Name	Ball
PC3/FCC3_CTS/FCC2_UT8_TXD2/DACK2 CTS4	AE27[2]
PC4/FCC2_UTM_RXENB/FCC2_UTS_RXENB SI2_L1ST4/FCC2_CD	AF27[2]
PC5/FCC2_UTM_TXCLAV FCC2_UTS_TXCLAV/SI2_L1ST3/FCC2_CTS	AF24[2]
PC6/FCC1_CD/L1CLKOC1 FCC1_UTM_RXADDR2/FCC1_UTS_RXADDR2 FCC1_UTM_RXCLAV1	AJ26[2]
PC7/FCC1_CTS/L1RQC1 FCC1_UTM_TXADDR2/FCC1_UTS_TXADDR2 FCC1_UTM_TXCLAV1	AJ25[2]
PC8/CD4/RENA4/FCC1_UT16_TXD0 SI2_L1ST2/CTS3	AF22[2]
PC9/CTS4/CLSN4/FCC1_UT16_TXD1 SI2_L1ST1/L1TSYNCA2/L1GNTA2	AE21[2]
PC10/CD3/RENA3/FCC1_UT16_TXD2 SI1_L1ST4/FCC2_UT8_RXD3	AF20[2]
PC11/CTS3/CLSN3/L1CLKOD1 L1TXD3A2/FCC2_UT8_RXD2	AE19[2]
PC12/CD2/RENA2/SI1_L1ST3 FCC1_UTM_RXADDR1/FCC1_UTS_RXADDR1	AE18[2]
PC13/CTS2/CLSN2 L1RQD1/FCC1_UTM_TXADDR1 FCC1_UTS_TXADDR1	AH18[2]
PC14/CD1/RENA1/FCC1_UTM_RXADDR0 FCC1_UTS_RXADDR0	AH17[2]
PC15/CTS1/CLSN1/SMTXD2 FCC1_UTM_TXADDR0/FCC1_UTS_TXADDR0	AG16[2]
PC16/CLK16/TIN4	AF15[2]
PC17/CLK15/TIN3/BRGO8	AJ15[2]
PC18/CLK14/TGATE2	AH14[2]
PC19/CLK13/BRGO7/SPICLK	AG13[2]
PC20/CLK12/TGATE1	AH12[2]
PC21/CLK11/BRGO6	AJ11[2]
PC22/CLK10/DONE1	AG10[2]
PC23/CLK9/BRGO5/DACK1	AE10[2]
PC24/FCC2_UT8_TXD3/CLK8/TOUT4	AF9[2]
PC25/FCC2_UT8_TXD2/CLK7/BRGO4	AE8[2]

Table 4-1. Pinout List (Continued)

Pin Name	Ball
PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK	AJ6[2]
PC27/FCC3_TXD/FCC3_TXD0/CLK5/BRGO3	AG2[2]
PC28/CLK4/TIN1/$\overline{\text{TOUT2}}$/$\overline{\text{CTS2}}$/CLSN2	AF3[2]
PC29/CLK3/TIN2/BRGO2/$\overline{\text{CTS1}}$/CLSN1	AF2[2]
PC30/FCC2_UT8_TXD3/CLK2/$\overline{\text{TOUT1}}$	AE1[2]
PC31/CLK1/BRGO1	AD1[2]
PD4/BRGO8/L1TSYNCD1/L1GNTD1 $\overline{\text{FCC3\_RTS}}$/SMRXD2	AC28[2]
PD5/FCC1_UT16_TXD3/$\overline{\text{DONE1}}$	AD27[2]
PD6/FCC1_UT16_TXD4/$\overline{\text{DACK1}}$	AF29[2]
PD7/SMSYN1/FCC1_UTM_TXADDR3 FCC1_UTS_TXADDR3/FCC2_UTM_TXADDR4 FCC1_TXCLAV2	AF28[2]
PD8/SMRXD1/FCC2_UT_TXPRTY/BRGO5	AG25[2]
PD9/SMTXD1/FCC2_UT_RXPRTY/BRGO3	AH26[2]
PD10/L1CLKOB2/FCC2_UT8_RXD1 L1RSYNCB1/BRGO4	AJ27[2]
PD11/$\overline{\text{L1RQB2}}$/FCC2_UT8_RXD0 L1TSYNCB1/L1GNTB1	AJ23[2]
PD12/SI1_L1ST2/L1RXDB1	AG23[2]
PD13/SI1_L1ST1/L1TXDB1	AJ22[2]
PD14/FCC1_UT16_RXD0/L1CLKOC2/I2CSCL	AE20[2]
PD15/FCC1_UT16_RXD1/$\overline{\text{L1RQC2}}$/I2CSDA	AJ20[2]
PD16/FCC1_UT_TXPRTY/L1TSYNCC1 L1GNTC1/SPIMISO	AG18[2]
PD17/FCC1_UT_RXPRTY/BRGO2/SPIMOSI	AG17[2]
PD18/FCC1_UTM_RXADDR4 FCC1_UTS_RXADDR4/FCC1_UTM_RXCLAV3 FCC2_UTM_RXADDR3/SPICLK	AF16[2]
PD19/FCC1_UTM_TXADDR4 FCC1_UTS_TXADDR4/FCC1_UTM_TXCLAV3 FCC2_UTM_TXADDR3/SPISEL/BRGO1	AH15[2]
PD20/$\overline{\text{RTS4}}$/TENA4 FCC1_UT16_RXD2/L1RSYNCA2	AJ14[2]
PD21/TXD4/FCC1_UT16_RXD3 L1RXD0A2/L1RXDA2	AH13[2]
PD22/RXD4/FCC1_UT16_TXD5/L1TXD0A2/L1TXDA2	AJ12[2]
PD23/$\overline{\text{RTS3}}$/TENA3/FCC1_UT16_RXD4/L1RSYNCD1	AE12[2]

Table 4-1. Pinout List (Continued)

Pin Name	Ball
PD24/TXD3/FCC1_UT16_RXD5/L1RXDD1	AF10[2]
PD25/RXD3/FCC1_UT16_TXD6/L1TXDD1	AG9[2]
PD26/$\overline{\text{RTS2}}$/TENA2/FCC1_UT16_RXD6/L1RSYNCC1	AH8[2]
PD27/TXD2/FCC1_UT16_RXD7/L1RXDC1	AG7[2]
PD28/RXD2/FCC1_UT16_TXD7/L1TXDC1	AE4[2]
PD29/$\overline{\text{RTS1}}$/TENA1/FCC1_UTM_RXADDR3 FCC1_UTS_RXADDR3/FCC1_UTM_RXCLAV2 FCC2_UTM_RXADDR4	AG1[2]
PD30/$\overline{\text{FCC2\_UTM\_TXENB/FCC2\_UTS\_TXENB}}$/TXD1	AD4[2]
PD31/RXD1	AD2[2]
SYN	AB3
SYN1	B9
GNDSYN	AB1
CLKIN2[1]	AE11
SPARE4[3]	U5
$\overline{\text{PCI\_MODE}}$[4]	AF25
SPARE6[3]	V4
THERMAL0[5]	AA1
THERMAL1[5]	AG4
I/O Power	AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5
Core Power	U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground	AA5, AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3

Notes:
1. This pin should be used as CLKIN2.
2. The default configuration of the CPM pins (PA[0-31], PB[4-31], PC[0-1], PD[4-31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.
3. Must be pulled down or left floating.
4. This pin should be asserted if the PCI function is desired or pulled up or left floating if PCI is not desired.
5. For information on how to use this pin, refer to *MPC8260 PowerQUICC II Thermal Resistor Guide* available at www.freescale.com/semiconductors.

Symbols used in Table 4-1 are described in Table 4-2.

Table 4-2. Symbol Legend

Symbol	Meaning
OVERBAR	Signals with overbars, such as $\overline{TA}$, are active low
UTM	Indicates that a signal is part of the UTOPIA master interface
UTS	Indicates that a signal is part of the UTOPIA slave interface
UT8	Indicates that a signal is part of the 8-bit UTOPIA interface
UT16	Indicates that a signal is part of the 16-bit UTOPIA interface
MII	Indicates that a signal is part of the media independent interface

5. Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the PC8265A.

5.1 DC Electrical Characteristics

This section describes the DC electrical characteristics for the PC8265A. Following table shows the maximum electrical ratings.

5.1.1 Absolute Maximum Ratings(1)

Rating	Symbol	Value	Unit
Core supply voltage(2)	V_{DD}	-0.3 to +2.5	V
PLL supply voltage(2)	SYN	-0.3 to +2.5	V
I/O supply voltage(3)	V_{DDH}	-0.3 to + 4.0	V
Input voltage(4)	V_{IN}	GND(-0.3) to +3.6	V
Storage temperature range	T_{STG}	-55 to +150	°C

Notes:
1. Absolute maximum ratings are stress ratings only; functional operation at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.
2. Caution: VDD/SYN must not exceed V_{DDH} by more than 0.4V at any time, including during power-on reset.
3. Caution: V_{DDH} can exceed VDD/SYN by 3.3V during power on reset by no more than 100 ms. V_{DDH} should not exceed VDD/SYN by more than 2.5V during normal operation.
4. Caution: V_{IN} must not exceed V_{DDH} by more than 2.5V at any time, including during power-on reset.

Following table lists recommended operational voltage conditions.

5.1.2 Recommended Operating Conditions(1)

Rating	Symbol	Value			Unit
Core supply voltage	V_{DD}	1.7 to 1.9(2)	1.7 to 2.1(3)	1.9 to 2.2(4)	V
PLL supply voltage	SYN	1.7 to 1.9(2)	1.7 to 2.1(3)	1.9 to 2.2(4)	V
CPU minimum frequency	Fmin	150	190	190	MHz
I/O supply voltage	V_{DDH}	3.135 – 3.465			V

5.1.2 Recommended Operating Conditions[1] (Continued)

Rating	Symbol	Value	Unit
Input voltage	V_{IN}	GND (-0.3) – 3.465	V
Tjunction	T_J	+125	°C
Tambiant	T_{amb}	-55	°C

Notes: 1. Caution: These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

2. CPU frequency less than or equal to 200 MHz.
3. CPU frequency greater than 200 MHz but less than or equal 233 MHz.
4. CPU frequency greater than 233 MHz.

Note: V_{DDH}, V_{CCSYN} and V_{DD} must track each other and both must vary in the same direction – in the positive direction (+5% and +0.1 V_{DC}) or in the negative direction (-5% and -0.1 V_{DC}).

This device contains circuitry protection against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

Table 5-1 shows DC Electrical Characteristics

Table 5-1. DC Electrical Characteristics[1]

Characteristic	Symbol	Min	Max	Unit
Input high voltage, all inputs except CLKIN	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
CLKIN input high voltage	V_{IHC}	2.4	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0.4	V
Input leakage current, $V_{IN} = V_{DDH}$	I_{IN}	–	10	µA
Hi-Z (off state) leakage current, $V_{IN} = V_{DDH}$	I_{OZ}	–	10	µA
Signal low input current, $V_{IL} = 0.8V$	I_L	–	1	µA
Signal high input current, $V_{IH} = 2.0V$	I_H	–	1	µA
Output high voltage, $I_{OH} = -2$ mA except XFC, UTOPIA mode, and open drain pins In UTOPIA mode: $I_{OH} = -8.0$ mA PA[0-31] PB[4-31] PC[0-31] PD[4-31]	V_{OH}	2.4	–	V
In UTOPIA mode: $I_{OL} = 8.0$ mA PA[0-31] PB[4-31] PC[0-31] PD[4-31]	V_{OL}	–	0.5	V

Table 5-1. DC Electrical Characteristics[1] (Continued)

Characteristic	Symbol	Min	Max	Unit
IOL = 7.0 mA BR BG ABB/IRQ2 TS A[0-31] TT[0-4] TBST TSIZE[0–3] AACK ARTRY DBG	V_{OL}	–	0.4	V
DBB/IRQ3 D[0-63] DP(0)/RSRV/EXT_BR2 DP(1)/IRQ1/EXT_BG2 DP(2)/TLBISYNC/IRQ2/EXT_DBG2 DP(3)/IRQ3/EXT_BR3/CKSTP_OUT DP(4)/IRQ4/EXT_BG3/CORE_SREST DP(5)/TBEN/IRQ5/EXT_DBG3 DP(6)/CSE(0)/IRQ6 DP(7)/CSE(1)/IRQ7 PSDVAL TA TEA GBL/IRQ1 CI/BADDR29/IRQ2 WT/BADDR30/IRQ3 L2_HIT/IRQ4 CPU_BG/BADDR31/IRQ5 CPU_DBG CPU_BR IRQ0/NMI_OUT IRQ7/INT_OUT/APE PORESET HRESET SRESET RSTCONF QREQ				

Table 5-1. DC Electrical Characteristics[1] (Continued)

Characteristic	Symbol	Min	Max	Unit
IOL = 5.3 mA $\overline{CS}$[0-9] $\overline{CS}$(10)/$\overline{BCTL1}$ $\overline{CS}$(11)/AP(0) BADDR[27–28] ALE $\overline{BCTL0}$ $\overline{PWE}$(0:7)/$\overline{PSDDQM}$(0:7)/$\overline{PBS}$(0:7) PSDA10/PGPL0 $\overline{PSDWE}$/PGPL1 $\overline{POE}$/$\overline{PSDRAS}$/PGPL2 PSDCAS/PGPL3 PGTA/PUPMWAIT/PGPL4/PPBS PSDAMUX/PGPL5 $\overline{LWE}$[0–3]$\overline{LSDDQM}$[0–3]/$\overline{LBS}$[0–3]/PCI_CFG[0–3[2] LSDA10/LGPL0/PCI_MODCKH0[2] LSDWE/LGPL1/PCI_MODCKH1[2]	V_{OL}	–	0.4	V

Table 5-1. DC Electrical Characteristics[1] (Continued)

Characteristic	Symbol	Min	Max	Unit
LOE/LSDRAS/LGPL2/PCI_MODCKH2[2] LSDCAS/LGPL3/PCI_MODCKH3[2] LGTA/LUPMWAIT/LGPL4/LPBS LSDAMUX/LGPL5/PCI_MODCK[2] LWR MODCK1/AP(1)/TC(0)/BNKSEL(0) MODCK2/AP(2)/TC(1)/BNKSEL(2) MODCK3/AP(3)/TC(2)/BNKSEL(2)				
IOL = 3.2 mA L_A14/PAR[2] L_A15/FRAME[2]/SMI L_A16/TRDY[2] L_A17/IRDY[2]/CKSTP_OUT L_A18/STOP[2] L_A19/DEVSEL[2] L_A20/IDSEL[2] L_A21/PERR[2] L_A22/SERR[2] L_A23/REQ0[2] L_A24/REQ1[2]/HSEJSW[2] L_A25/GNT0[2] L_A26/GNT1[2]/HSLED[2] L_A27/GNT2[2]/HSENUM[2] L_A28/RST[2]/CORE_SRESET L_A29/INTA[2] L_A30/REQ2[2] L_A31 LCL_D(0-31)/AD(0-31)[2] LCL_DP(0-3)/C/BE(0-3)[2] PA[0–31] PB[4–31] PC[0–31] PD[4–31] TDO				

Notes:
1. The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.
2. The leakage current is measured for nominal V_{DDH} and V_{DD} or both V_{DDH} and V_{DD} must vary in the same direction; that is, V_{DDH} and V_{DD} either both vary in the positive direction (+5% and +0.1 V_{DC}) or both vary in the negative direction (-5% and -0.1 V_{DC}).

5.1.3 Thermal Characteristics

Table 5-2 describes thermal characteristics.

Table 5-2. Thermal Characteristics for the 480 TBGA Package

Characteristics	Symbol	Value	Unit	Air Flow
Junction to ambient	Θ_{JA}	13(1)	°C/W	NC(2)
		10(1)		1 m/s
		11(3)		NC
		8(3)		1 m/s
Junction to board(4)	Θ_{JB}	4	°C/W	–
Junction to case(5)	Θ_{JC}	1.1	°C/W	–

Notes:
1. Assumes a single layer board with no thermal vias.
2. Natural convection.
3. Assumes a four layer board.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5.1.4 Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

where

T_A = ambient temperature °C
Θ_{JA} = package thermal resistance, junction to ambient, °C/W
$P_D = P_{INT} + P_{I/O}$
$P_{INT} = I_{DD} \times V_{DD}$ Watts (chip internal power)
$P_{I/O}$ = power dissipation on input and output pins (determined by user)

For most applications $P_{I/O} < 0.3 \times P_{INT}$. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is as follows:

$$P_D = K/(T_J + 273°C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

5.1.5 Layout Practices

Each pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the chip. The power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to the chip and ground should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as GND planes.

All output pins on the PC8265A have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses.

Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 5-3 provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required for conditions above P_D = 3W (when the ambient temperature is 70°C or greater) to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink.

Table 5-3. Estimated Power Dissipation for Various Configurations[1]

Bus (MHz)	CPM Multiplier	Core CPU Multiplier	CPM (MHz)	CPU (MHz)	P_{INT}(W)[2]			
					Vddl 1.8 Volts		Vddl 2.0 Volts	
					Nominal	Maximum	Nominal	Maximum
66.66	2	3	133	200	1.2	2	1.8	2.3
66.66	2.5	3	166	200	1.3	2.1	1.9	2.3
66.66	3	4	200	266	–	–	2.3	2.9
66.66	3	4.5	200	300	–	–	2.4	3.1
83.33	2	3	166	250	–	–	2.2	2.8
83.33	2	3	166	250	–	–	2.2	2.8
83.33	2.5	3.5	208	291	–	–	2.4	3.1

Notes: 1. Test temperature = room temperature (25°C)

2. $P_{INT} = I_{DD} \times V_{DD}$ Watts (chip internal power)

5.2 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for the 66 MHz PC8265A device. Note that AC timings are based on a 50-pf load. Typical output buffer impedances are shown in Table 5-4.

Table 5-4. Output Buffer Impedances[1]

Output Buffers	Typical Impedance (Ω)
60x bus	40
Local bus	40
Memory Controller	40
Parallel I/O	46
PCI	25

Note: 1. These are typical values at 65°C. The impedance may vary by ±25% with process and temperature.

Table 5-5 lists CPM output characteristics.

Table 5-5. AC Characteristics for CPM Outputs[1]

Spec_num Max/Min	Characteristic	Max Delay (ns)		Min Delay (ns)	
		66 MHz	83 MHz	66 MHz	83 MHz
sp36a/sp37a	FCC outputs – internal clock (NMSI)	6	5.5	1	1
sp36b/sp37b	FCC outputs – external clock (NMSI)	14	12	2	1
sp40/sp41	TDM outputs/SI	25	16	5	4
sp38a/sp39a	SCC/SMC/SPI/I2C outputs – internal clock (NMSI)	19	16	1	0.5
sp38b/sp39b	Ex_SCC/SMC/SPI/I2C outputs – external clock (NMSI)	19	16	2	1
sp42/sp43	TIMER/IDMA outputs	14	11	1	0.5
sp42a/sp43a	PIO outputs	14	11	0.5	0.5

Note: 1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Table 5-6 lists CPM input characteristics.

Table 5-6. AC Characteristics for CPM Inputs[1]

Spec_num	Characteristic	Setup (ns)		Hold (ns)	
		66 MHz	83 MHz	66 MHz	83 MHz
sp16a/sp17a	FCC inputs – internal clock (NMSI)	10	8	0	0
sp16b/sp17b	FCC inputs – external clock (NMSI)	3	2.5	3	2
sp20/sp21	TDM inputs/SI	15	12	12	10
sp18a/sp19a	SCC/SMC/SPI/I2C inputs – internal clock (NMSI)	20	16	0	0
sp18b/sp19b	SCC/SMC/SPI/I2C inputs – external clock (NMSI)	5	4	5	4
sp22/sp23	PIO/TIMER/IDMA inputs	10	8	3	3

Note: 1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 5-1 shows the FCC external clock.

Figure 5-1. FCC External Clock Diagram

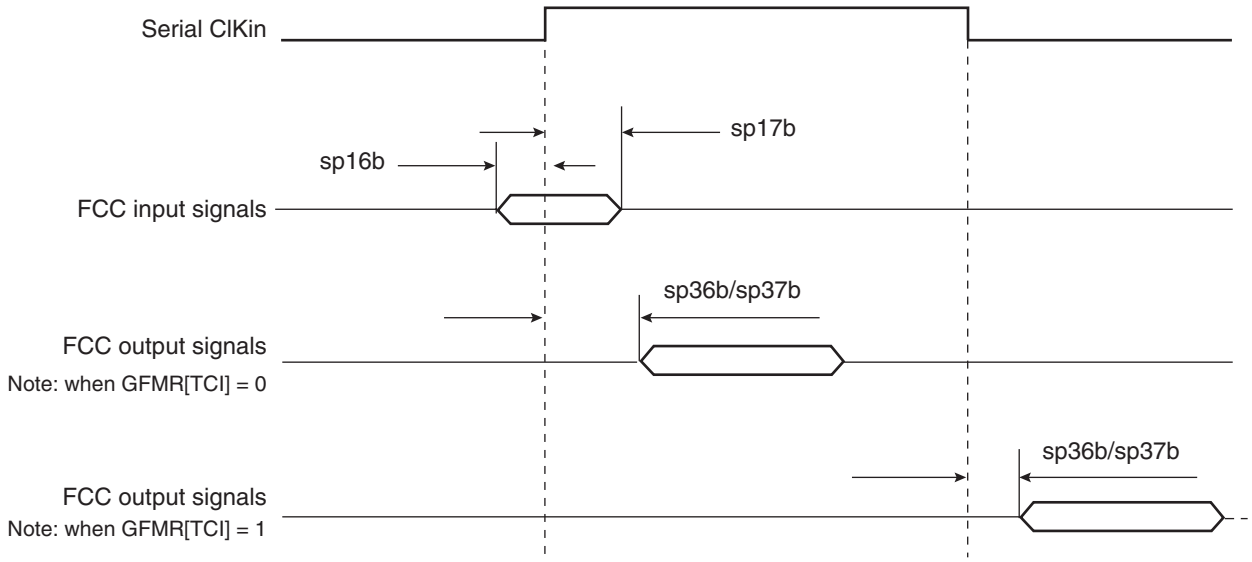


Figure 5-2 shows the FCC internal clock.

Figure 5-2. FCC Internal Clock Diagram

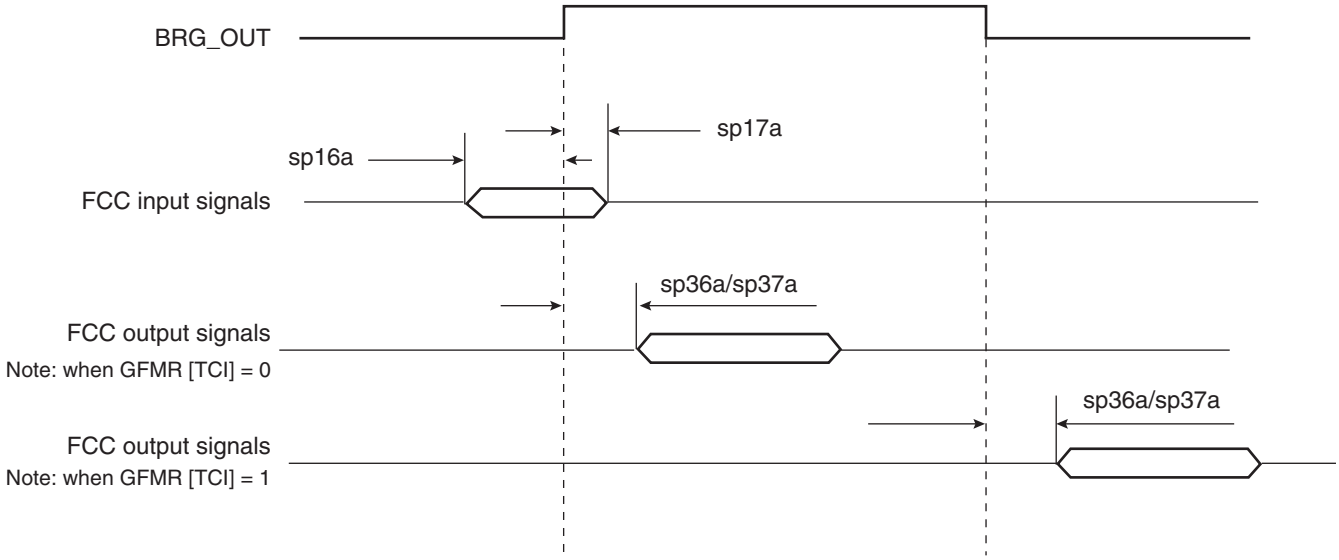
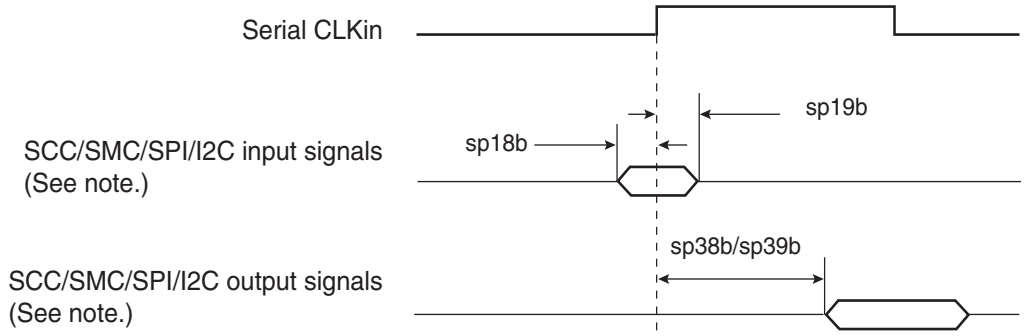


Figure 5-3 shows the SCC/SMC/SPI/I²C external clock.

Figure 5-3. SCC/SMC/SPI/I²C External Clock Diagram

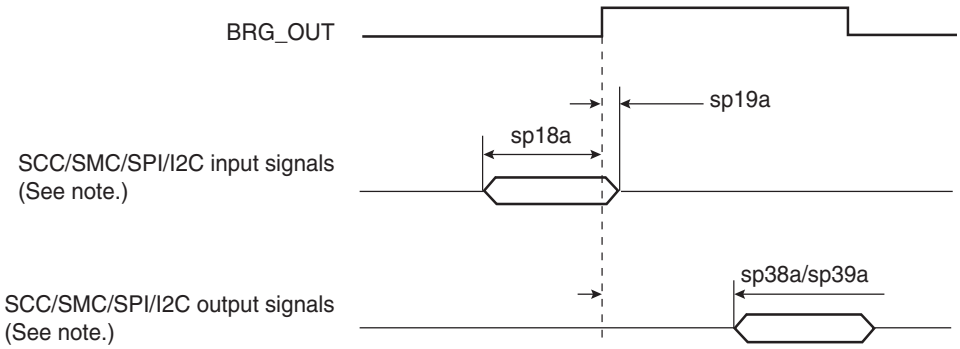


Note: The clock edge is selectable on SCC and SPI.

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 5-4 shows the SCC/SMC/SPI/I²C internal clock.

Figure 5-4. SCC/SMC/SPI/I²C Internal Clock Diagram

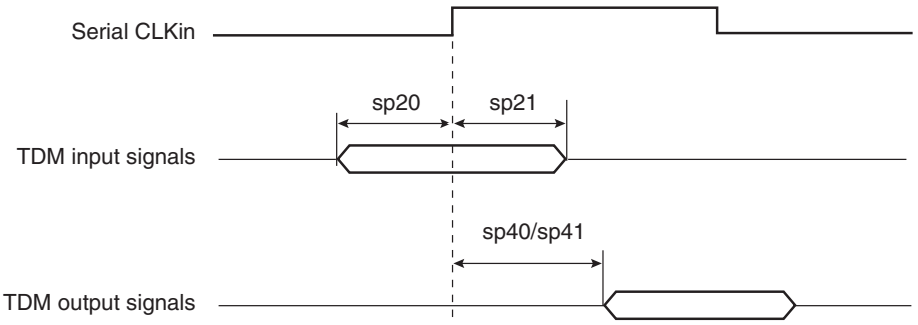


Note: There are four possible TDM timing conditions:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 5-5 shows TDM input and output signals.

Figure 5-5. TDM Signals Diagram

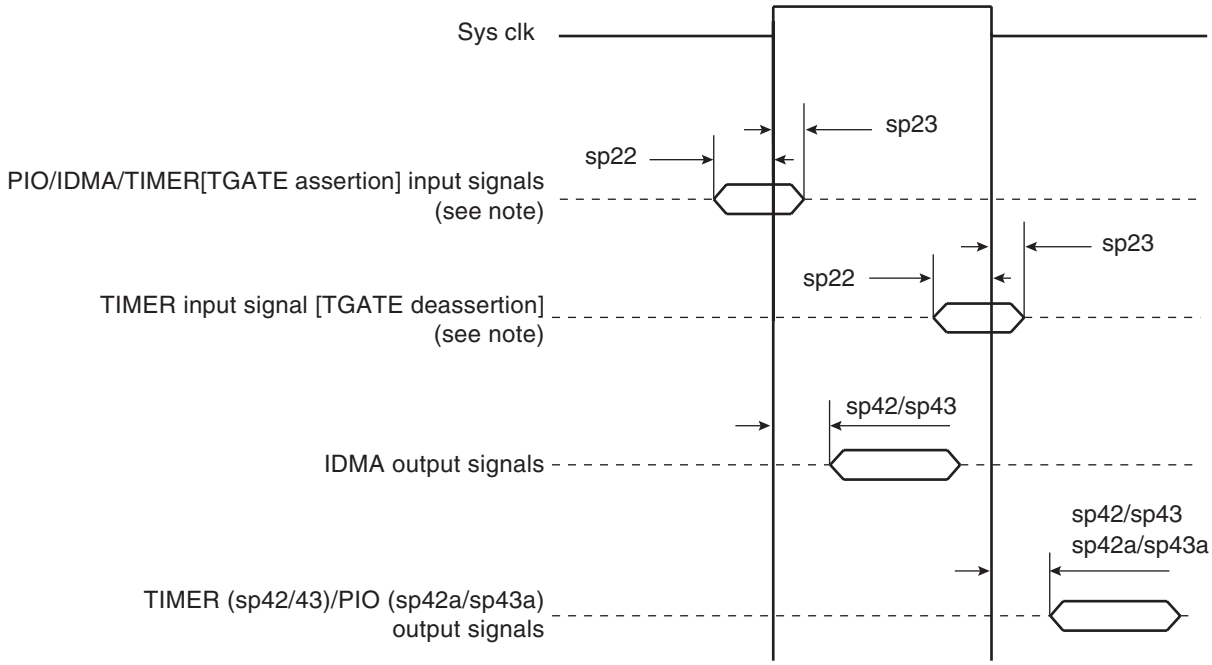


Note: There are four possible TDM timing conditions:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 5-6 shows PIO, timer, and DMA signals.

Figure 5-6. PIO, Timer, and DMA Signal Diagram



Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

Table 5-7 lists SIU input characteristics.

Table 5-7. AC Characteristics for SIU Inputs[1]

Spec Number			Setup (ns)		Hold (ns)	
Min	**Max**	**Characteristic**	**66 MHz**	**83 MHz**	**66 MHz**	**83 MHz**
sp11	sp10	$\overline{AACK}/\overline{ARTRY}/\overline{TA}/\overline{TS}/\overline{TEA}/\overline{DBG}/\overline{BG}/\overline{BR}$	6	5	0.5	0.5
sp12	sp10	Data bus in normal mode	5	4	0.5	0.5
sp13	sp10	Data bus in ECC and PARITY modes	8	6	0.5	0.5
sp14	sp10	DP pins	7	6	0.5	0.5
sp15	sp10	All other pins	5	4	0.5	0.5

Note: 1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Table 5-8 lists SIU output characteristics.

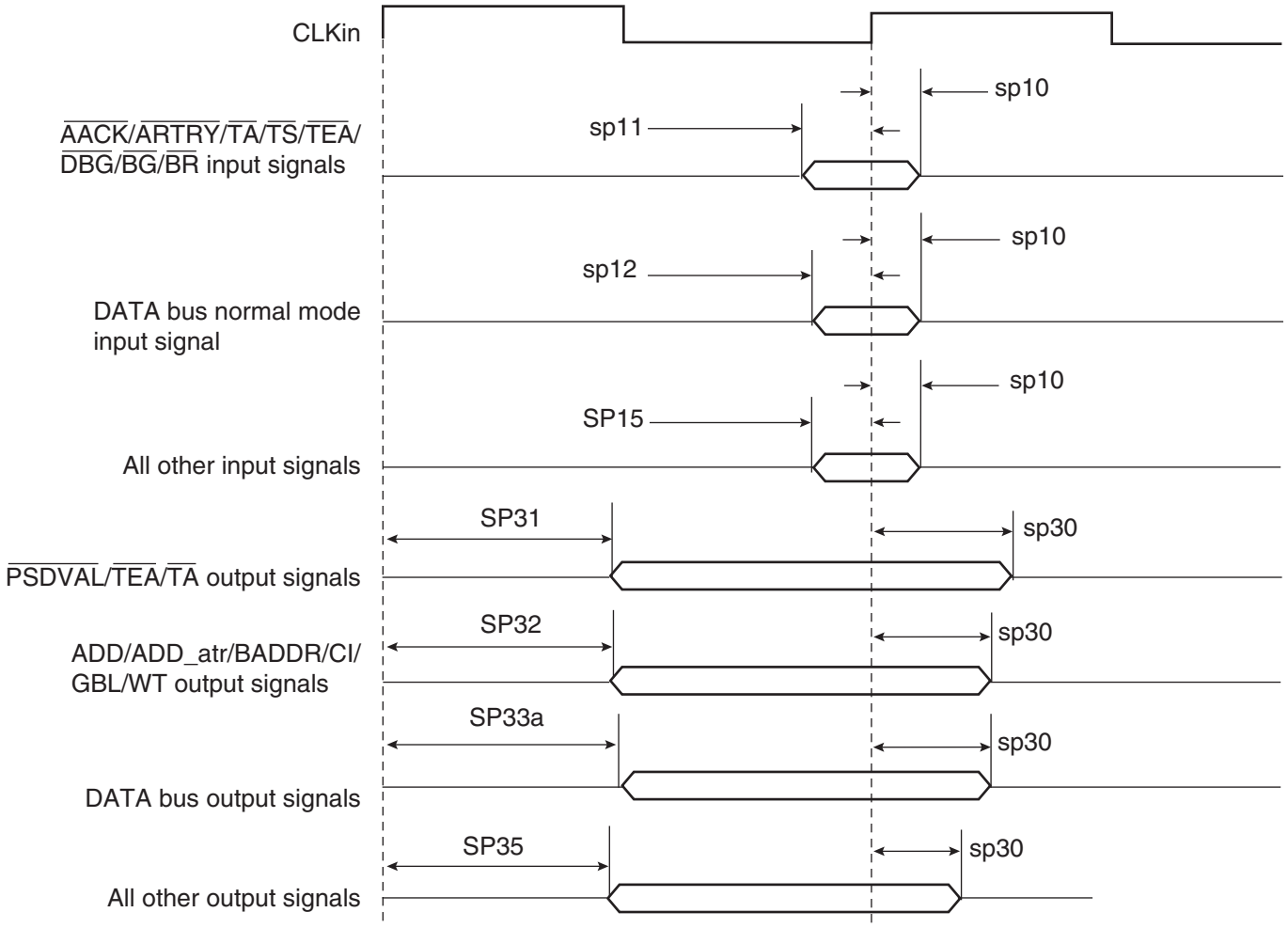
Table 5-8. AC Characteristics for SIU Outputs[1]

Spec Number			Setup (ns)		Hold (ns)	
Min	**Max**	**Characteristic**	**66 MHz**	**83 MHz**	**66 MHz**	**83 MHz**
sp31	sp30	$\overline{PSDVAL}/\overline{TEA}/\overline{TA}$	7	6	0.5	0.5
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	0.5	0.5
sp33a	sp30	Data bus	6.5	6.5	0.5	0.5
sp33b	sp30	DP	8	7	0.5	0.5
sp34	sp30	Memory controller signals/ALE	6	5	0.5	0.5
sp35	sp30	All other signals	6	5.5	0.5	0.5

Note: 1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Figure 5-7 shows the interaction of several bus signals.

Figure 5-7. Bus Signals



Note: Activating data pipelining (setting BR × [DR] in the memory controller) improves the AC timing. When data pipelining is activated, sp12 can be used for data bus setup even when ECC or PARITY are used. Also, sp33a can be used as the AC specification for DP signals.

Figure 5-8 shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).

Figure 5-8. Parity Mode Diagram

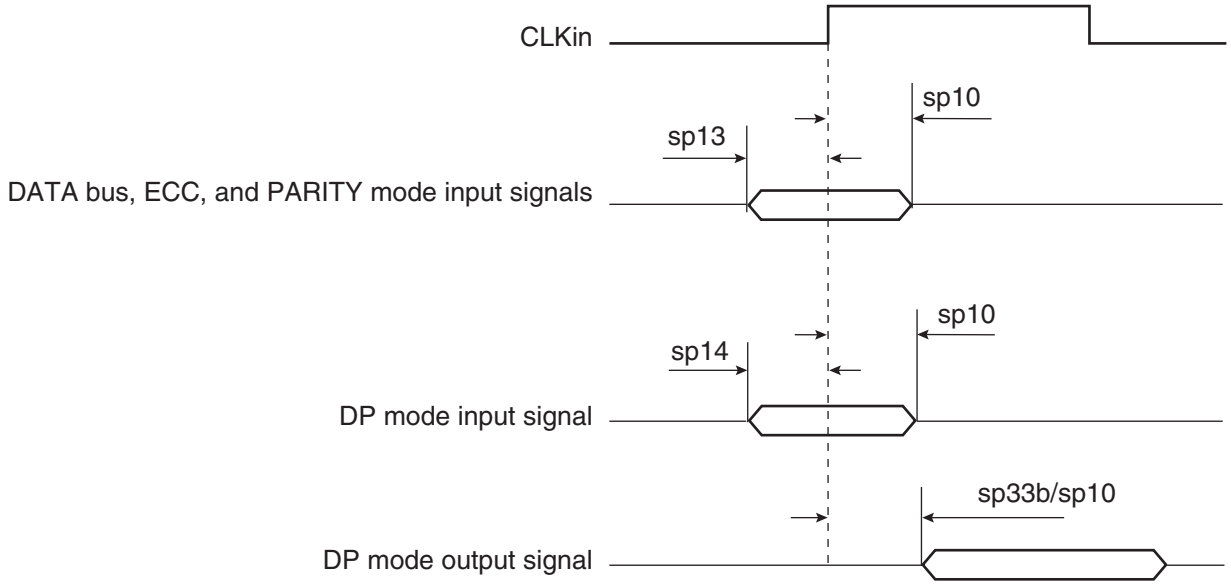
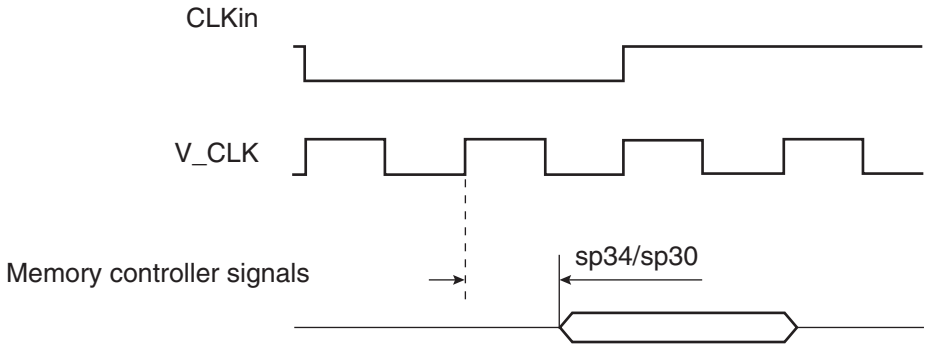


Figure 5-9 shows signal behavior in MEMC mode.

Figure 5-9. MEMC Mode Diagram



Note: Generally, all PC8265A bus and system output signals are driven from the rising edge of the input clock (CLKin). Memory controller signals, however, trigger on four points within a CLKin cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKin. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 5-9.

Table 5-9. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKin)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKin	1/2 CLKin	3/4 CLKin
1:2.5	3/10 CLKin	1/2 CLKin	8/10 CLKin
1:3.5	4/14 CLKin	1/2 CLKin	11/14 CLKin

Figure 5-10 is a graphical representation of Table 5-9.

Figure 5-10. Internal Tick Spacing for Memory Controller Signals

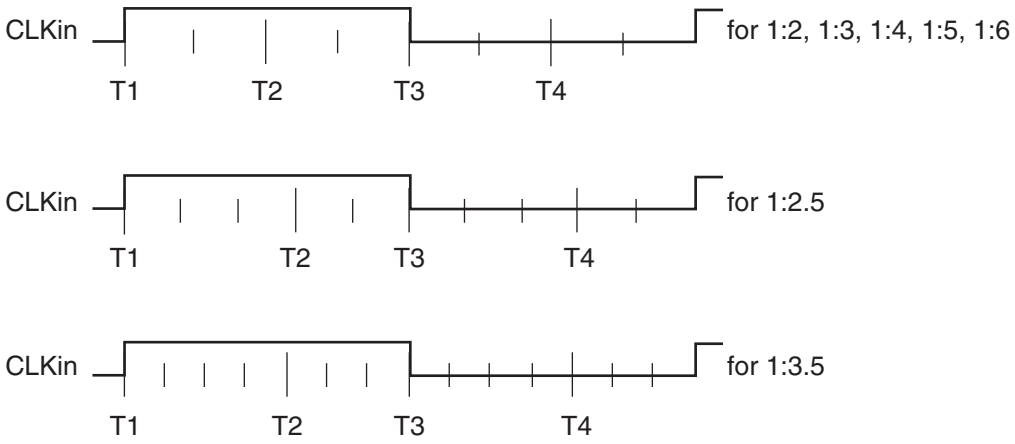


Table 5-10 lists the JTAG timings.

Table 5-10. JTAG Timings[1]

Parameter	Symbol	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	25	MHz	
JTAG external clock cycle time	t_{JTG}	40	–	ns	
JTAG external clock pulse width measured at 1.4V	t_{JTKHKL}	20	–	ns	
JTAG external clock rise and fall	t_{JTGR} and t_{JTGF}	0	5	ns	(6)
TRST assert time	t_{TRST}	25	–	ns	(3)(6)
Input setup times - Boundary-scan data - TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 – –	 ns ns	 (4)(7) (4)(7)
Input hold times - Boundary-scan data - TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 – –	 ns ns	 (4)(7) (4)(7)

Table 5-10. JTAG Timings[1]

Parameter	Symbol	Min	Max	Unit	Notes
Output valid times - Boundary-scan data - TDO	 t_{JTKLDV} t_{JTKLOV}	 – –	 25 25	 ns ns	 (5)(7) (5)(7)
Output hold times Boundary-scan data TDO	t_{JTKLDX} t_{JTKLOX}	1 1	– –	ns ns	(5)(7) (5)(7)
JTAG external clock to output high impedance - Boundary-scan data - TDO	t_{JTKLDZ} t_{JTKLOZ}	1 1	25 25	ns ns	(5)(6) (5)(6)

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω. load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design.
7. Guaranteed by design and device characterization.

Note: The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin's rising edge.

5.3 Clock Configuration Modes

To configure the main PLL multiplication factor and the core, the CPM, and 60x bus frequencies, the MODCK[1:3] pins are sampled while $\overline{\text{HRESET}}$ is asserted. Table 5-11 shows the eight basic configuration modes. Another 49 modes are available by using the configuration pin ($\overline{\text{RSTCONF}}$) and driving four pins on the data bus.

5.3.1 Local Bus Mode

Table 5-11 describes default clock modes for the PC8265A.

Table 5-11. Clock Default Modes

MODCK[1–3]	Input Clock Frequency (MH)z	CPM Multiplication Factor	CPM Frequency (MHz)	Core Multiplication Factor	Core Frequency (MHz)
000	33	3	100	4	133
001	33	3	100	5	166
010	33	4	133	4	133
011	33	4	133	5	166

Table 5-11. Clock Default Modes (Continued)

MODCK[1–3]	Input Clock Frequency (MH)z	CPM Multiplication Factor	CPM Frequency (MHz)	Core Multiplication Factor	Core Frequency (MHz)
100	66	2	133	2.5	166
101	66	2	133	3	200
110	66	2.5	166	2.5	166
111	66	2.5	166	3	200

Table 5-12 describes all possible clock configurations when using the hard reset configuration sequence.

Note that the clock configuration changes only after $\overline{\text{POR}}$ is asserted. Note also that basic modes are shown in boldface type.

Table 5-12. Clock Configuration Modes[1]

MODCK_H–MODCK[1–3]	Input Clock Frequency[2][3] (MHz)	CPM Multiplication Factor[2]	CPM Frequency[2] (MHz)	Core Multiplication Factor[2]	Core Frequency[2] (MHz)
0001_000	33	2	66	4	133
0001_001	33	2	66	5	166
0001_010	33	2	66	6	200
0001_011	33	2	66	7	233
0001_100	33	2	66	8	266
0001_101	33	3	100	4	133
0001_110	33	3	100	5	166
0001_111	33	3	100	6	200
0010_000	33	3	100	7	233
0010_001	33	3	100	8	266
0010_010	**33**	**4**	**133**	**4**	**133**
0010_011	**33**	**4**	**133**	**5**	**166**
0010_100	33	4	133	6	200
0010_101	33	4	133	7	233
0010_110	33	4	133	8	266
0010_111	33	5	166	4	133
0011_000	33	5	166	5	166
0011_001	33	5	166	6	200
0011_010	33	5	166	7	233
0011_011	33	5	166	8	266

Table 5-12. Clock Configuration Modes[1] (Continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency[2][3] (MHz)	CPM Multiplication Factor[2]	CPM Frequency[2] (MHz)	Core Multiplication Factor[2]	Core Frequency[2] (MHz)
0011_100	33	6	200	4	133
0011_101	33	6	200	5	166
0011_110	33	6	200	6	200
0011_111	33	6	200	7	233
0100_000	33	6	200	8	266
0100_001	Reserved				
0100_010					
0100_011					
0100_100					
0100_101					
0100_110					
0100_111	Reserved				
0101_000					
0101_001					
0101_010					
0101_011					
0101_100					
0101_101	66	2	133	2	133
0101_110	**66**	**2**	**133**	**2.5**	**166**
0101_111	**66**	**2**	**133**	**3**	**200**
0110_000	66	2	133	3.5	233
0110_001	66	2	133	4	266
0110_010	66	2	133	4.5	300
0110_011	66	2.5	166	2	133
0110_100	**66**	**2.5**	**166**	**2.5**	**166**
0110_101	**66**	**2.5**	**166**	**3**	**200**
0110_110	66	2.5	166	3.5	233
0110_111	66	2.5	166	4	266
0111_000	66	2.5	166	4.5	300

Table 5-12. Clock Configuration Modes[1] (Continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency[2][3] (MHz)	CPM Multiplication Factor[2]	CPM Frequency[2] (MHz)	Core Multiplication Factor[2]	Core Frequency[2] (MHz)
0111_001	66	3	200	2	133
0111_010	66	3	200	2.5	166
0111_011	**66**	3	200	**3**	**200**
0111_100	66	3	200	3.5	233
0111_101	66	3	200	4	266
0111_110	66	3	200	4.5	300
0111_111	66	3.5	233	2	133
1000_000	66	3.5	233	2.5	166
1000_001	66	3.5	233	3	200
1000_010	66	3.5	233	3.5	233
1000_011	66	3.5	233	4	266
1000_100	66	3.5	233	4.5	300

Notes:
1. Because of speed dependencies, not all of the possible configurations in Table 5-12 are applicable.
2. The user should choose the input clock frequency and the multiplication factors such that the frequency of the CPU is equal to or greater than150 MHz and the CPM ranges between 66 – 233 MHz.
3. Input clock frequency is given only for the purpose of reference. MODCK_H–MODCK_L should be set so that the resulting configuration does not exceed the frequency rating of the user's part.

Example. If a part is rated at 266 MHz CPU, 200 MHz CPM, and 66 MHz bus, any of the following are possible (note that the three input clock frequencies are only three of many possible input clock frequencies):

1. 66 MHz input clock and MODCK_H–MODCK_L[0111–101] (with a core multiplication factor of 4 and a CPM multiplication factor of 3). The resulting configuration equals the part's maximum possible frequencies of 266 MHz CPU, 200 MHz CPM, and 66 MHz bus.
2. 50 MHz input clock and MODCK_H–MODCK_L[0111–101] to achieve a configuration of 200 MHz CPU, 150 MHz CPM, and 50 MHz bus.
3. 40 MHz input clock and MODCK_H–MODCK_L[0010–011] to achieve a configuration of 200 MHz CPU, 160 MHz CPM, and 40 MHz bus.

Note that with each example, any one of several values for MODCK_H–MODCK_L could possibly be used as long as the resulting configuration does not exceed the part's rating.

5.4 PCI Mode

The PC8265 has three clocking modes: local, PCI host, and PCI agent. The clocking mode is set according to three input pins: PCI_MODE, PCI_CFG[0], PCI_MODCK, as shown in Table 5-13.

Table 5-13. PC8265 Clocking Modes

Pins			Clocking Mode	PCI Clock Frequency Range (MHz)
PCI_MODE	PCI_CFG[0]	PCI_MODCK		
1	–	–	Local bus	–
0	0	0	PCI host	50-66
0	0	1		25-50
0	1	0	PCI agent	50-66
0	1	1		25-50

In addition, note the following:

Notes:
1. PCI_MODCK
   In PCI mode only, PCI_MODCK comes from the LGPL5 pin and MODCK_H[0–3] comes from {LGPL0, LGPL1, LGPL2, LGPL3}.
2. Tval (Output Hold)
   The minimum Tval = 2 when PCI_MODCK = 1, and the minimum Tval = 1 when PCI_MODCK = 0. Therefore, designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.
3. Clock configurations change only after $\overline{\text{POR}}$ is asserted.

Table 5-14. Clock Default Configurations in PCI Host Mode (MODCK_HI = 0000)

MODCK[1–3](1)	Input Clock Frequency	CPM Multiplication	CPM Frequency	Core Multiplication	Core Frequency	PCI Division Factor(2)	PCI Frequency(2)
000	66 MHz	2	133 MHz	2.5	166 MHz	2/4	66/33 MHz
001	66 MHz	2	133 MHz	3	200 MHz	2/4	66/33 MHz
010	66 MHz	2.5	166 MHz	3	200 MHz	3/6	55/28 MHz
011	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
100	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
101	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
110	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
111	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz

Notes:
1. Assumes MODCK_HI = 0000.
2. The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic ‘1’), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.)

Table 5-15 describes all possible clock configurations when using the PC8265A or the PC8266A's internal PCI bridge in host mode.

Table 5-15. Clock Configuration Modes in PCI Host Mode

MODCK_H – MODCK[1–3]	Input Clock Frequency[1] (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor[2]	PCI Frequency[2]
0001_000	33 MHz	3	100 MHz	5	166 MHz	3/6	33/16 MHz
0001_001	33 MHz	3	100 MHz	6	200 MHz	3/6	33/16 MHz
0001_010	33 MHz	3	100 MHz	7	233 MHz	3/6	33/16 MHz
0001_011	33 MHz	3	100 MHz	8	266 MHz	3/6	33/16 MHz
0010_000	33 MHz	4	133 MHz	5	166 MHz	4/8	33/16 MHz
0010_001	33 MHz	4	133 MHz	6	200 MHz	4/8	33/16 MHz
0010_010	33 MHz	4	133 MHz	7	233 MHz	4/8	33/16 MHz
0010_011	33 MHz	4	133 MHz	8	266 MHz	4/8	33/16 MHz
0011_000[3]	33 MHz	5	166 MHz	5	166 MHz	5	33 MHz
0011_001[3]	33 MHz	5	166 MHz	6	200 MHz	5	33 MHz
0011_010[3]	33 MHz	5	166 MHz	7	233 MHz	5	33 MHz
0011_011[3]	33 MHz	5	166 MHz	8	266 MHz	5	33 MHz
0100_000[3]	33 MHz	6	200 MHz	5	166 MHz	6	33 MHz
0100_001[3]	33 MHz	6	200 MHz	6	200 MHz	6	33 MHz
0100_010[3]	33 MHz	6	200 MHz	7	233 MHz	6	33 MHz
0100_011[3]	33 MHz	6	200 MHz	8	266 MHz	6	33 MHz
0101_000	66 MHz	2	133 MHz	2.5	166 MHz	2/4	66/33 MHz
0101_001	66 MHz	2	133 MHz	3	200 MHz	2/4	66/33 MHz
0101_010	66 MHz	2	133 MHz	3.5	233 MHz	2/4	66/33 MHz
0101_011	66 MHz	2	133 MHz	4	266 MHz	2/4	66/33 MHz
0101_100	66 MHz	2	133 MHz	4.5	300 MHz	2/4	66/33 MHz
0110_000	66 MHz	2.5	166 MHz	2.5	166 MHz	3/6	55/28 MHz
0110_001	66 MHz	2.5	166 MHz	3	200 MHz	3/6	55/28 MHz
0110_010	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
0110_011	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
0110_100	66 MHz	2.5	166 MHz	4.5	300 MHz	3/6	55/28 MHz

Table 5-15. Clock Configuration Modes in PCI Host Mode (Continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency[1] (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor[2]	PCI Frequency[2]
0111_000	66 MHz	3	200 MHz	2.5	166 MHz	3/6	66/33 MHz
0111_001	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
0111_010	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
0111_011	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz
0111_100	66 MHz	3	200 MHz	4.5	300 MHz	3/6	66/33 MHz
1000_000	66 MHz	3	200 MHz	2.5	166 MHz	4/8	50/25 MHz
1000_001	66 MHz	3	200 MHz	3	200 MHz	4/8	50/25 MHz
1000_010	66 MHz	3	200 MHz	3.5	233 MHz	4/8	50/25 MHz
1000_011	66 MHz	3	200 MHz	4	266 MHz	4/8	50/25 MHz
1000_100	66 MHz	3	200 MHz	4.5	300 MHz	4/8	50/25 MHz
1001_000	66 MHz	3.5	233 MHz	2.5	166 MHz	4/8	58/29 MHz
1001_001	66 MHz	3.5	233 MHz	3	200 MHz	4/8	58/29 MHz
1001_010	66 MHz	3.5	233 MHz	3.5	233 MHz	4/8	58/29 MHz
1001_011	66 MHz	3.5	233 MHz	4	266 MHz	4/8	58/29 MHz
1001_100	66 MHz	3.5	233 MHz	4.5	300 MHz	4/8	58/29 MHz
1010_000	100 MHz	2	200 MHz	2	200 MHz	3/6	66/33 MHz
1010_001	100 MHz	2	200 MHz	2.5	250 MHz	3/6	66/33 MHz
1010_010	100 MHz	2	200 MHz	3	300 MHz	3/6	66/33 MHz
1010_011	100 MHz	2	200 MHz	3.5	350 MHz	3/6	66/33 MHz
1010_100	100 MHz	2	200 MHz	4	400 MHz	3/6	66/33 MHz
1011_000	100 MHz	2.5	250 MHz	2	200 MHz	4/8	62/31 MHz
1011_001	100 MHz	2.5	250 MHz	2.5	250 MHz	4/8	62/31MHz
1011_010	100 MHz	2.5	250 MHz	3	300 MHz	4/8	62/31 MHz
1011_011	100 MHz	2.5	250 MHz	3.5	350 MHz	4/8	62/31 MHz
1011_100	100 MHz	2.5	250 MHz	4	400 MHz	4/8	62/31 MHz

Notes: 1. Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.

Example. If a part is rated at 266 MHz CPU, 200 MHz CPM, and 66 MHz bus, any of the following are possible (note that the three input clock frequencies are only three of many possible input clock frequencies):

1. 66 MHz input clock, MODCK_H–MODCK_L[0111–011] (with a core multiplication factor of 4 and a CPM multiplication factor of 3), and PCI_MODCK = 0 (see note 2 below). The resulting configuration equals the part's maximum possible frequencies of 266 MHz CPU, 200 MHz CPM, 66 MHz 60x bus, and a PCI frequency of 66 MHz.
2. 50 MHz input clock, MODCK_H–MODCK_L[0111–011], and PCI_MODCK = 0 (see note 2below) to achieve a configuration of 200 MHz CPU, 150 MHz CPM, 50 MHz 60x bus, and a PCI frequency of 50 MHz.
3. 40 MHz input clock, MODCK_H–MODCK_L[0010–000], and PCI_MODCK = 0 (see note 2 below) to achieve a configuration of 200 MHz CPU, 160 MHz CPM, 40 MHz 60x bus, and a PCI frequency of 40 MHz.

Note that with each of the examples, any one of several values for MODCK_H–MODCK_L could possibly be used as long as the resulting configuration does not exceed the part's rating.

2. The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic "1"), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.).
3. In this mode, PCI_MODCK must be "0"

.

Table 5-16. Clock Default Configurations in PCI Agent Mode (MODCK_HI = 0000)(1)

MODCK[1–3](2)	Input Clock Frequency (PCI)(3)	CPM Multiplication Factor(3)	CPM Frequency	Core Multiplication Factor	Core(4) Frequency	Bus Division Factor	60x Bus(5) Frequency
000	66/33 MHz	2/4	133 MHz	2.5	166 MHz	2	66 MHz
001	66/33 MHz	2/4	133 MHz	3	200 MHz	2	66 MHz
010	66/33 MHz	3/6	200 MHz	3	200 MHz	3	66 MHz
011	66/33 MHz	3/6	200 MHz	4	266 MHz	3	66 MHz
100	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
101	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
110	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
111	66/33 MHz	4/8	266 MHz	3	300 MHz	2.5	100 MHz

Notes:
1. The user should verify that all buses and functions run frequencies that are within the supported ranges.
2. Assumes MODCK_HI = 0000
3. The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2.
4. Core frequency = (60x bus frequency)(core multiplication factor).
5. Bus frequency = CPM frequency/bus division factor.

Table 5-17 describes all possible clock configurations when using the PC8265A or the PC8266A's internal PCI bridge in agent mode

Table 5-17. Clock Configuration Modes in PCI Agent Mode[1]

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)[2][3]	CPM Multiplication Factor[2]	CPM Frequency	Core Multiplication Factor	Core[4] Frequency	Bus Division Factor	60x Bus[5] Frequency
0001_001	66/33 MHz	2/4	133 MHz	5	166 MHz	4	33 MHz
0001_010	66/33 MHz	2/4	133 MHz	6	200 MHz	4	33 MHz
0001_011	66/33 MHz	2/4	133 MHz	7	233 MHz	4	33 MHz
0001_100	66/33 MHz	2/4	133 MHz	8	266 MHz	4	33 MHz
0010_001	50/25 MHz	3/6	150 MHz	3	180 MHz	2.5	60 MHz
0010_010	50/25 MHz	3/6	150 MHz	3.5	210 MHz	2.5	60 MHz
0010_011	50/25 MHz	3/6	150 MHz	4	240 MHz	2.5	60 MHz
0010_100	50/25 MHz	3/6	150 MHz	4.5	270 MHz	2.5	60 MHz
0011_000	66/33 MHz	2/4	133 MHz	2.5	110MHz	3	44 MHz
0011_001	66/33 MHz	2/4	133 MHz	3	132 MHz	3	44 MHz
0011_010	66/33 MHz	2/4	133 MHz	3.5	154 MHz	3	44 MHz
0011_011	66/33 MHz	2/4	133 MHz	4	176 MHz	3	44 MHz
0011_100	66/33 MHz	2/4	133 MHz	4.5	198 MHz	3	44 MHz
0100_000	66/33 MHz	3/6	200 MHz	2.5	166 MHz	3	66 MHz
0100_001	66/33 MHz	3/6	200 MHz	3	200 MHz	3	66 MHz
0100_010	66/33 MHz	3/6	200 MHz	3.5	233 MHz	3	66 MHz
0100_011	66/33 MHz	3/6	200 MHz	4	266 MHz	3	66 MHz
0100_100	66/33 MHz	3/6	200 MHz	4.5	300 MHz	3	66 MHz
0101_000[6]	33 MHz	5	166 MHz	2.5	166 MHz	2.5	66 MHz
0101_001[6]	33 MHz	5	166 MHz	3	200 MHz	2.5	66 MHz
0101_010[6]	33 MHz	5	166 MHz	3.5	233 MHz	2.5	66 MHz
0101_011[6]	33 MHz	5	166 MHz	4	266 MHz	2.5	66 MHz
0101_100[6]	33 MHz	5	166 MHz	4.5	300 MHz	2.5	66 MHz
0110_000	50/25 MHz	4/8	200 MHz	2.5	166 MHz	3	66 MHz
0110_001	50/25 MHz	4/8	200 MHz	3	200 MHz	3	66 MHz
0110_010	50/25 MHz	4/8	200 MHz	3.5	233 MHz	3	66 MHz
0110_011	50/25 MHz	4/8	200 MHz	4	266 MHz	3	66 MHz
0110_100	50/25 MHz	4/8	200 MHz	4.5	300 MHz	3	66 MHz

Table 5-17. Clock Configuration Modes in PCI Agent Mode[1] (Continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)[2][3]	CPM Multiplication Factor[2]	CPM Frequency	Core Multiplication Factor	Core[4] Frequency	Bus Division Factor	60x Bus[5] Frequency
0111_000	66/33 MHz	3/6	200 MHz	2	200 MHz	2	100 MHz
0111_001	66/33 MHz	3/6	200 MHz	2.5	250 MHz	2	100 MHz
0111_010	66/33 MHz	3/6	200 MHz	3	300 MHz	2	100 MHz
0111_011	66/33 MHz	3/6	200 MHz	3.5	350 MHz	2	100 MHz
1000_000	66/33 MHz	3/6	200 MHz	2	160 MHz	2.5	80 MHz
1000_001	66/33 MHz	3/6	200 MHz	2.5	200 MHz	2.5	80 MHz
1000_010	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
1000_011	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
1000_100	66/33 MHz	3/6	200 MHz	4	320 MHz	2.5	80 MHz
1000_101	66/33 MHz	3/6	200 MHz	4.5	360 MHz	2.5	80 MHz
1001_000	66/33 MHz	4/8	266 MHz	2.5	166 MHz	4	66 MHz
1001_001	66/33 MHz	4/8	266 MHz	3	200 MHz	4	66 MHz
1001_010	66/33 MHz	4/8	266 MHz	3.5	233 MHz	4	66 MHz
1001_011	66/33 MHz	4/8	266 MHz	4	266 MHz	4	66 MHz
1001_100	66/33 MHz	4/8	266 MHz	4.5	300 MHz	4	66 MHz
1010_000	66/33 MHz	4/8	266 MHz	2.5	222 MHz	3	88 MHz
1010_001	66/33 MHz	4/8	266 MHz	3	266 MHz	3	88 MHz
1010_010	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
1010_011	66/33 MHz	4/8	266 MHz	4	350 MHz	3	88 MHz
1010_100	66/33 MHz	4/8	266 MHz	4.5	400 MHz	3	88 MHz
1011_000	66/33 MHz	4/8	266 MHz	2	212MHz	2.5	106 MHz
1011_001	66/33 MHz	4/8	266 MHz	2.5	265 MHz	2.5	106 MHz
1011_010	66/33 MHz	4/8	266 MHz	3	318 MHz	2.5	106 MHz
1011_011	66/33 MHz	4/8	266 MHz	3.5	371 MHz	2.5	106 MHz
1011_100	66/33 MHz	4/8	266 MHz	4	424 MHz	2.5	106 MHz

Notes:
1. The user should verify that all buses and functions run frequencies that are within the supported ranges.
2. The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2.
3. Input clock frequency is given only for the purpose of reference. MODCK_H–MODCK_L should be set so that the resulting configuration does not exceed the frequency rating of the user's part.

Example. If a part is rated at 266 MHz CPU, 200 MHz CPM, and 66 MHz bus, any of the following are possible (note that the three input clock frequencies are only three of many possible input clock frequencies):

1. 50 MHz input clock, MODCK_H–MODCK_L[0110–011] (with a core multiplication factor of 4, a CPM multiplication factor of 4, and a bus division factor of 3), and PCI_MODCK = 0 (see note 2 above). The PCI frequency is 50 MHz and the resulting configuration equals the part's maximum possible frequencies of 266 MHz CPU, 200 MHz CPM, and 66 MHz 60x bus.
2. 66 MHz input clock, MODCK_H–MODCK_L[0100–001], and PCI_MODCK = 1 (see note 2 above) to achieve a PCI frequency of 33 MHz and a configuration of 200MHz CPU, 200 MHz CPM, and 66 MHz 60x bus.
3. 40 MHz input clock, MODCK_H–MODCK_L[1001–011], and PCI_MODCK = 0 (see note 2 above) to achieve a PCI frequency of 40 MHz and a configuration of 160 MHz CPU, 160 MHz CPM, and 40 MHz 60x bus.

Note that with each of the examples, any one of several values for MODCK_H–MODCK_L could possibly be used as long as the resulting configuration does not exceed the part's rating.

4. Core frequency = (60x bus frequency) (core multiplication factor)
5. Bus frequency = CPM frequency/bus division factor
6. In this mode, PCI_MODCK must be "1".

6. Package Description

The following sections provide the package parameters and mechanical dimensions for the PC8265A.

6.1 Package Parameters

The package parameters are as provided in Table 6-1. The package type is a 37.5 × 37.5 mm, 480-lead TBGA.

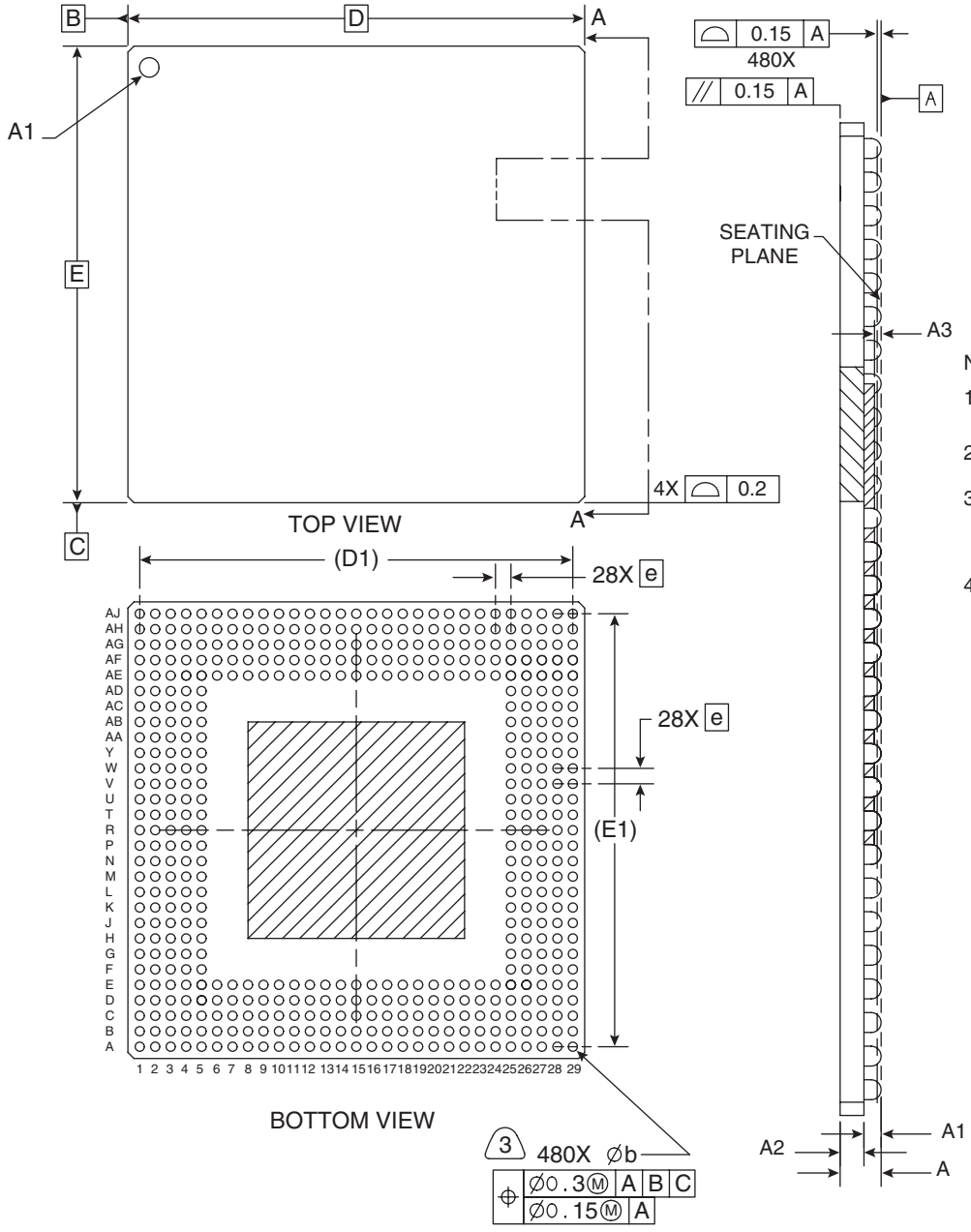
Table 6-1. Package Parameters

Parameter	Value
Package Outline	37.5 × 37.5 mm
Interconnects	480 (29 × 29 ball array)
Pitch	1.27 mm
Nominal unmounted package height	1.55 mm

6.1.1 Mechanical Dimensions

Figure 6-1 provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA package.

Figure 6-1. Mechanical Dimensions and Bottom Surface Nomenclature



Notes:

1. Dimensions and Tolerancing per ASME Y14.5M-1994
2. Dimensions in millimeters
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary data A
4. Primary data A and the seating plane are defined by the spherical crowns of the solder balls

Dim	Millimeters	
	Min	Max
A	1.45	1.65
A1	0.60	0.70
A2	0.85	0.95
A3	0.25	_
b	0.65	0.85
D	37.50 BSC	
D1	35.56 REF	
e	1.27 BSC	
E	37.50 BSC	
E1	35.56 REF	

7. Ordering Information

xx 8265 y xxx U nnn x

Product Code[1]	Part Identifier	Temperature Range[1]	Package[1]	Screening Level	CPU/CPM/Bus Speed[1] (MHz)	Revision Level[1]
PC(X)[2]	8265	M: T_{amb} = -55˚C, T_j = +125˚C	TP = 480 TBGA	Upscreening	M = 266 MHz H = 166 MHz B = 66 MHz	C

Notes: 1. For availability of the different versions, contact your local e2v sales office.

2. The letter X in the part number designates a "Prototype" product that has not been qualified by e2v. Reliability of a PCX part-number is not guaranteed and such part-number shall not be used in Flight Hardware. Product changes may still occur while shipping prototypes.

8. Definitions

8.1 Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. e2v customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify e2v for any damages resulting from such improper use or sale.

9. Document Revision History

Table 9-1 provides a revision history for this hardware specification.

Table 9-1. Revision History

Revision Number	Date	Substantive Change(s)
0873F	06/2007	Name change from Atmel to e2v
5336E	04/2006	- Addition of VCCSYN to “Note: Core, PLL, and I/O Supply Voltages” following Table 2. - Addition of note 1 to Table 5-1 on page 22. - Table 5-2 on page 26: Changes to Θ_{JA} and Θ_{JB} and Θ_{JC}. - Addition of notes or modifications to Figure 5-4 on page 30, Figure 5-5 on page 31, and Figure 5-6 on page 31. - Table 5-7 on page 32: Change of sp10. - Addition of Table 5-13 on page 40. - Addition of note 2 to Table 4-1 on page 8. - Table 4-1 on page 8: Addition of FCC2 Rx and Tx [3,4] to CPM pins PD7, PD18, PD19, and PD29. Also, the addition of SPICLK to PC19. Addition of Table 5-10 on page 35.
5336D	01/2006	T_c replaced by T_{amb} at -55°C
5336C	11/2004	Preliminary α-site replaced by Preliminary β-site Motorola changed to Freescale
5336B	06/2004	Ordering information: T_j replaced by T_c
5336A	08/2003	Initial revision

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