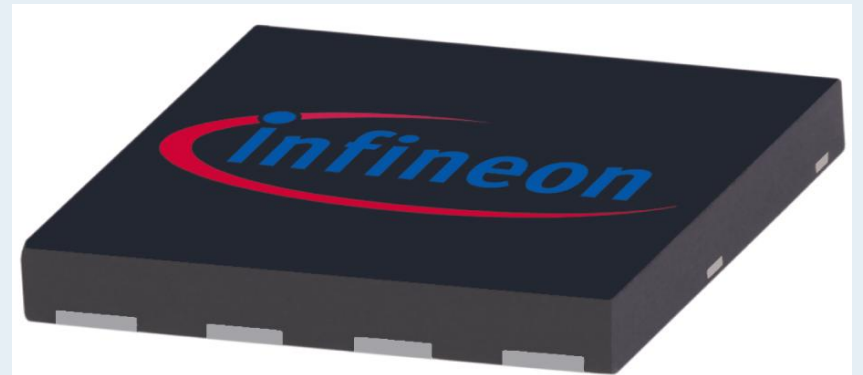


# Q&A ThinPAK 8x8

## New leadless SMD package for CoolMOS

April 2010

V 1.0



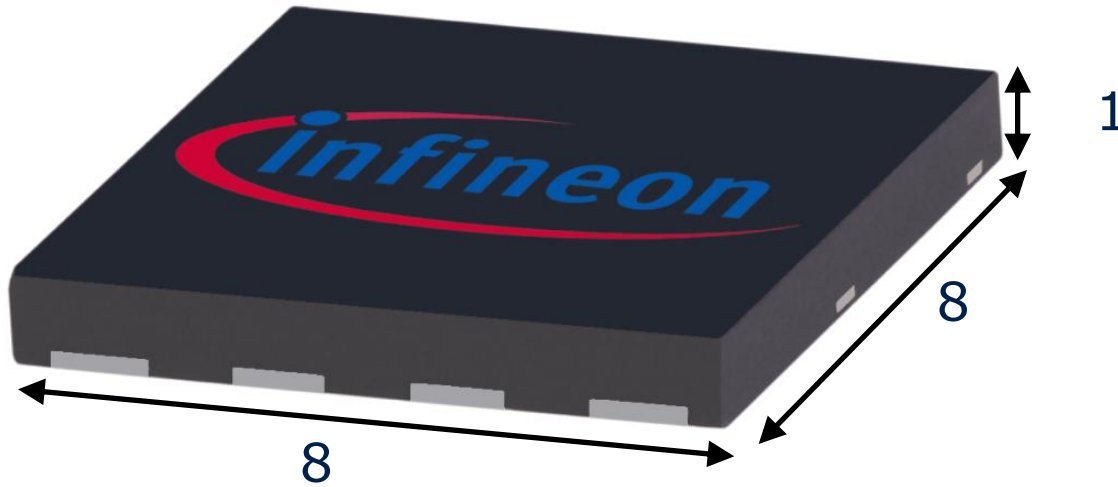
# Contents

- Package outline
- Manufacturing
- Package quality
- Materials and packing
- Electrical and thermal characteristics
- General

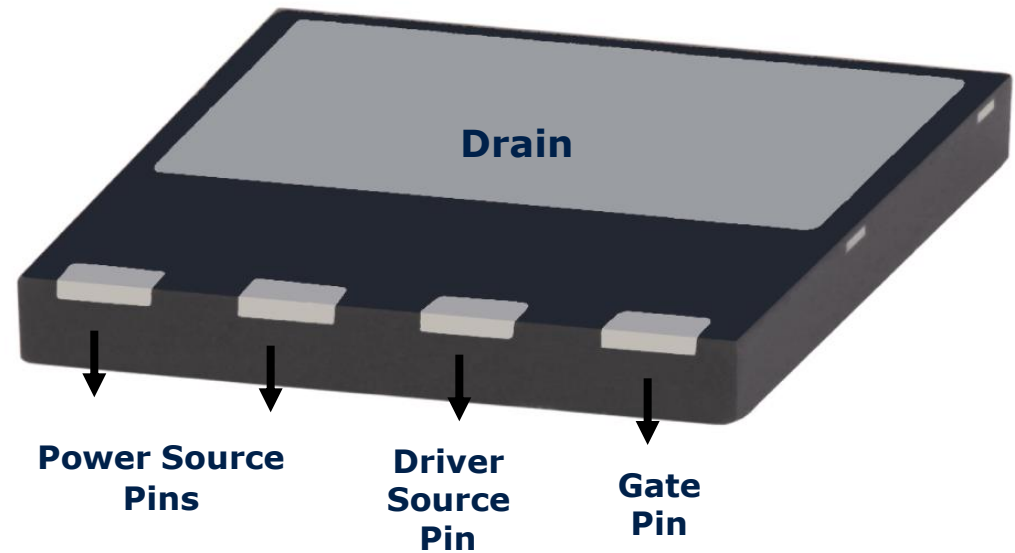
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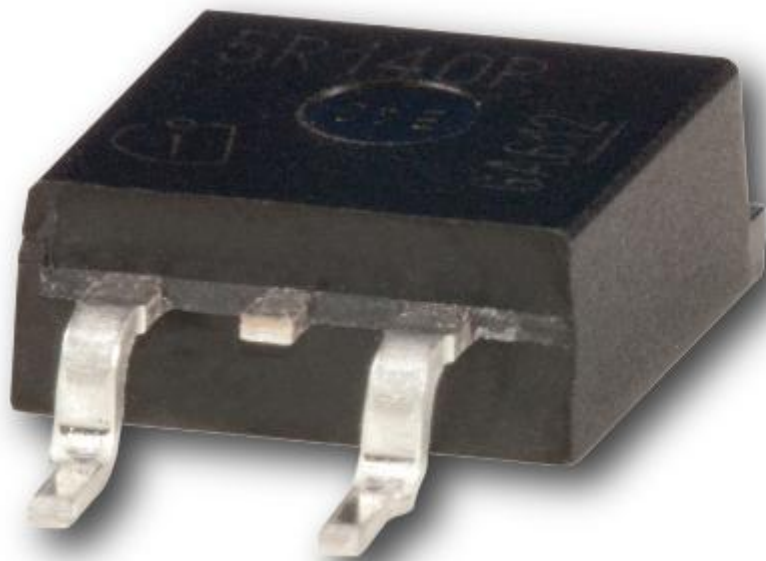
# 3D view and pinning



leadless SMD package with an exposed drain pad for optimum heat transfer to the PCB



# ThinPAK vs. D2PAK



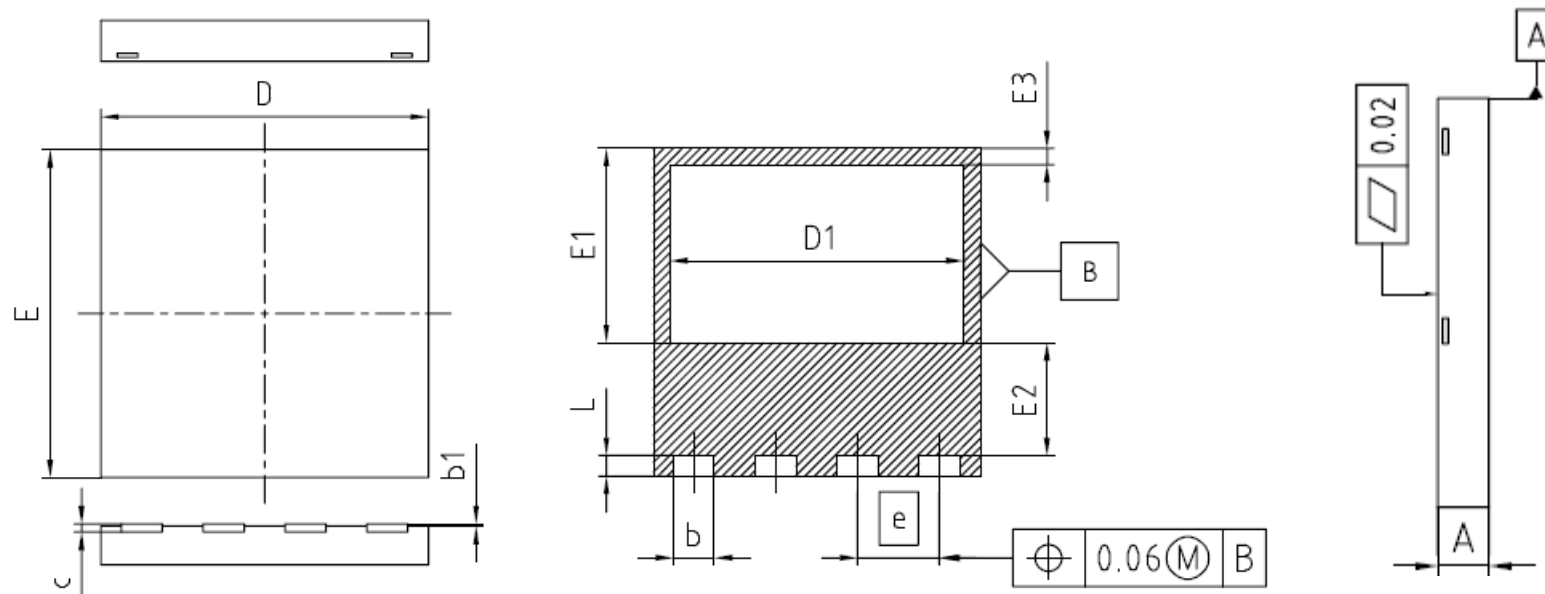
10 x 15 x 4.4 mm<sup>3</sup>



8 x 8 x 1 mm<sup>3</sup>

60 % footprint reduction - 80% height reduction

# ThinPAK 8x8 – Package outline, Lead finishing



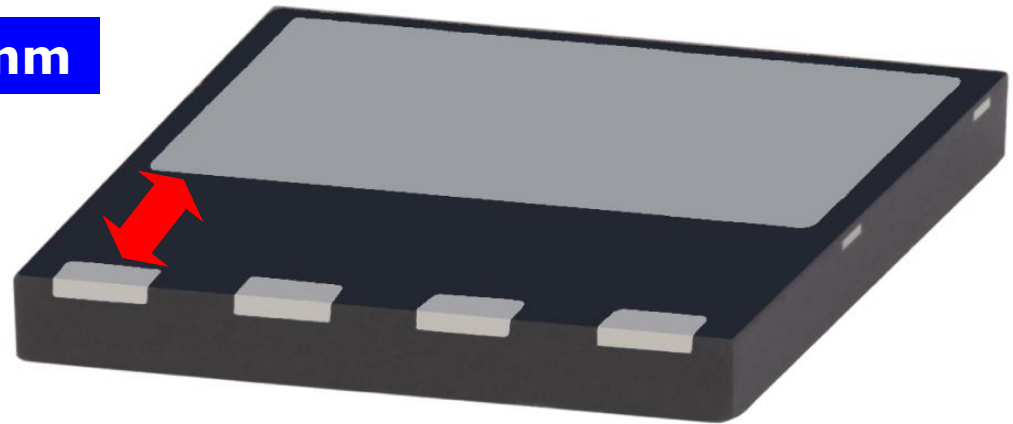
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.90	1.10	0.035	0.043
b1	0.00	0.05	0.000	0.002
c	0.10	0.30	0.004	0.012
D	7.90	8.10	0.311	0.319
D1	7.10	7.30	0.280	0.287
E	7.90	8.10	0.311	0.319
E1	4.65	4.85	0.183	0.191
E2	2.65	2.85	0.104	0.112
E3	0.30	0.50	0.012	0.020
e	2.00 (BSC)		0.079 (BSC)	
L	0.40	0.60	0.016	0.024
N	4		4	

Lead finishing: pure tin plating

# Creepage distance

- The creepage distance corresponds to the IPC9592 standard for linear functional spacing requirements for an operational voltage of 400 V

**Creepage distance: 2.75 mm**



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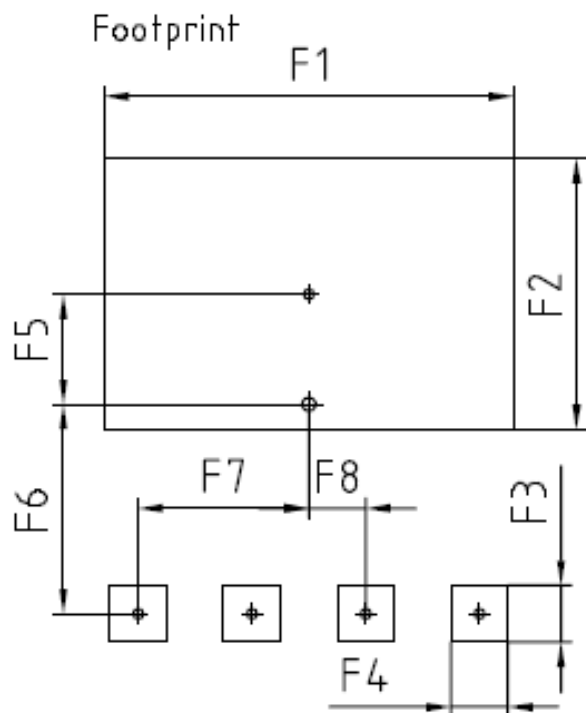


# Wave and reflow soldering

- Is the package suited for wave soldering ?
  - Yes
- What is the recommended reflow soldering temperature profile ?
  - Typically, the reflow profile depends on different factors like solder paste, component mix, etc. One of these factors is the package, which is qualified according J-STD-020D with a maximum soldering temperature of 260°C. Details can be found in the application note "Recommendations for board assembly of ThinPAK 8x8"

# Board pad design

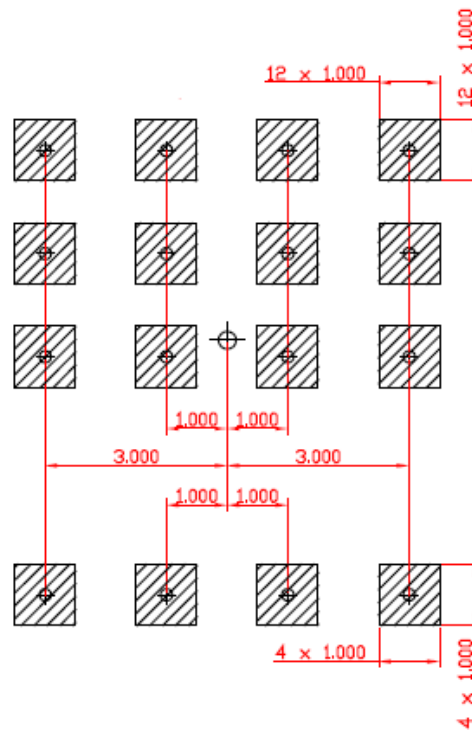
- What is the recommended board pad design ?



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	7.20		0.283	
F2	4.75		0.187	
F3	1.00		0.039	
F4	1.00		0.039	
F5	1.43		0.056	
F6	4.20		0.165	
F7	3.00		0.118	
F8	1.00		0.039	

# Stencil design

- What is the recommended stencil design (apertures, stencil thickness) ?
- Typical stencil thickness 100 -150  $\mu\text{m}$



Stencil apertures

# Solder paste

- What is the recommended solder paste (e.g. no clean solder paste) ?
  - Lead containing (typically Sn63Pb37 or Sn62Pb36Ag2) as well as lead free solder paste (typically Sn96.5Ag3Cu0.5) can be used. A "no-clean" solder paste is preferred since cleaning below the package is difficult. The paste must be suitable for printing the solder stencil aperture dimensions; type 3 paste is typical.
- What are recommended Pick and Place process parameters ?
  - Minimum placement accuracy +/-150  $\mu\text{m}$ ; Maximum force 10 N., Recognition is comparable to other tin plated leadless packages

# Inspection, cleaning and rework

- How can the solder joint quality be inspected ?
  - The solder joint meniscus of the 4 source/gate leads can be inspected by optical microscope or AOI. If it is intended to inspect the drain pad solder joint this can be done by X-ray
- What are recommendations for cleaning the board ?
  - Since cleaning under the component is difficult we recommend to use "no-clean" solder paste. Details can be found in the application note "Recommendations for board assembly of ThinPAK 8x8"
- What is the reworking procedure for this package ?
  - It is recommended to use a rework station for rework to obtain best quality and reliability. Using a soldering iron is not recommended, using hot air gun may be possible but the rework process can't be controlled accurately (e.g. overheating).

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# Qualification

- For which applications is this package qualified ?
  - The package is qualified for Server applications. Qualification extension for industrial application is started
- Is the package automotive qualified ?
  - No, the package is not qualified for automotive applications
- What is the TCoB stability of this package ?
  - Internal TCoB -40/125°C on a 4 layer, 1.6 mm PCB show a reliability of minimum 2000 cy.
- What is the min/maximum operating temperature ?
  - Minimum operating temperature is -40°C, maximum operating temperature is 150°C

# Qualification

- What qualifications tests were performed ?
  - Pre-Conditioning prior to all tests (MSL3, 260°C)
  - Temperature cycling TC (-40/125°C), 500 cy.
  - Autoclave AC (121°C / 100% rh), 96 h.
  - High Humidity High Temp. Reverse Bias H3TRB (85°C / 85%rh V = 80V), 500 h.
  - High Temperature Reverse Bias HTRB (Ta =150°C,V = 540V), 500 h
  - High Temperature Gate stress HTGS (Ta =150°C, Vg = ±20V), 500 h
  - Intermittend Operational Life Test IOL (Delta T=100K ), 7500 cy.



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# Materials and packing

- Is the package RoHS compliant ?
  - Yes, the package is RoHS compliant
- Is the mold compound halogen free ?
  - Yes the package is halogen-free according to IEC61249-2-21
- What is the MSL level of the package ?
  - The package is qualified for MSL 3, 260°C
- What is the packing of the package ?
  - The package is packed in tape and reel (4" reel, pcs., 3.5 k/reel)

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# Advantages, Parasitic inductivity

- What is the advantage of using this package in the application ?
  - The package gives different advantages:
    - high power density,
    - short commutation loop,
    - very small drain source overshoots
    - best behaviour for fast switching technologies
- What is the parasitic inductivity of this package compared to other packages like D2PAK and TO220 ?
  - The parasitic inductivity of the ThinPAK is 2 nH, D2PAK 6 nH and for TO220 depending on the leadlength between 6 and 12 nH
- What is the advantage of using a low parasitic package ?
  - A low inductive package minimizes overshoots and is easy to use

# Power capability

- What power can the package handle ?
  - This depends on the product used and on the thermal system. In an optimized cooling system a thermal resistance of 10 K/W is feasible when using a heatsink and forced convection. This would mean a power of 5 to 7 W is feasible.
- What is the maximum current, pulse current ?
  - Max. current: this depends on the product. For the IPL60R199CP continuous current: 16 A pulse current 51 A ( $T_c = 25^\circ\text{C}$ )
- How does the efficiency compare to other package types ?
  - There is no significant difference in terms of efficiency compared to traditional SMD packages

# Waveform, thermal performance

- What does the waveform look like compared to packages like D2PAK and TO220 ?
  - The low parasitic inductivity results in a very smooth waveform with minimum ringing and overshoots.
- How is the thermal performance in comparison to a D2PAK ?
  - The thermal performance is similar to existing traditional SMD packages like the D2PAK
- What is an optimized thermal system (Heatsink, interface material, board design) ?
  - The ThinPAK features an exposed drainpad. Therefore the dominant heatpath is to the PCB. To increase the power capability the usage of a heatsink which is mounted on the bottom side of the PCB is recommended. To keep the thermal resistance through the PCB low the PCB shall be designed with many vias (e.g. 40 or even more)

# Layout, thermal resistances

- What is a optimized layout ?
  - Please see the application note: CoolMOSTM CP - How to make most beneficial use of the latest generation of super junction technology devices
- What is the optimized layout for paralleling ?
  - The use of a common source layer is recommended
- What is the thermal resistance  $R_{thjc}$ ,  $R_{thja}$  ?
  - For IPL60R199CP the  $R_{thjc}$  is max. 0.9 K/W
  - The  $R_{thja}$  for 600 mm<sup>2</sup>, 70 μm Cu, single layer board is max. 42 K/W
- Can this package be used for top-side cooling ?
  - Yes, but one has to consider that the thermal resistance to the top side is higher than to the bottom side which results in a dominant heatflow to the PCB

# Rthjc\_top, Spice Models, Gate resistor

- What is the Rthjc to the top side ?
  - For IPL60R199CP the Rthjc to the top side is ~ 30 K/W
- Are spice models available ?
  - Yes, they can be downloaded from the Infineon homepage
- What is the optimum gate resistor ?
  - Please see the application note: CoolMOSTM CP - How to make most beneficial use of the latest generation of super junction technology devices



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# Applications and products

- What are typical applications ?
  - Applications are high power density designs from server to adapter
- Which products are available ?

Part Number	Maximum Ratings		$R_{DS(ON)}$ (mOhm)		Qg (nC) typ.
	$V_{DSS}$ (V)	$I_D$ (A)	Typ.	Max.	
IPL60R199CP	600	16	180	199	32
IPL60R299CP	600	11	270	299	22
IPL60R385CP	600	9	350	385	17

# Product outlook and 2nd source

- Are there plans for other products
  - There are plans to increase the portfolio and to have the SiC diodes in this package
- Is there a 2nd source available ?
  - ST Microelectronics has the same package which has the same outline.
- What are the difference between ST and IFX package ?
  - Both packages are the same from an outline perspective. The same board pad design can be used
- Do ST and IFX manufacture in the same location ?
  - No, both companies produce at different locations

A background image showing a person in a white lab coat and a white face mask, holding a clipboard. The person is slightly out of focus, and the background is a bright, clean laboratory or office setting.

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**We innovate.**

**We partner.**

**We create value.**

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