ML7105-002

Bluetooth® Low Energy

■Overview

ML7105-002 is a Bluetooth® Low Energy (here in after LE) LSI integrating RF, Baseband, microproccessor core and each peripherals, which has Bluetooth® LE compliant 2.4GHz band radio communication capability. ML7105-002 (hereafter "ML7105") is suitable for applications such as Wrist Watch, Remote Controller or PC peripherals.

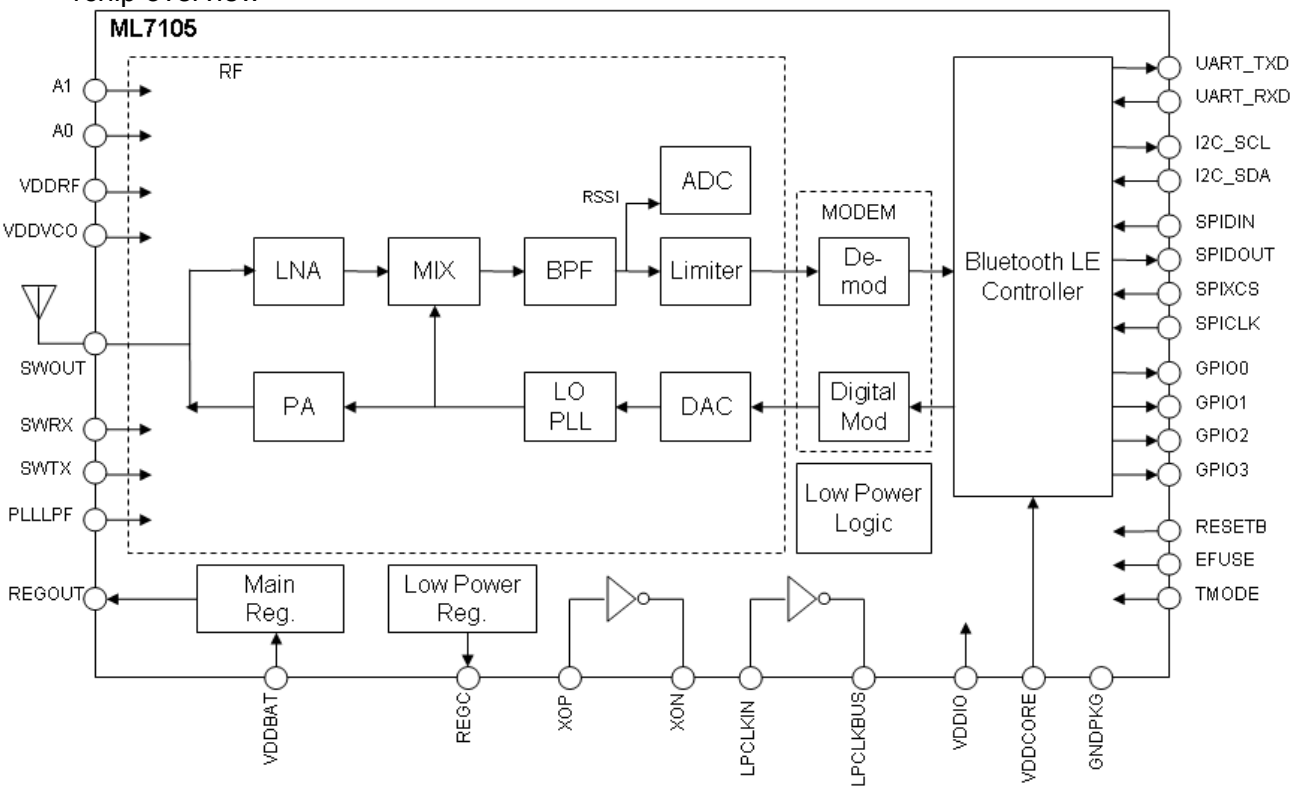
■Features

- Bluetooth® SIG Core Spec v4.0 compliant
- Ultra Low Power RF block
- Cortex-M0 Micro processor, it has interrupt controller and Sys-Tick Timer
- 64KB ROM (CODE_ROM) for Program, 16KB RAM (DATA_RAM) for Data
- 12KB RAM (CODE_RAM) for user Program
- Bluetooth® LE single mode compliant Baseband controller
- UART interface for Bluetooth® Host Controller Interface (HCI)
- SPI (Slave mode) interface for Custom Host Controller Interface
- I2C (Master & Slave) interface for EEPROM or Custom Host Controller Interface
- GPIO ports
- System Clock Timer and External Low Power Clock Timer
- Low Power operating mode
- Single power supply 1.6V to 3.6V
- Operating Temperature -20 deg.C to 70 deg.C
- Current Consumptions
  - Deep Sleep Mode below 0.7uA (with external Low Power Clock)
    below 2.9uA (with internal Low Power Clock oscillator circuit)
  - Idle Mode below 3.0mA
  - TX mode below 9.0mA
  - RX mode below 9.0mA
- Package
  - 32pins WQFN (P-WQFN32-0505-0.50-A63)

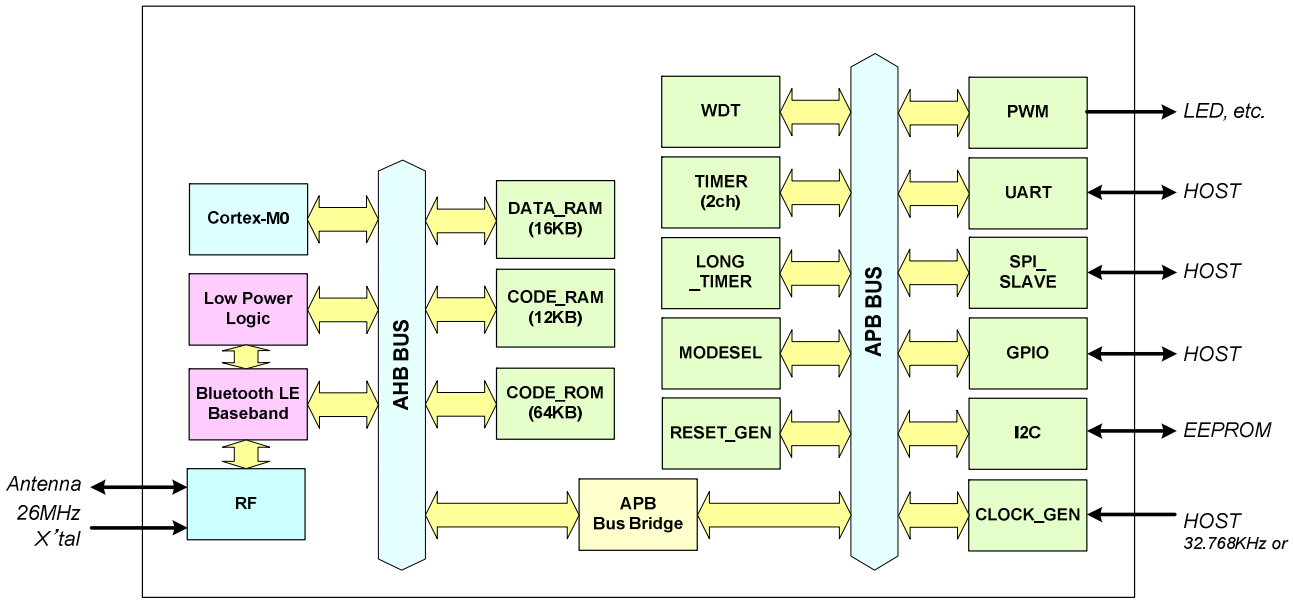
Pb Free, RoHS compliant

■Block Diagram

●1chip overview

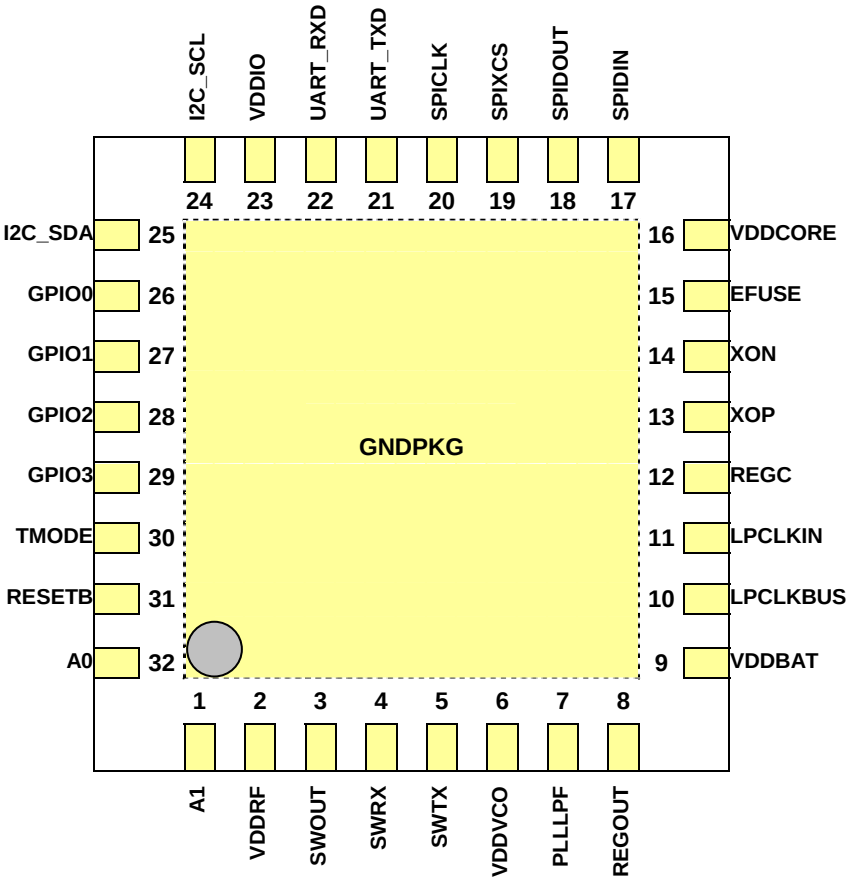


●Bluetooth® LE Controller



■Pin assignment

32pins WQFN



TOP VIEW

Note: Centre of the chip at bottom side is GND (symbol : Package GND)

■Pin definitions

No.	Pin Name	I/O	ANA/DIG	IO TYPE	Function
1	A1	IN	ANA	DIRIO	General purpose analog input
2	VDDRF	---	PWR	VCC	Power supply for RF block (1.2V)
3	SWOUT	INOUT	ANA	DIRIO_RF	RF signal RX/TX inout
4	SWRX	INOUT	ANA	DIRIO_RF	RX SW control signal
5	SWTX	INOUT	ANA	DIRIO_RF	TX SW control signal
6	VDDVCO	---	PWR	VCC	Power supply for RF-VCO (1.2V)
7	PLLLPF	OUT	ANA	DIRIO	PLL Loop Filter
8	REGOUT	OUT	ANA	DIRIO	Regulator output
9	VDDBAT	---	PWR	VCC	Power supply from Battery (=VDDIO) (1.6V to 3.6V)
10	LPCLKBUS	INOUT	ANA	DIRIO	Low power clock output/
11	LPCLKIN	INOUT	ANA	DIRIO	Low power clock/Xtal input
12	REGC	OUT	ANA	DIRIO	Decoupling capacitor pin for internal regulator
13	XOP	INOUT	ANA	DIRIO	Positive inout pin for XTAL oscillator block
14	XON	INOUT	ANA	DIRIO	Negative inout pin for XTAL oscillator block
15	EFUSE	---	DIG	DIRIO	Power supply for E-Fuse (fixed to GND in normal)
16	VDDCORE	---	PWR	VCC	Power supply for digital core (1.2V)
17	SPIDIN	IN	DIG	CMOS, IN	SPI Slave Data input
18	SPIDOUT	INOUT	DIG	CMOS, BiDIR	SPI Slave Data output
19	SPIXCS	IN	DIG	CMOS, IN	SPI Slave Chip Select
20	SPICLK	IN	DIG	CMOS, IN	SPI Slave Clock
21	UART_TXD	OUT	DIG	CMOS, OUT	UART TXD output
22	UART_RXD	IN	DIG	CMOS, IN	UART RXD input
23	VDDIO	---	PWR	VCC	Power supply for digital IO (1.6V to 3.6V)
24	I2C_SCL	INOUT	DIG	CMOS, BiDIR	I2C_SCL
25	I2C_SDA	INOUT	DIG	CMOS, BiDIR	I2C_SDA
26	GPIO0 /RF_ACTIVE	INOUT	DIG	CMOS, BiDIR	GPIO inout/RF_ACTIVE
27	GPIO1 /WAKEUP	INOUT	DIG	CMOS, BiDIR	GPIO inout/WAKEUP
28	GPIO2 /IRQ	INOUT	DIG	CMOS, BiDIR	GPIO inout/IRQ
29	GPIO3 /PS_CONTROL	INOUT	DIG	CMOS, BiDIR	GPIO inout/external control switch control
30	TMODE	IN	DIG	CMOS, IN	TESTMODE input
31	RESETB	IN	DIG	CMOS, IN	Reset input
32	A0	IN	ANA	DIRIO	General purpose analog input
G	GNDPKG	---	GND	GND	Package GND

■Pin definition

I/O definitions

I_{RF}	:	RF input and output
I	:	Digital input
I_{pd}	:	Digital input with pull-down resistor
I_A	:	Analog input
I_{AH}	:	Analog input support 3V
I_{SH}	:	Low-Power Clock input
X_{SH}	:	X'tal pin for Low-Power Clock
X_M	:	X'tal pin for Master Clock
O_2	:	Digital output with 2mA load capability
B_2	:	Digital inout with 2mA load capability
O_A	:	Analog output
O_{AH}	:	Analog output support 3V

●RF analog pins

No	Pin Name	Status in reset	I/O	Active Level	Function
3	SWOUT	Hi-Z	I_{RF}	---	RF signal RX/TX inout
4	SWRX	Hi-Z	I_{RF}	---	RX SW control signal
5	SWTX	Hi-Z	I_{RF}	---	TX SW control signal
32	A0	Hi-Z	I_{AH}	---	General purpose analog input
1	A1	Hi-Z	$I_{AH,}$	---	General purpose analog input
7	PLLLPF	Hi-Z	O_A	---	PLL Loop Filter

●XO, LPXO pins

No	Pin Name	Status in reset	I/O	Active Level	Function
13	XOP	Hi-Z	X_M	---	Positive inout pin for Master clock oscillator block
14	XON	Hi-Z	X_M	---	Negative inout pin for Master clock oscillator block
10	LPCLKBUS	0V	X_{SH}	---	Low power clock Xtal output
11	LPCLKIN	I_{SH}	X_{SH}, I_{SH}	---	Low power clock/Xtal input

●SPI pins

No	Pin Name	Status in reset	I/O	Active Level	Function
17	SPIDIN	Input	I	---	SPI SLAVE Data input
18	SPIDOUT	Output	B_2	---	SPI SLAVE Data output
19	SPIXCS	Input	I	Low	SPI SLAVE Chip Select
20	SPICLK	Input	I	---	SPI SLAVE Clock

●UART pins

No	Pin Name	Status in reset	I/O	Active Level	Function
21	UART_TXD	High output	O_2	---	UART TXD output
22	UART_RXD	input	I_{pd}	---	UART RXD input

●I2C pins

No	Pin Name	Status in reset	I/O	Active Level	Function
24	I2C_SCL	Input	B_2	---	I2C_SCL
25	I2C_SDA	Input	B_2	---	I2C_SDA

●GPIO pins

No	Pin Name	Status in reset	I/O	Active Level	Function
26	GPIO0 /RF_ACTIVE	Low output	B_2	---	GPIO inout/RF_ACTIVE (default : RF_ACTIVE)
27	GPIO1 /WAKEUP	Input	B_2	---	GPIO inout/WAKEUP (default : WAKEUP)
28	GPIO2 /IRQ	High output	B_2	---	GPIO inout/IRQ (default : IRQ)
29	GPIO3 /PS_CONTROL	Low output	B_2	---	GPIO inout/external switch control (default : PS_CONTROL)

●Miscellaneous pins

No	Pin Name	Status in reset	I/O	Active Level	Function
31	RESETB	input	I	Low	Reset input (Low = Reset)
15	EFUSE	---	---	---	Power supply for E-Fuse (fixed to GND in normal)
30	TMODE	input	I	---	TESTMODE input (Low = normal mode)

●Regulator pins

No	Pin Name	Status in reset	I/O	Active Level	Function
8	REGOUT	Hi-Z	O_{AH}	---	Regulator output
12	REGC	1.2V output	O_{AH}	---	Decoupling capacitor pin for internal regulator

●Power Supply pin

No	Pin Name	Status in reset	I/O	Active Level	Function
2	VDDRF	---	---	---	Power supply for RF block (1.2V)
6	VDDVCO	---	---	---	Power supply for RF-VCO (1.2V)
9	VDDBAT	---	---	---	Power supply from Battery (=VDDIO) (1.6V to 3.6V)
16	VDDCORE	---	---	---	Power supply for digital core (1.2V)
23	VDDIO	---	---	---	Power supply for digital IO (1.6V to 3.6V)
G	GNDPKG	---	---	---	Package GND

●Unused pins

Followings are recommendation for pins are not used.

No	Pin Name	Recommendation
1	A1	Open
10	LPCLKBUS	Open
15	EFUSE	Fix to GND
17	SPIDIN	Fix to VDDIO
18	SPIDOUT	Fix to VDDIO
19	SPIXCS	Fix to VDDIO
20	SPICLK	Fix to VDDIO
21	UART_TXD	Open
22	UART_RXD	Fix to GND (See operating mode section)
24	I2C_SCL	Fix to VDDIO
25	I2C_SDA	Fix to GND
26	GPIO0	Open
27	GPIO1	Fix to VDDIO or GND (See operating mode section)
28	GPIO2	Open
29	GPIO3	Open
32	A0	Open

Note

Leaving input pins open with Hi-Z status, current consumption will be increased. It is highly recommended that input or inout pins should not be left open.

■Electrical Characteristics

●Absolute Maximum Rating

Item	Symbol	Condition	Rating	Unit
Power supply 3.3V (*1)	V_{DDIO1} V_{DDIO2}	Ta = –20 to +70 deg.C GND= 0 V (*3) VDDRF=VDDVCO =VDDCORE, VDDBAT=VDDIO,	–0.3 to +4.6	V
Power supply 1.2V (*2)	V_{DDRF}		–0.3 to +1.8	V
Digital input voltage (*4)	V_{DIN}		–0.3 to V_{DDIO}+0.3	V
Digital output voltage (*5)	V_{DO}		–0.3 to V_{DDIO}+0.3	V
Analog IO voltage (*6)	V_A		–0.3 to V_{DDRF}+0.3	V
Analog HV IO voltage (*7)	V_{AH}		–0.3 to V_{DDIO}+0.3	V
Digital IO load current	I_{DO}		–10 to +10	mA
Analog IO current (*6)(*7)	I_A		–2 to +2	mA
Power Dissipation	P_D		1.0	W
Storage temperature	T_{stg}	–	–55 to +125	deg.C

(*1) VDDBAT, VDDIO pins
(*2) VDDRF, VDDVCO, VDDCORE,
(*3) GND: GND pin (Package GND)
(*4) IO pins with I, I_{PD}, B_2 symbol in pin definition
(*5) IO pins with O_2,B_2 symbol in pin definition
(*6) IO pins with I_A, O_A, X_M symbol in pin definition
(*7) IO pins with I_{AH}, O_{AH}, I_{SH}, X_{SH}, symbol in pin definition

●Recommended Operating Conditions

Item	Symbol	Condition	Min	Typ	Max	Unit
Power Supply	V_{DDIO1}	VDDIO pin (VDDBAT≧VDDIO)	1.6	3.3	3.6	V
Power Supply	V_{DDIO2}	VDDBAT pin (VDDBAT≧VDDIO)	1.6	3.3	3.6	V
Ambient Temperature	Ta	–	–20	+25	+85	°C
Rising time digital input pins	t_{IR1}	Digital input/inout pins	–	–	20	Ns
Falling time digital input pins	t_{IF1}	Digital input/inout pins	–	–	20	Ns
Load capacitance digital	C_{DL}	Digital output/inout pins	–	–	20	pF
Master Clock (26 MHz) crystal oscillator frequency	F_{MCK1}	Connect cristal oscillator between XOP－XON pins (*1), (*2)	–40 ppm	26	+40 ppm	MHz
Low Power Clock (32.768 kHz) crystal oscillator frequency	F_{LPCK1}	LPCLKIN pin, LPCLKBUS pin (*2)	–250 ppm	32.768	+250 ppm	kHz
Low Power Clock Input Duty Ratio	D_{LPCK1}	External input from LPCLKIN, LPCLKBUS pin left OPEN	30	50	70	%
RF Channel frequency (*2)	F_{RF}	SWOUT pin	2402	–	2480	MHz
RF input level	P_{RFIN}		-70	–	-10	dBm

(*1) Cristal oscillator is recommended
(*2) The cristal should be used the one that meet the specification include peripheral circuit.
(*3) Frequency range F = 2402 + 2 x k [MHz] here k=0, 1,2,…,39.

●Current consumption

(Ta = –20 to +70 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
Current Consumption (*1)	I_{DD1}	Deep Sleep state (External Low Power Clock)	–	0.7	–	uA
	I_{DD2}	Deep Sleep state (Internal Low Power Clock oscillation)	–	2.9	–	uA
	I_{DD3}	Idle state	–	3	–	mA
	I_{DD4}	RF RX state		9	–	mA
	I_{DD5}	RF TX state (-6dBm)	–	9	–	mA
		RF TX state (0dBm)	–	10.9	–	mA

(*1) Condition: Ta = 25deg. VDDHV = 3.3V

●DC characteristics

(Ta = –20 to +70 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
H level Voltage Input	V_{IH1}	(*1) (*2) (*5)	V_{DDIO} X0.7	–	V_{DDIO}	V
L level Voltage input	V_{IL1}	(*1) (*2) (*5)	0	–	V_{DDIO} X0.3	V
LPCLKIN pin H level Voltage Input	V_{IH2}	(*3)	1	–	V_{DDIO}	V
LPCLKIN pin L level Voltage input	V_{IL2}	(*3)	0	–	0.3	V
Input leak current	I_{IH1}	$V_{IH} = V_{DDIO}$ (*1) (*5)	–1	–	1	uA
	I_{IH2}	$V_{IH} = V_{DDIO}$ (*2)	5	–	250	uA
	I_{IL1}	V_{IL} = 0 V (*1) (*2) (*5)	–-1	–	1	uA
Tri-state output leak current	I_{OZH}	$V_{OH} = V_{DDIO}$ (*4) (*5)	–1	–	1	uA
	I_{OZL}	V_{OL} = 0 V (*4) (*5)	–1	–	1	uA
H level Voltage Output	V_{OH}	I_{OH} = –2mA (*4) (*5) $V_{DDIO} = V_{DDRF}$ = 1.6V to 3.6V	V_{DDIO} × 0.75	–	V_{DDIO}	V
L level Voltage Output	V_{OL}	I_{OL} = 2mA (*4) (*5)	0	–	V_{DDIO} × 0.25	V
Input pin capacitance	C_{IN}	F=1MHz (*1) (*2) (*4) (*5)	–	8	–	pF

(*1) IO pins with I symbol in pin definition
(*2) IO pins with I_{PD} symbol in pin definition
(*3) IO pins with I_{SH} symbol in pin definition
(*4) IO pins with O_2 symbol in pin definition
(*5) IO pins with B_2 symbol in pin definition

●RF Characteristics

(Ta = –20 to +70 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
TX						
TX power	P_{OUT1}	0dBm setting	–3	0	3	dBm
	P_{OUT2}	-18dBm setting	–	–18	–	dBm
Centre Frequency tolerance	F_{CERR}	Master Clock tolerance < 40 ppm	–40	–	40	ppm
Modulation data rate	D_{RATE}	–	–	1	–	Mbps
Modulation index	F_{IDX}	–	0.45	0.50	0.55	–
Bandwidth-bit rate products BT	BT	GFSK	–	0.5	–	–
Modulation characteristics	F_{1avg}	Frequency deviation of 10101010 pattern	225	250	275	kHz
	F_{RATE}	Frequency deviation ratio between 10101010 and 00001111 sequence	80	–	–	%
	F_{DELTA}	Minimum Frequency Deviation	185	–	–	kHz
In-band spurious	P_{OS1}	2MHz apart from carrier frequency in a 1MHz bandwidth	–	–	-20	dBm
	P_{OS2}	3MHz apart from carrier frequency in a 1MHz bandwidth	–	–	-30	dBm
RX						
Receiver Sensitivity	P_{SENS}	PER = 30.8% (*1)	–	-85	-70	dBm
Interference performance PER<30.8% Wanted signal :-67dBm Interfering signal : modulated signal (*2)	CI_{CO}	Co-channel interference C/I	21	–	–	dB
	CI_{S1}	Adjacent (1MHz) interference C/I	15	–	–	dB
	CI_{S2}	Adjacent (2MHz) interference C/I	-17	–	–	dB
	CI_{S3}	Adjacent (>=3MHz) interference C/I	-27	–	–	dB
	CI_{IMG}	Image frequency interference (-4MHz) C/I	-9	–	–	dB
	CI_{IMGS1}	Adjacent (1MHz) interference to image frequency (-3MHz,-5MHz)) C/I	-15	–	–	dB
Out of band blocking PER<30.8% Wanted signal :-67dBm Interfering signal:CW (*2) (*3)	P_{BLK1}	30MHz to 2000MHz BW 10MHz	-30	–	–	dBm
	P_{BLK2}	2003 to 2399MHz BW 3MHz	-35	–	–	dBm
	P_{BLK3}	2484 to 2997MHz BW 3MHz	-35	–	–	dBm
	P_{BLK4}	3000MHz to 12.75GHz BW 25MHz	-30	–	–	dBm

Intermodulation PER<30.8% Wanted signal :-64dBm (*2)	P_{IM}	CW interering signal +/-3MHz Modulated interfering signal +/-6MHz or CW interfering signal +/-4MHz Modulated interfering signal +/-8MHz or CW interfering signal +/-5MHz Modulated interfering signal +/-10MHz	-50	–	–	dBm
Maximum input level(*2)	P_{RXMAX}	PER = 30.8% (*1)	–	–	-10	dBm
RSSI detection range (*2)	$P_{RSSIMAX}$	Upper	-40	–	–	dBm
	$P_{RSSIMIN}$	Lower	–	–	-80	dBm

(*1) PER=30.8% is corresponding to BER=0.1%
(*2) Condition: Ta = 25deg.、VDDHV = 3.3V
(*3) Follow RCV-LE/CA/04/C test spec of Bluetooth SIG

●SPI interface

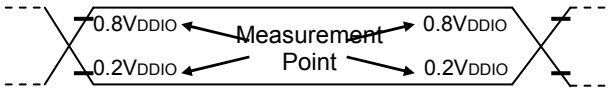
(Ta = –20 to +70 deg.C)

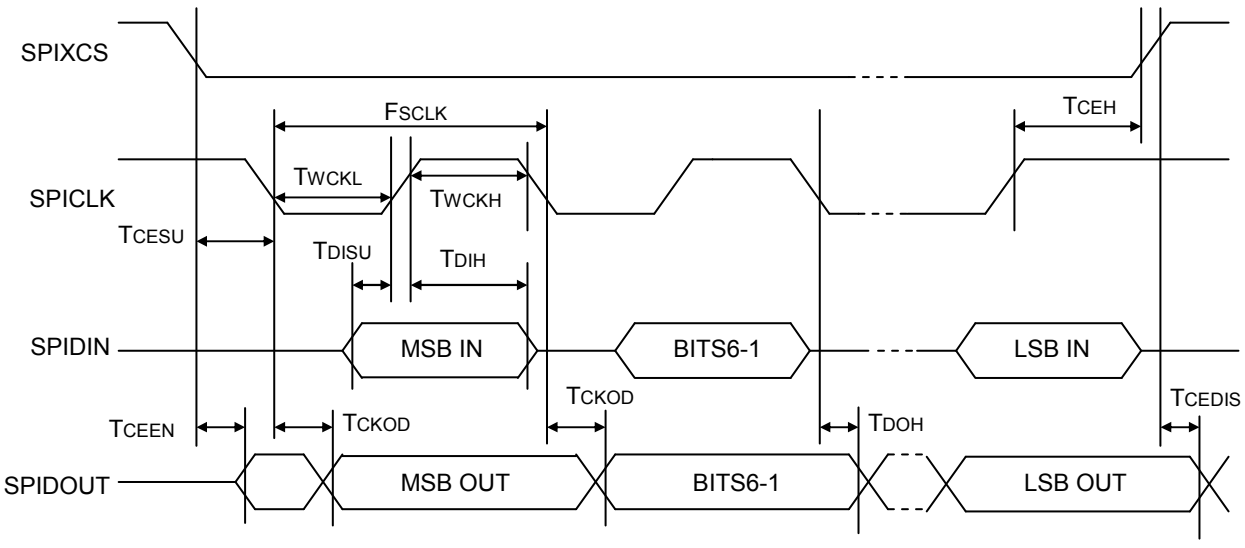
Item	Symbol	Condition	Min	Typ	Max	Unit
SPICLK Clock Frequency	FSCLK	Load capacitance CL=20pF	16.384	32.768	1625	kHz
SPIXCS input setup time	TCESU		1/Fsclk	–	–	ms
SPIXCS input hold time	TCEH		1/Fsclk	–	–	ms
SPICLK minimum high pulse width	TWCKH		250	–	–	ns
SPICLK minimum low pulse width	TWCKL		250	–	–	ns
SPIDIN input setup time	TDISU		5	–	–	ns
SPIDIN input hold time	TDIH		250	–	–	ns
SPICLK output delay time	TCKOD		–	–	250	ns
SPIDOUT output hold time	TDOH		5	–	–	ns
SPIXCS enable delay time	TCEEN		0	–	300	ns
SPIXCS disable delay time	TCEDIS		150	–	–	ns

Note: When using the width of the following SPICLK edge from the data output trigger SPICLK edge within 250 ns, there is possibility that the output timing of SPIDOUT becomes simultaneous with the following edge. Consider the data input setup time of HOST and set pulse width.

Remarks: All timing specification is defined at V_{DDIO} x 20% and V_{DDIO} x 80%
SPIXCS input setup/hold time have to be at least 1cycle of SPICLK clock frequency

Measurement point

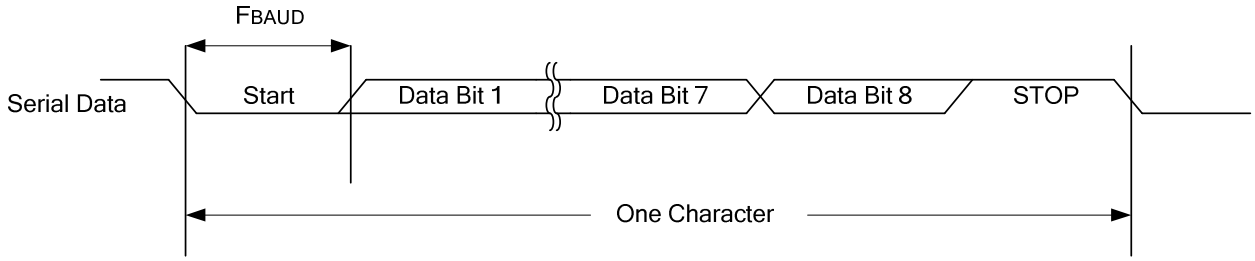




●UART interface

(Ta = –20 to +70 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
Baud Rate	FBAUD	Load capacitance CL=20pF	–	57600	–	bps(Hz)



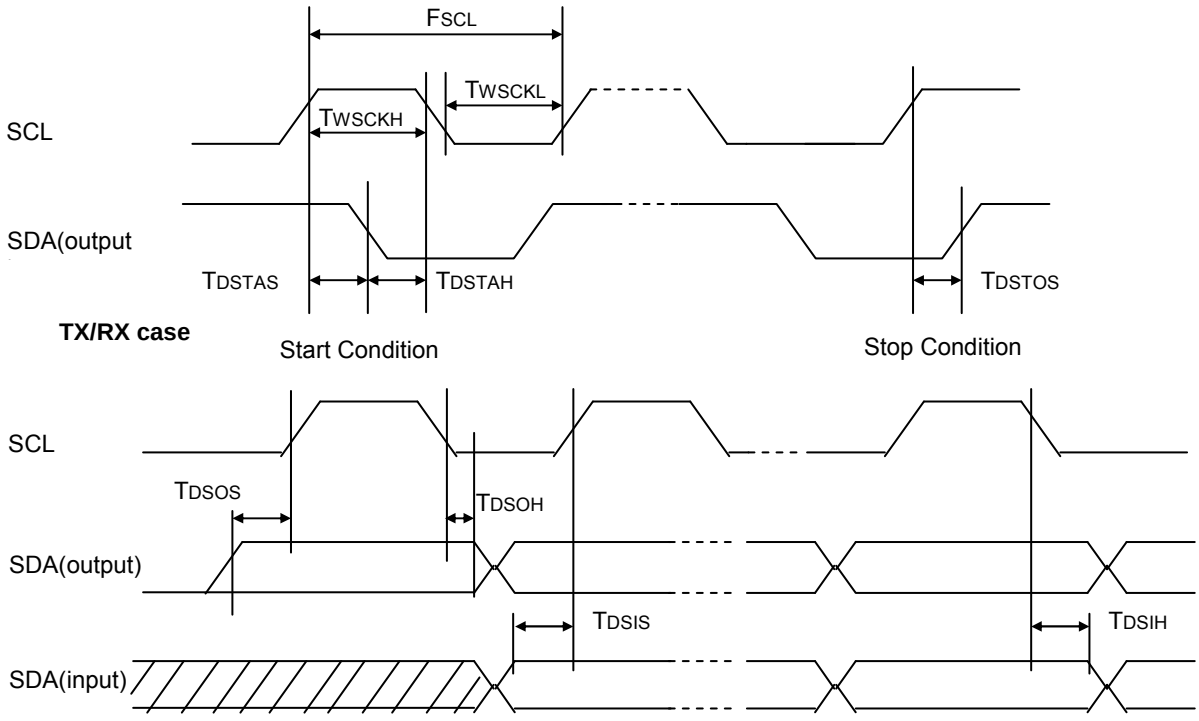
●I2C interface

(Ta = –20 to +70 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
SCL clock frequency	FSCL	Load capacitance CL=20pF	–	–	400	kHz
SCL minimum high pulse width	TWSCKH		10	–	–	us
SCL minimum low pulse width	TWSCKL		10	–	–	us
Start condition hold time	TDSTAH		5	–	–	us
Start condition setup time	TDSTAS		5	–	–	us
Stop condition setup time	TDSTOS		5	–	–	us
SDA output hold time	TDSOH		5	–	–	us
SCL output delay time	TDSOS		5	–	–	us
SDA input setup time	TDSIS		80	–	–	ns
SDA input hold time	TDSIH		0	–	–	ns

Note: SCL clock frequency is fixed to 400kHz

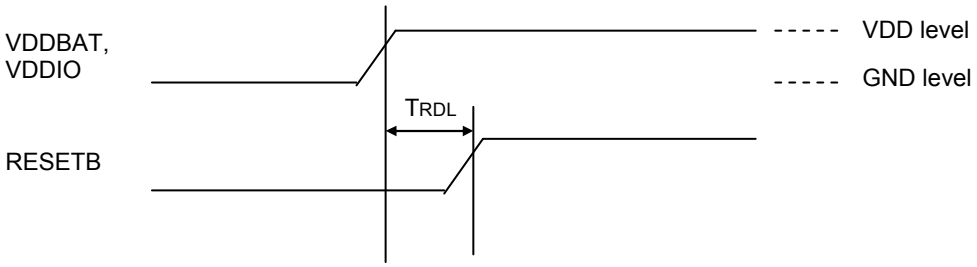
Start condition（SDA falling edge while SCL=1）, Stop condition（SDA rising edge while SCL=1）



●Reset operation

(Ta = –20 to +70 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
RESETB propagation delay time （Power on）	TRDL	Start supplying power (VDDBAT,VDDIO)	20	–	–	ms
RESETB Pulse width	TRPLS	RESETB pin	1	–	–	us



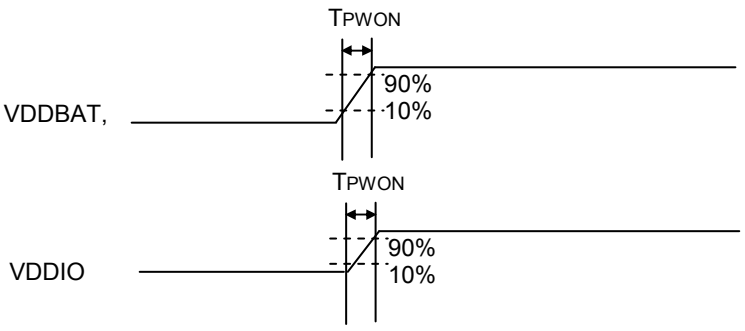
Power on reset function

Reset function from RESETB pin
It is possible to reset internal circuit by asserting RESETB after power supply is on.
It is possible to reset internal circuit by same way even if it is not power sequence. Internal circuit will move to normal state after oscillation circuit become stable by clock stabilizing circuit after reset function.

●Power on

(Ta = –20 to +70 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
VDD pin rising time	TPWON	While power on VDD pins (VDDBAT,VDDIO)	0.2	1	5	ms
Time difference between VDD pin while power on state	TPWONdly	While power on VDD pins (VDDBAT,VDDIO)	0	-	-	ms
Time difference between VDD pin while power off state	TPWOFdly	While power off VDD pins (VDDBAT,VDDIO)	0	-	-	ms



■Operating mode

Following 4 operating modes are available to use

BACI Mode:	Application mode using SPI-SLAVE interface
HCI Mode:	HCI mode (Bluetooth LE standard compliant) using UART interface.
RAM Mode:	Function extension mode downloading user program to internal memory
Debug Mode:	Debugging mode to have access to I2C-EEPROM write and read.

■Operating mode configuration

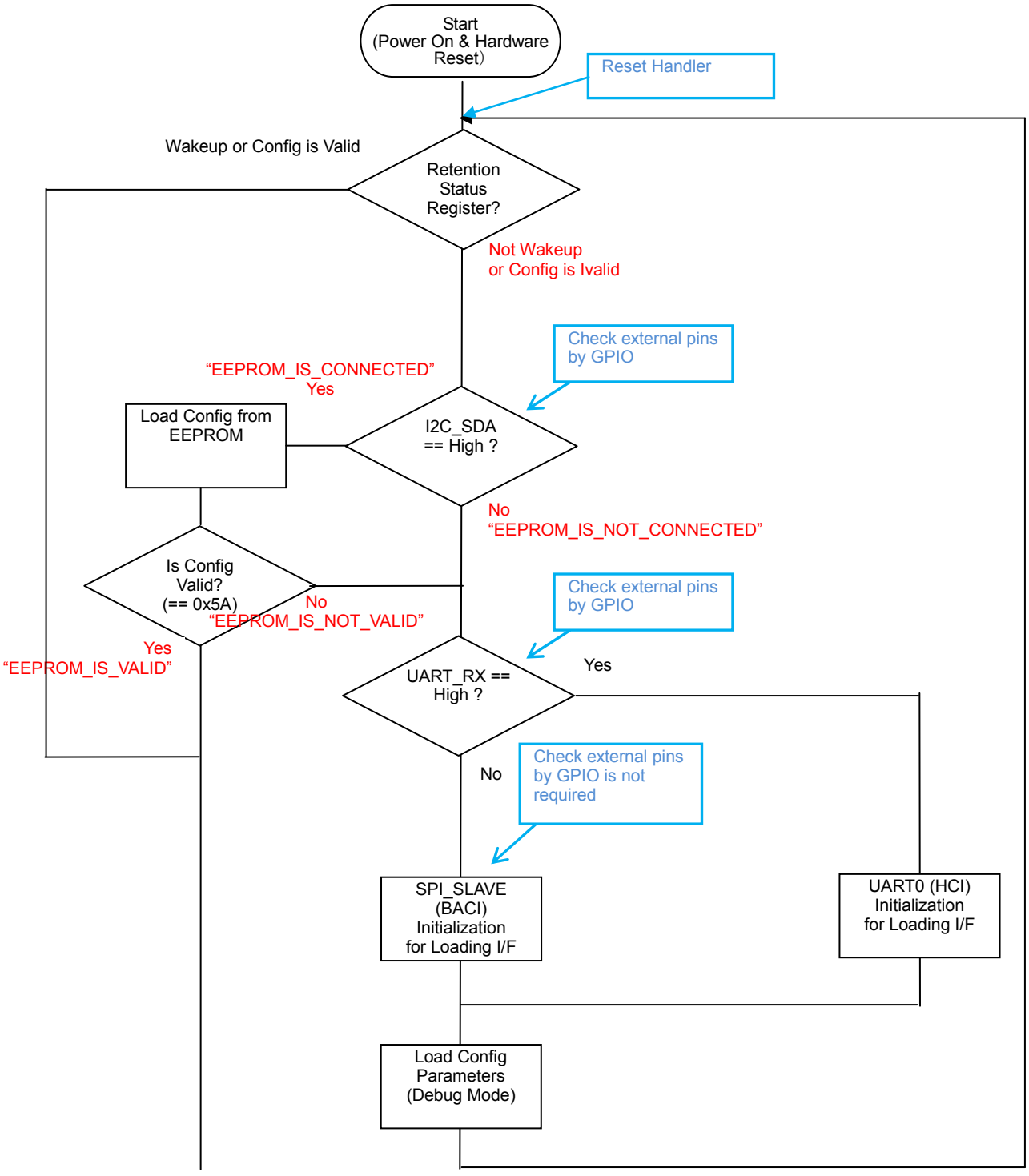
Configuration of operating mode will be done by pin status shown in table below. The symbol “X“ is don’t care, it has to be used as normal function. When configure operating mode, reset has to be issued.
RAM mode and Debug mode is distinguished by configuration parameter.

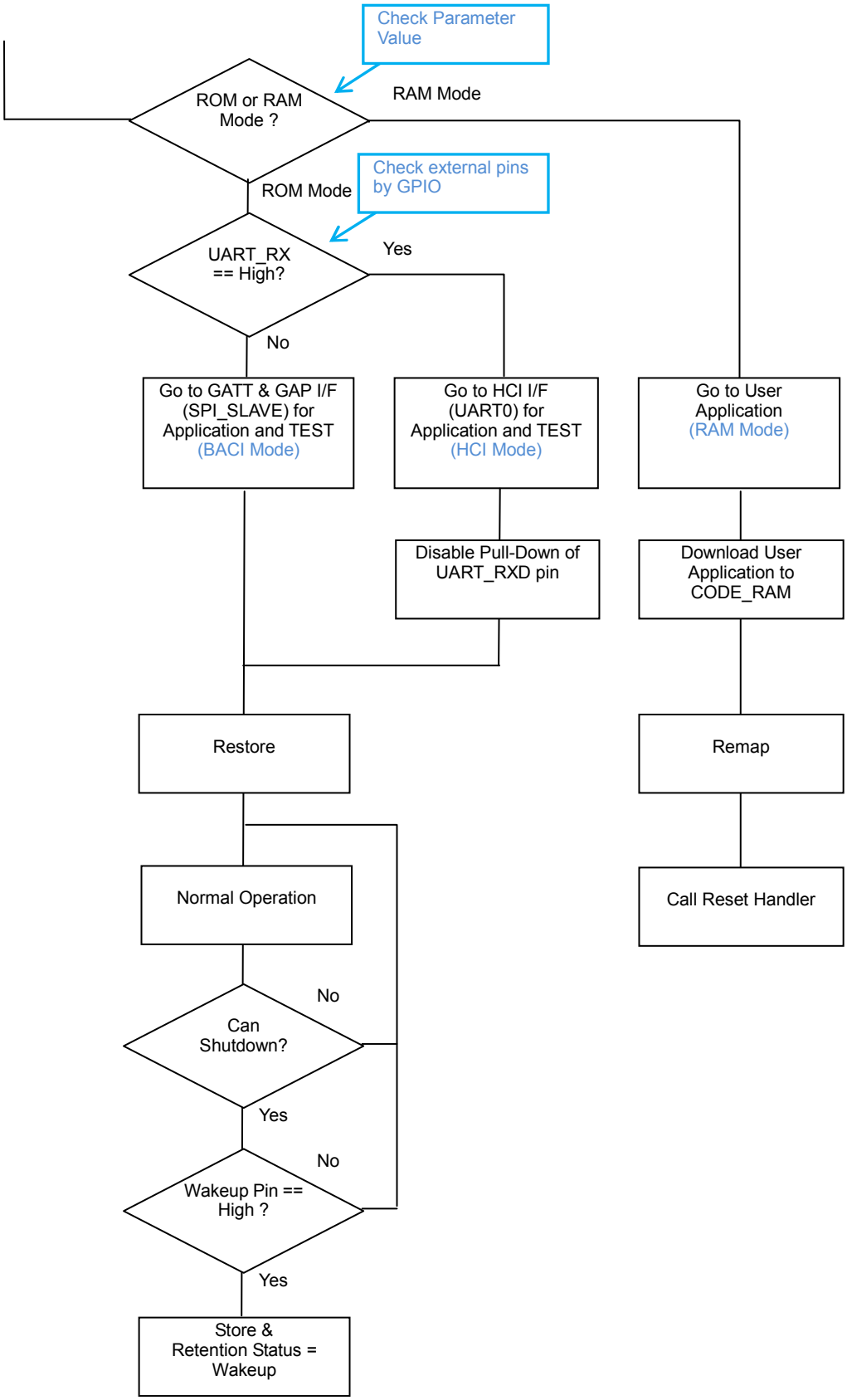
Operating mode	Pin confitions
	UART_RXD
BLI Mode	Low
HCI Mode ※1	High
RAM Mode	X
Debug Mode	X

(*) Fix Wakeup pin to Low on HCI mode.
See anootations on Section about Power State Transition

■Boot Sequence

Operating mode will be deciede by boot sequence shown below.




Check Parameter Value
ROM or RAM Mode ?
RAM Mode
ROM Mode
Check external pins by GPIO
UART_RX == High?
Yes
No
Go to GATT & GAP I/F (SPI_SLAVE) for Application and TEST (BACI Mode)
Go to HCI I/F (UART0) for Application and TEST (HCI Mode)
Go to User Application (RAM Mode)
Disable Pull-Down of UART_RXD pin
Download User Application to CODE_RAM
Restore
Remap
Normal Operation
Call Reset Handler
Can Shutdown?
No
Yes
Wakeup Pin == High ?
No
Yes
Store & Retention Status = Wakeup

■Power Management

●Power Mode

Following Power modes are available.
Active mode
Idle mode
Deep sleep mode
Application Sleep

[Active mode]
Active Mode will be used during RF connection state.

[Idle mode]
Idle mode is low power consumption mode. It can be used between connection events with short time interval which is equal to or less than 40msec.

[Deep sleep mode]
Deep sleep mode will be used between connection evenrs or system function is suspended. Oscillation block in RF block is suspeded, communication time interval will be counted by low power clock supplied from external pin.

[Application Sleep]
Application Sleep mode will suspend oscillation in RF block, and stand by with low power clock supplied from external pin. This is low power mode used in the case communications is unnecessary.
Sleep command issue by host cpu makes become this mode, and this mode is kept till wake up from external pin.

●Power State Transition

Power mode transition is described in Fig.1

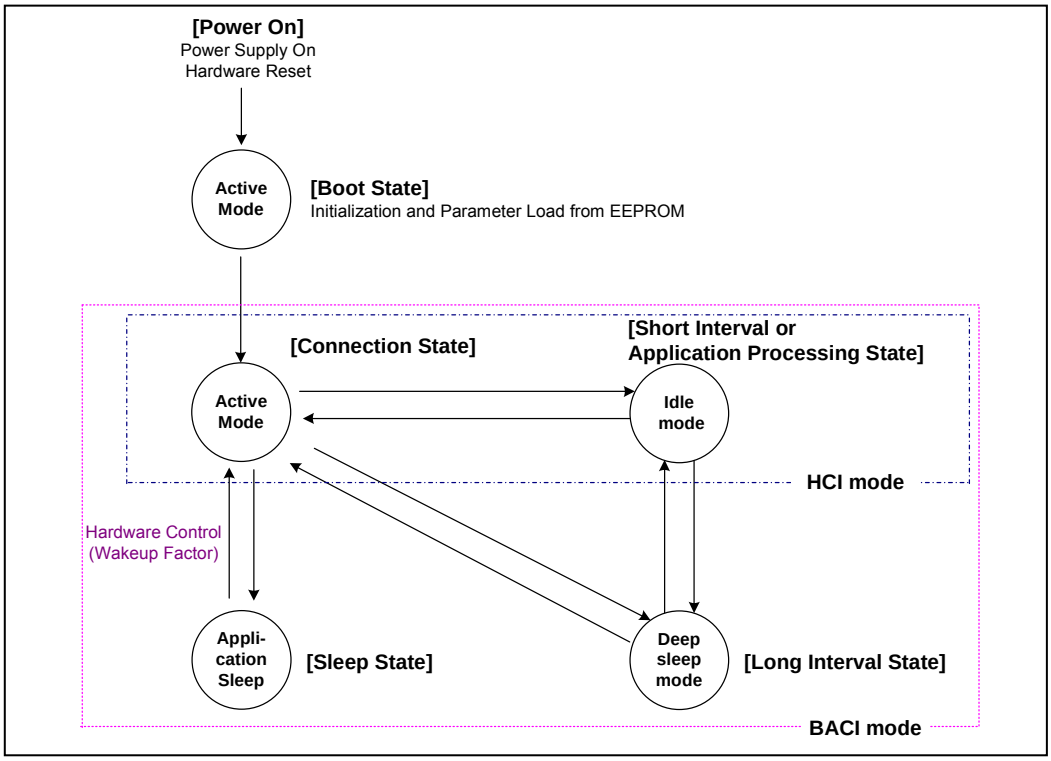


Fig. 1 Power state transition and operating mode

[Power On]
Assert hardware reset pin for a definite period when power supply is started.ML7105 will become oot state When hardware reset is released.

[Boot State]
Booting operation will be started when hardware reset is released. Booting program will execute to initileze peripheral blocks and download of parameters.

[Connection State]
Communication setting and application processing will be performed in Active mode.

[Short Interval or Application Processing State]
Short period (≦40msec) between communications and simple application processing will be performed in Sleep mode.

[Long Interval State]
Deep sleep mode will be used during a long period of waiting for radio commutication or when no access is made by HOST for a certain time in a non-communication period. Deep sleep mode is kept with 32.768KHz low power clock from an external pin.
(Note) In this state, the communication interval is counted by the internal timer, enabling ML7105 to return from the Deep Sleep mode temporarily at the timer expiration (at about 40-second interval). When you want to keep the Deep Sleep state, make a transition to the Sleep State.

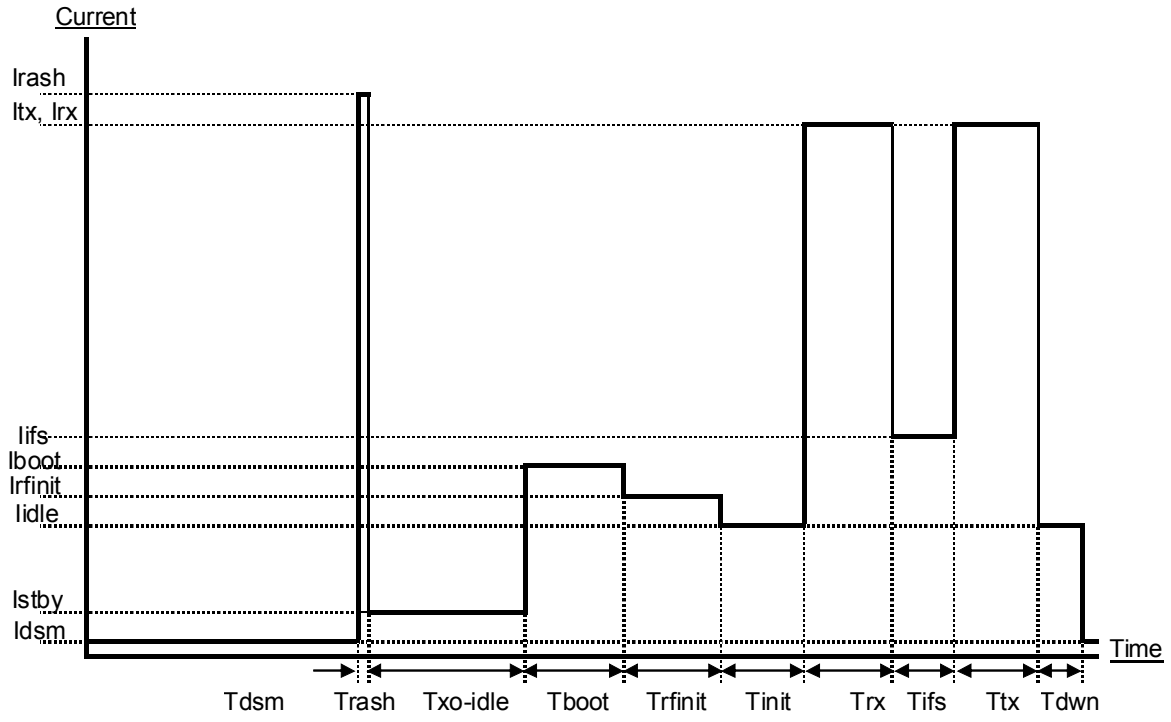
[Sleep State]
It is allowed to become Shutdown state if all operations can be temporarily stopped, by BACI command or HCI vender command. Sleep mode will suspend 26MHz clock in RF block, and be kept with 32.768KHz low power clock from external pin till wakeup.
(Note) In the HCI Mode, the transition to the Long Interval State or Sleep State is not performed.

●Wakeup Factor

Wakeup Factor is necessary to return from Deep sleep mode or Application Sleep. Wakeup Factor, low state of GPIO1 pin or WAKEUP pin, will be detected, and RF block clock will start to oscillate.

●Current Profile

Following example shows current consumption and power state transition waking up from Deep sleep mode, perform RX and TX and return to Deep sleep mode.



Status	Definition
Tdsm	Deepsleep period depend on connection interval
Trash	Spike from voltage regulator wake-up
Txo_idle	Start up time for xtal oscillator block for systems clock 26MHz
Tboot	System is in booting operation
Trfinit	Initialize RF register
Tinit	Pre-processing after deep sleep mode
Trx	Packet reception
Tifs	Time between RX to TX operation
Ttx	Packet transmission
Tdwn	Post processing before moving to deep sleep operation

■HOST interfaces

●Overview

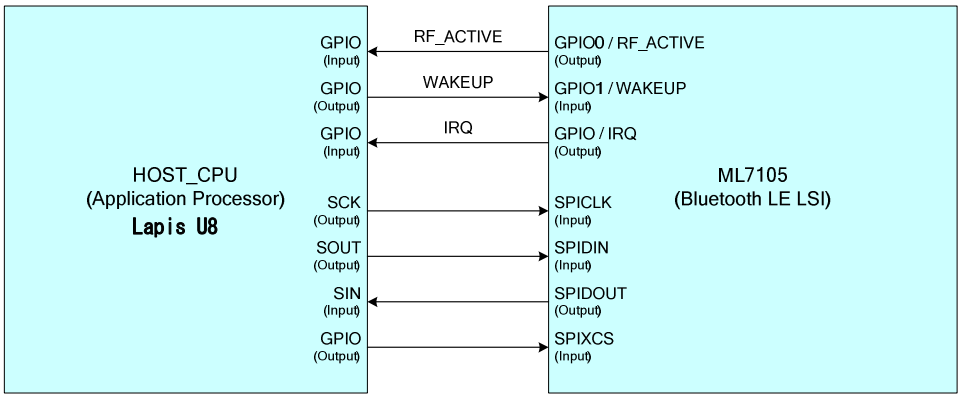
There are two host interfaces available shown below.

《SPI interface – BACI Mode》
SPI-SLAVE intrerface will be used as HOST interface. HOSTsystem can send command or receive event information via through SPI inrerface.

《UART interface – HCI Mode & Debug Mode》
UART intrerface will be used as HOST interface. HOST system can send command or receive event information via through UART interface.

●Connection with HOST system

Connection with HOST system consist of serial interface (UART or SPI-SLAVE) and 3pins of GPIO. Following example shows SPI-SLAVE used as HOST interface.



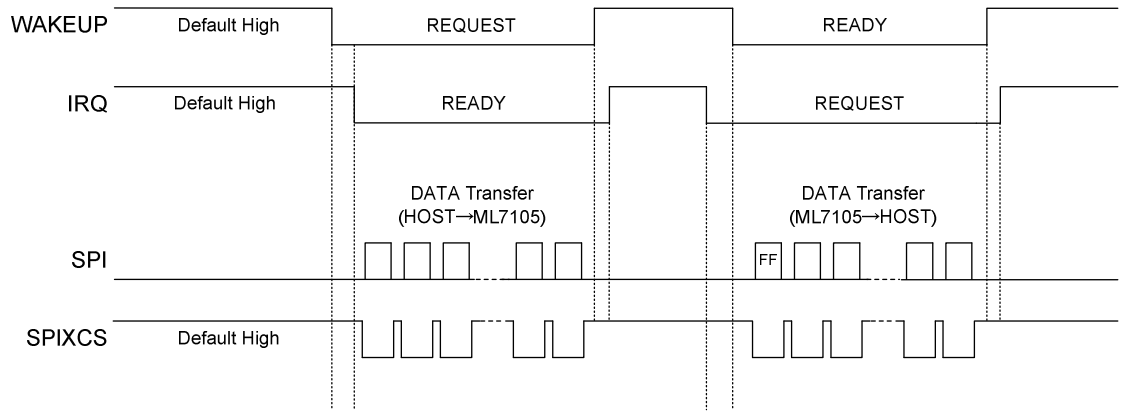
3pins of GPIO have following functionality.

RF_ACTIVE: Indicates Bluetooth communication is active or trans from Deep Sleep to IDLE/(shows higher current load).
When ML7105 wake-up from DeepSleep by internal timer, RF_ACTIVE Indicates rush current .
But when ML7105 wakes-up from DeepSleep by WAKEUP pin, or wake-up from PowerDown, RF_ACTIVE indicates nothing.

WAKEUP: Control signal indicate REQUEST or READY status from HOST system to ML7105.
It has to be asserted Low before start SPI communication (REQUEST).

IRQ: IRQ indicates REQUEST or READY status from ML7105 to HOST system.
Once ML7105 receive REQUEST from HOST system and it become READY, ML7105 set IRQ signal to Low.
Reporting REQUEST from ML7105 will be done by asserting IRQ signal to low.

Behavior of each pins are described below.



The normal state of the RF_ACTIVE pin is Low. The normal states of the WAKEUP, IRQ, and SPIXCS pins are High.
The SPI communication is performed in the following sequence:

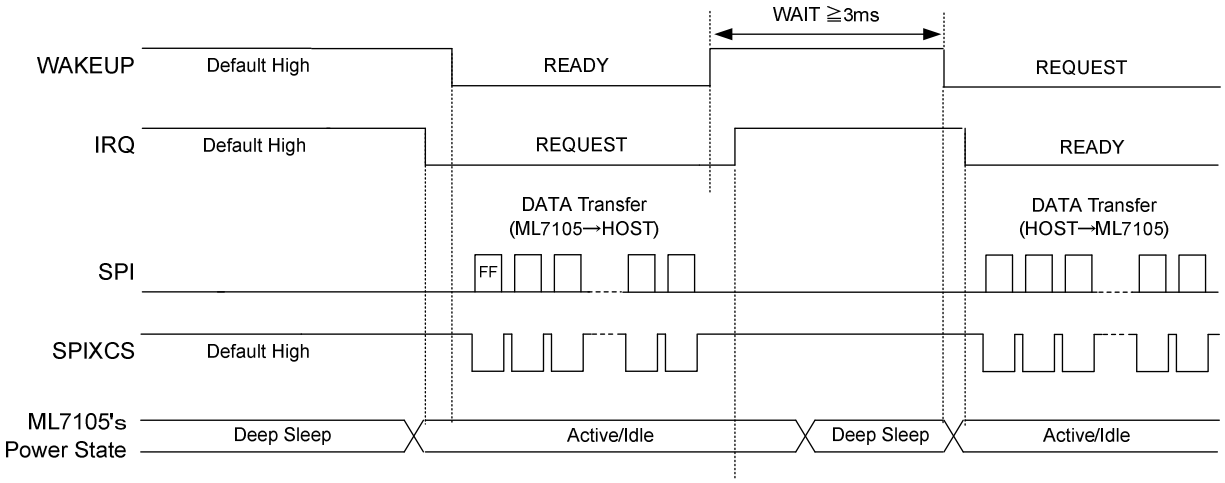
- Communication request from HOST
  1. HOST toggles the WAKEUP pin to Low.
  2. When ML7105 detects WAKEUP and goes to the READY state, ML7105 toggles the IRQ pin to Low.
  3. HOST starts the SPI communication. During the communication, HOST toggles the SPIXCS pin to Low.
  4. When the SPI communication is completed, HOST toggles the WAKEUP pin to High.
  5. When ML7105 detects that the WAKEUP pin turns to High, ML7105 toggles the IRQ pin to High.

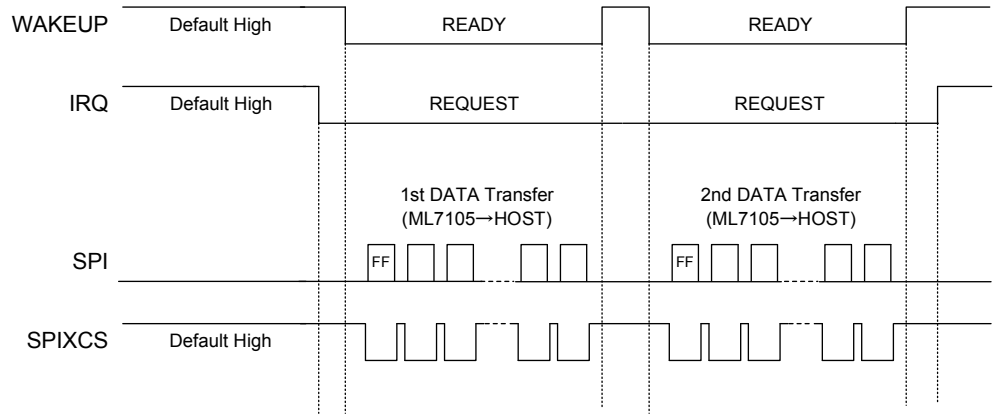
  [Note] When transmitting dummy data other than BACI packet from HOST, be sure to transmit 0xFF.

- Communication request from ML7105 (when transmitting one BACI packet)
  1. ML7105 toggles the IRQ pin to Low.
  2. When HOST detects IRQ and goes to the READY state, HOST toggles the WAKEUP pin to Low.
  3. HOST starts the SPI communication. During the communication, HOST toggles the SPIXCS pin to Low.
     ML7105 outputs the dummy data (0xFF) and then starts the transmission of the BACI packet.
  4. ML7105 starts transmitting the BACI packet.
  5. When HOST completes receiving the BACI packet, HOST must toggle the WAKEUP pin to High.
  6. When ML7105 detects that the WAKEUP pin turns to High, ML7105 toggles the IRQ pin to High.

- Timing control when a communication request from HOST is made

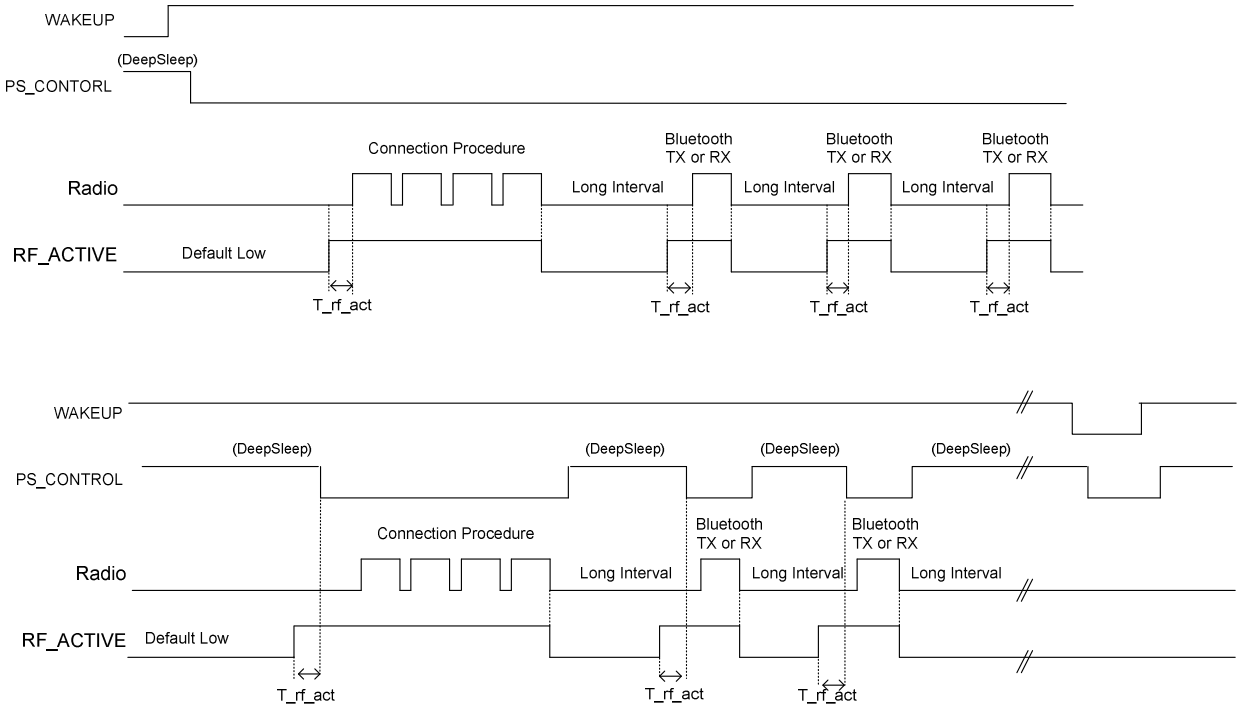
  After toggling the IRQ signal to High, ML7105 transitions to the Deep Sleep mode if no communication request from HOST is made for a specified period (about 1 ms). During this transition to the Deep Sleep mode, no communication request from HOST is accepted. Therefore, insert a WAIT of 3 ms or more after toggling the WAKEUP signal to High before toggling it to Low, so that a communication request from HOST can be accepted. If there is no IRQ signal response to the communication request from HOST, perform the retry process (toggle the WAKEUP signal back to High and then toggle it to Low again).





- Communication request from ML7105 (when transmitting two BACI packets continuously)
  1. ML7105 toggles the IRQ pin to Low.
  2. When HOST detects IRQ and goes to the READY state, HOST toggles the WAKEUP pin to Low.
  3. HOST starts the SPI communication. During the communication, HOST toggles the SPIXCS pin to Low.
     ML7105 outputs the dummy data (0xFF) and then starts the transmission of the BACI packet.
  4. When HOST completes receiving the BACI packet, HOST must toggle the WAKEUP pin to High.
  5. If there are more BACI packets to be transmitted continuously, ML7105 keeps IRQ in the Low state.
  6. When HOST detects that IRQ is in the Low state, HOST must toggle the WAKEUP pin to Low.
  7. HOST starts the SPI communication. During the communication, HOST toggles the SPIXCS pin to Low.
     ML7105 outputs the dummy data (0xFF) and then starts the transmission of the second BACI packet.
  8. When HOST completes receiving the BACI packet, HOST must toggle the WAKEUP pin to High.
  9. When ML7105 detects that the WAKEUP pin turns to High, ML7105 toggles the IRQ pin to High.

Behavior of RF_ACTIVE is shown below.



The RF_ACTIVE pin outputs High during the period of RF communication or calibration where an increased current is required.
The RF_ACTIVE pin outputs High also at return from Deep Sleep by the internal timer, since the current increases due to the rush current.
The RF_ACTIVE pin outputs High during the T_rf_act period before the current increases. The value of T_rf_act varies depending on the cause to be notified. When RF_ACTIVE notifies the current increase due to RF communication, T_rf_act is 625 µsec * 2 = about 1.2 msec or 625 µsec *3 = about 1.8 msec. On the other hand, T_rf_act is about 1 msec at return from Deep Sleep. The RF_ACTIVE pin is toggled to Low when the RF communication is completed or at transition to Deep Sleep.
While the RF communication continues, the RF_ACTIVE pin always outputs High.
At a return from power-down or at a return to IDLE from Deep Sleep by the WAKEUP pin, the current increases due to the rush current just like the case at the return from Deep Sleep by the internal timer. However, the RF_ACTIVE pin does not output High in this case.

●SPI interface description

Possible combination of parameters are described below when SPI-SLAVE block are used as HOST interface.

Table 1 SPI_SLAVE Settings

Parameter	Spec
Bit rate	Typ. 32.768KHz Max. 1.625MHz
SPI mode	Motorola SPI (Mode 3)
Data size	8 bits
Chip select	Low Active

●UART interface description

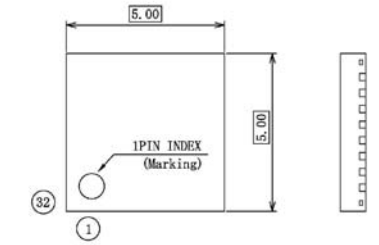
Possible combination of parameters are described below when UART block are used as HOST interface.

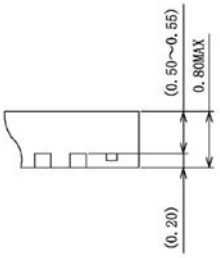
Table 2 UART Settings

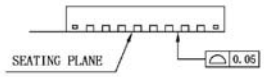
Parameter	Spec
Baud rate	57600bps
Data size	8 bits
Parity bit	No parity
Stop bit	1 stop bit
Flow control	No

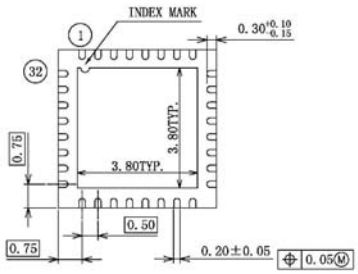
■Package dimensions

P-WQFN32-0505-0.50-A63









LAPIS Semiconductor Co.,Ltd.

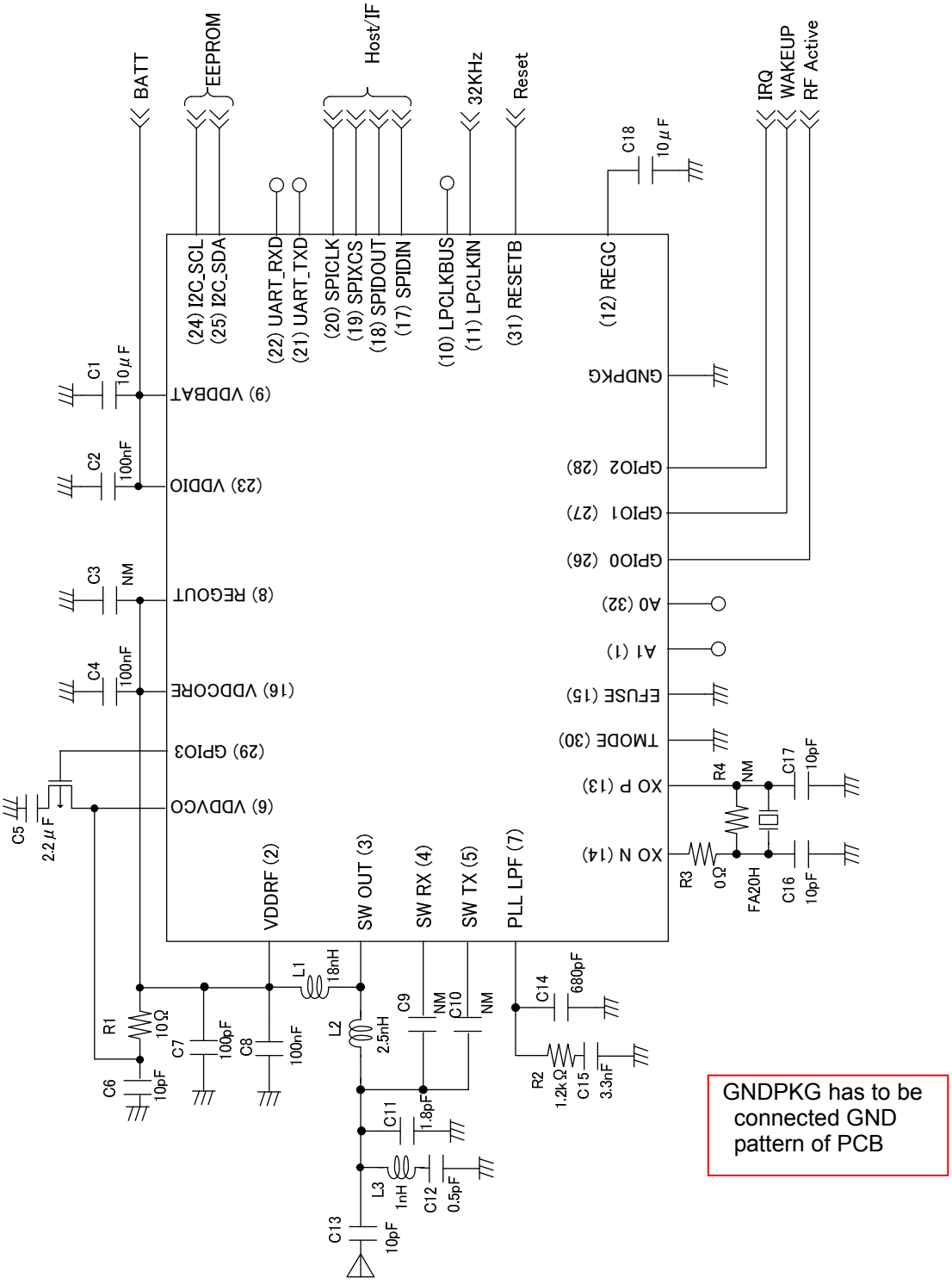
Package material	Epoxy resin
Lead frame material	Cu alloy
Lead finish	Ni/Pd/Au
Pin treatment (μm)	Au/Pd 0.01 max./0.15 max.
Package weight (g)	0.055 TYP.
Rev. No./Last Revised	2/Sep. 21 2011

Notes for Mounting the Surface Mount Type Packages

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

■Application example

The following circuit shows the typical application circuit. This circuit may vary depending on the shipment time or other factor. This circuit shows ML7105 Application example and does not guarantee the characteristics.
It is recommended that choosing and finalize the best component valuse by evaluationg on the target board.



■Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7105-002-01	June, 10, 2013	–	–	Final 1st Edition

NOTES

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