EV8AQ160

Quad 8-bit 1.25 Gsps
Dual 8-bit 2.5 Gsps
Single 8-bit 5 Gsps

Datasheet *Summary*

1. Main Features

- Quad ADC with 8-bit Resolution
  - 1.25 Gsps Sampling Rate in Four-channel Mode
  - 2.5 Gsps Sampling Rate in Two-channel Mode
  - 5 Gsps Sampling Rate in One-channel Mode
  - Built-in four to Four Cross Point Switch
- 2.5 GHz Differential Symmetrical Input Clock Required
- ADC Master Reset (LVDS)
- Double Data Rate Output Protocol
- LVDS Output Format
- Digital Interface (SPI) with Reset Signal
  - Selectable 1:1 or 1:2 Demultiplexed Outputs
  - Channel Mode Selection
  - 500 mVpp or 625 mVpp Analog Input (Differential AC or DC Coupled, Single-ended AC-coupled)
  - Selectable bandwidth (Four Available Settings)
  - Gain Control (±15%)
  - Offset Control (±40 mV)
  - Phase Control (±15 ps Range)
  - Standby Mode (Full or Partial)
  - Binary or Gray Coding Selection
  - Test Mode
- Power Supplies: 3.3V and 1.8V (Outputs), 1.8V (Digital)
- Power Dissipation: 3.9 W Total (1:1 DMUX Mode)
- EBGA380 Package (RoHS, 1.27 mm Pitch)

2. Performance

- Selectable 2.5 GHz, 1.5 GHz, 800 MHz or 600 MHz
- Full Power Input Bandwidth (–3 dB)
- Band Flatness: ±0.5 dB from DC to 30% of Full Power Input Bandwidth
- Channel-to-channel Isolation: 60 dB
- Four-channel Mode (Fsampling = 1.25 Gsps, –1 dBFS)
  - Fin = 100 MHz: ENOB = 7.5 bit, SFDR = 52 dBc, SNR = 48 dB, DNL = ±0.25 LSB, INL = ±0.25 LSB
  - Fin = 620 MHz: TBD
- Two-channel Mode (Fsampling = 2.5 Gsps, –1 dBFS)
  - Fin = 100 MHz: ENOB = 7.3 bit, SFDR = 51 dBc, SNR = 46 dB, DNL = ±0.4 LSB, INL = ±0.5 LSB
  - Fin = 620 MHz: TBD
- One-channel Mode (Fsampling = 5 Gsps, Fin = 100 MHz, –1 dBFS)
  - Fin = 100 MHz: ENOB = 7.1 bit, SFDR = 49 dBc, SNR = 44 dB, DNL = ±0.5 LSB, INL = ±0.5 LSB
  - Fin = 620 MHz: TBD
  - BER: 10^{-16} at 1.25 Gsps per ADC

Visit our website: www.e2v.com
for the latest version of the datasheet

3. Screening

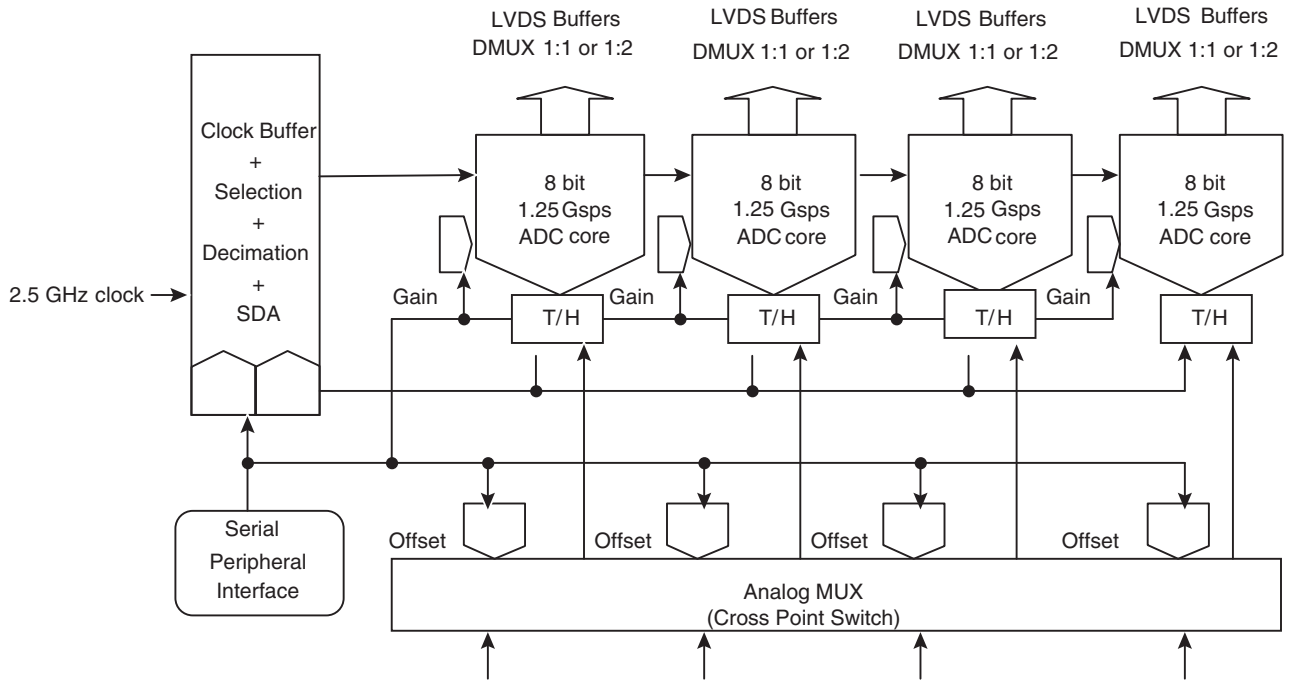
- Temperature range for packaged device:
  - Commercial *C* grade: 0°C < T_{amb} < 70°C

4. Applications

- High-speed Digital Oscilloscopes.

5. Block Diagram

Figure 5-1. Simplified Block Diagram



6. Description

The Quad ADC is constituted by four 8-bit ADC cores which can be considered independently (four-channel mode) or grouped by two cores (two-channel mode with the ADCs interleaved two by two or one-channel mode where all four ADCs are all interleaved.)

All four ADCs are clocked by the same external input clock signal and controlled via an SPI (Serial Peripheral Interface). An analog multiplexer (cross point switch) is used to select the analog input depending on the mode the Quad ADC is used.

The Clock Circuit is common to all four ADCs. This block receives an external 2.5 GHz clock (maximum frequency) and preferably a low jitter sinewave signal. In this block, the external clock signal is then divided by two in order to generate the internal sampling clocks:

– In four-channel mode, the same 1.25 GHz clock is directed to all four ADC cores and T/H.
– In two-channel mode, the in-phase 1.25 GHz clock is sent to ADC A or C and the inverted 1.25 GHz clock is sent to ADC B or D, while the analog input is sent to both ADCs, resulting in an interleaved mode with an equivalent sampling frequency of 2.5 Gsps.
– In one-channel mode, the in-phase 1.25 GHz clock is sent to ADC A while the inverted 1.25 GHz clock is sent to ADC B, the in-phase 1.25 GHz clock is delayed by 90° to generate the clock for ADC C and the inverted 1.25 GHz clock is delayed by 90° to generate the clock for ADC D, resulting in an interleaved mode with an equivalent sampling frequency of 5 Gsps.

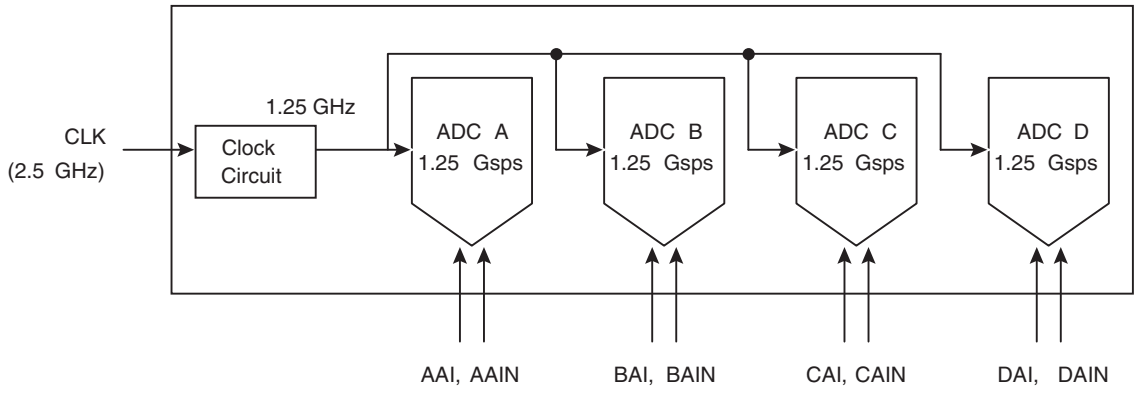
The clock circuit also implements a decimation function with a selectable factor (64, 16, 4). The factor is chosen via the SPI.

Several adjustments for the sampling delay and the phase are included in this clock circuit to ensure a proper phase relation between the different clocks generated internally from the 2.5 GHz clock.

The *cross point switch* (Analog MUX) is common to all ADCs. It allows to select which analog input has been chosen by the user:

– In four-channel mode, each analog input is sent to the corresponding ADC (AAI to ADC A, BAI to ADC B, CAI to ADC C and DAI to ADC D)
– In two-channel mode, one can consider that there 2 two independent ADCs composed of ADC A and B for the first one and of ADC C and D for the second one; the two analog inputs can be applied on AAI or on BAI for the first ADC (in which case, the signal is redirected internally to the second ADC of the pair that is B or A respectively) and on CAI or DAI (in which case, the signal is redirected internally to the second ADC of the pair, that is D or C respectively)
– In one-channel mode, one analog input is chosen among AAI, BAI, CAI and DAI and then sent to all four ADCs

Figure 6-1. Four-channel Mode Configuration



0846BS–BDC–07/07

Figure 6-2. Two-channel Mode Configuration (Analog Input A and Analog Input C)

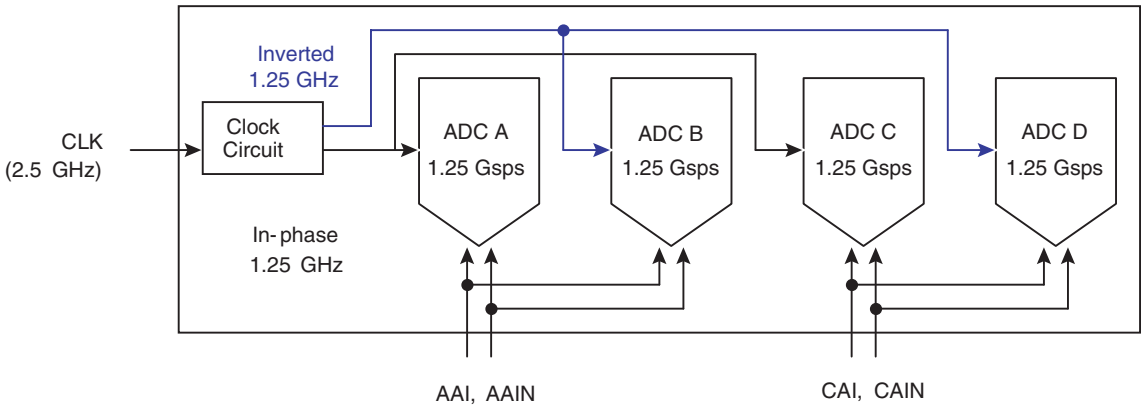


Figure 6-3. Two-channel Mode Configuration (Analog Input A and Analog Input D)

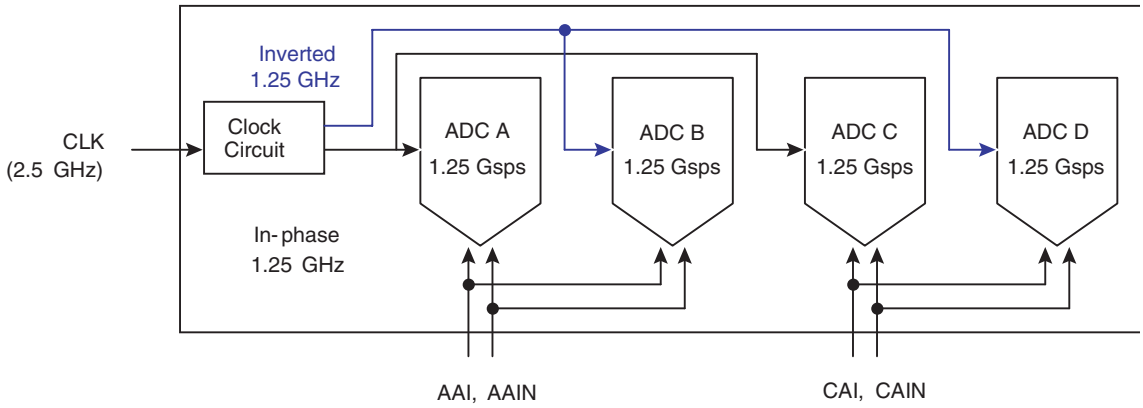


Figure 6-4. Two-channel Mode Configuration (Analog Input B and Analog Input C)

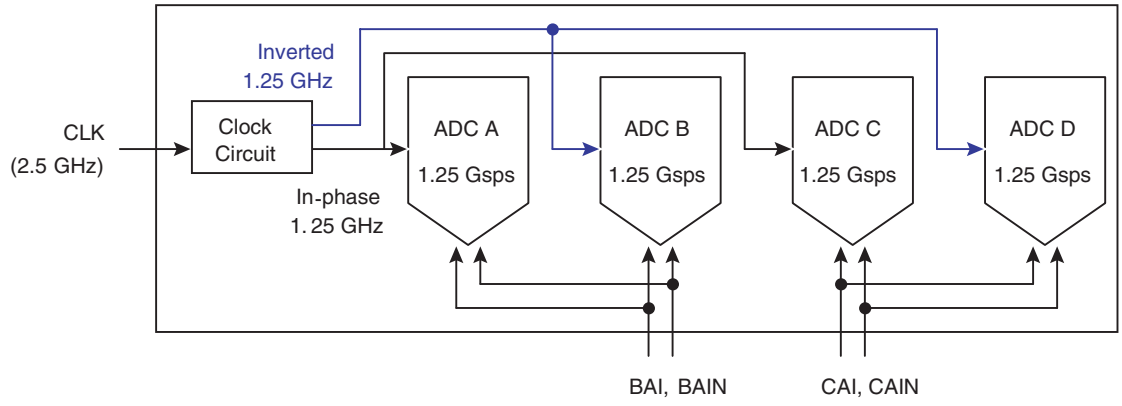


Figure 6-5. Two-channel Mode Configuration (Analog Input B and Analog Input D)

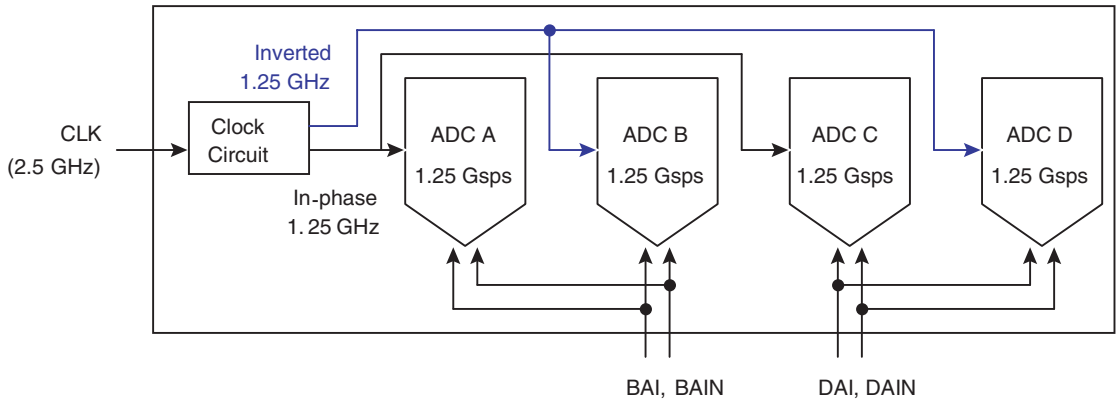
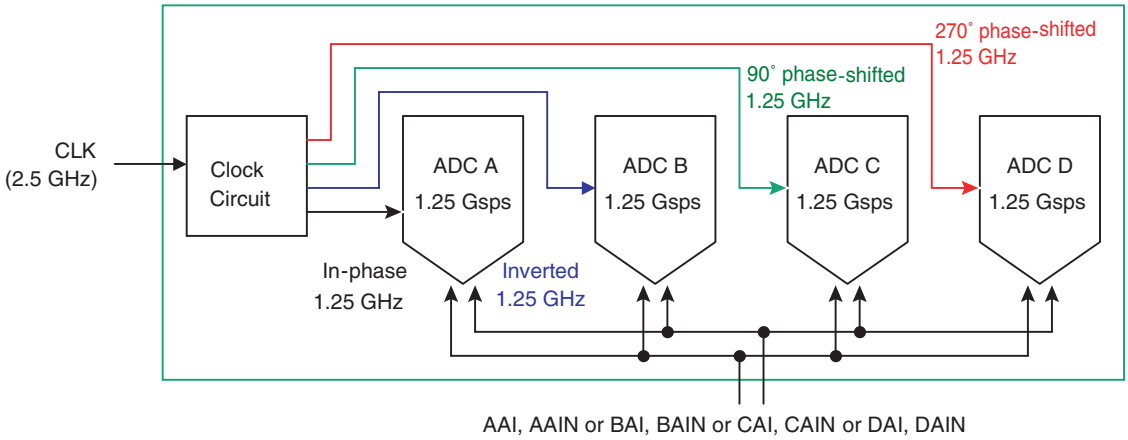


Figure 6-6. One-channel Mode Configuration



Note: For simplification purpose of the timer the temporal order of ports regarding sampling is A C B D, therefore samples order at output port is as follows:
A: N, N + 4, N + 8, N + 12…
C: N + 1, N + 5, N + 9…
B: N + 2, N + 6, N + 10…
D: N + 3, N + 7, N + 11…

The T/H (Track and Hold) is located after the Cross Point Switch and before the ADC cores. This block is used to track the data when the internal sampling clock is low and to hold the data when the internal sampling clock is high. This stage has a gain of two.

The ADC cores are all the same for the four ADCs. They include a quantifier block as well as a fast logic block composed of regenerating latches and the Binary/Gray decoding block. They can handle a maximum sampling rate of 1.25 Gsps.

The SPI block provides the digital interface for the digital controls of the ADCs. All the functions of the ADC are contained in the SPI registers and controlled via this SPI (channel selection, standby mode, Binary or Gray coding, 1:1 or 1:2 DMUX, offset, gain and phase adjust, etc.).

The demultiplexer block allows the user to divide the output data rate by a factor of 2 (1:2 DMUX, selectable via the SPI, in the Control register), hence decreasing the output rate to a maximum of 625 Msps instead of 1.25 Gsps in double data rate.

The output buffers are LVDS compatible. They should be terminated using a 100Ω external termination resistor. When the 1:1 DMUX ratio is selected, half of the output data buffers (*L* port data bits) is switched off to optimize the power consumption. In this mode, the *L* port data bits can then be left floating (no termination required), since both outputs of the buffers will deliver High logical level.

The ADC SYNC buffer is also LVDS compatible. When active, the SYNC signal makes the output clock signals go low. The output data are undetermined during the reset and until the output clock restarts.

When the SYNC signal is released, the output clock signals restart after TDR + pipeline delay + a certain number of input clock cycles which is programmed via the SPI in the SYNC register (from minimum delay [TBD] to minimum delay + 15 × 2 input clock cycles).

A diode for the die junction temperature monitoring is implemented using a diode-mounted transistor but not connected to the die: both cathode and anode are accessible externally.

Eight DACs for the gain and the offset controls are included in the design and are addressed through the SPI:

– Offset DACs act close to the cross point switch

– Gain DACs act on the biasing of the reference ladders of each ADC core

These DACs have a resolution of 8-bit and will allow the control via the SPI of the offset and gain of the ADCs:

– Gain adjustment on 256 steps, ±15% range

– Offset adjustment on 256 steps, ±40 mV range

Four DACs for fine phase control are included in the design and are addressed through the SPI, they have an 8-bit resolution, and a tuning range of ±15 ps (one step is about 120 fs).

7. Specifications

7.1 Recommended Conditions of Use

Table 7-1. Recommended Conditions of Use

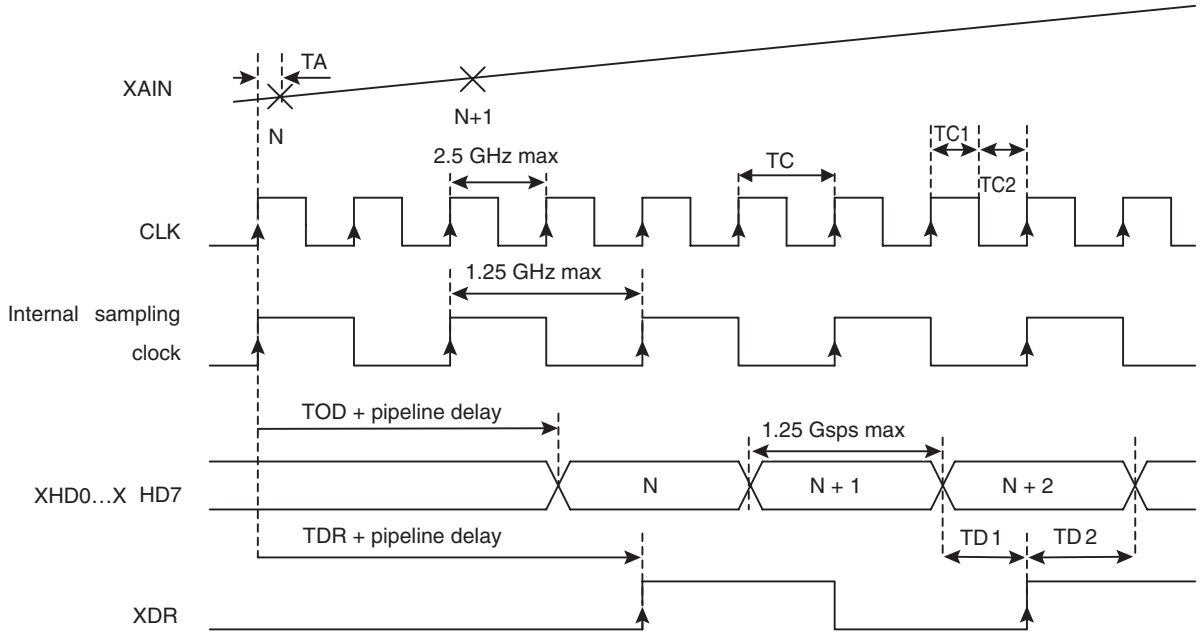
Parameter	Symbol	Comments	Recommended Value	Unit
Positive supply voltage	V_{CC}	analog core and SPI pads	3.3	V
Positive digital supply voltage	V_{CCD}	Digital parts	1.8	V
Positive output supply voltage	V_{CCO}	Output buffers	1.8	V
Differential analog input voltage (Full Scale)	V_{IN}, V_{INN} $V_{IN} – V_{INN}$		±250 500	mV mVpp

Table 7-1. Recommended Conditions of Use

Parameter	Symbol	Comments	Recommended Value	Unit
Clock input power level	P_{CLK}, P_{CLKN}		0	dBm
Clock frequency	F_{CLK}		2.5	GHz
Operating temperature range	T_{amb}	Commercial grade	0°C < T_{amb} < 70°C	°C
Storage temperature	T_{stg}		–65 to 150	°C

7.2 Timing Information

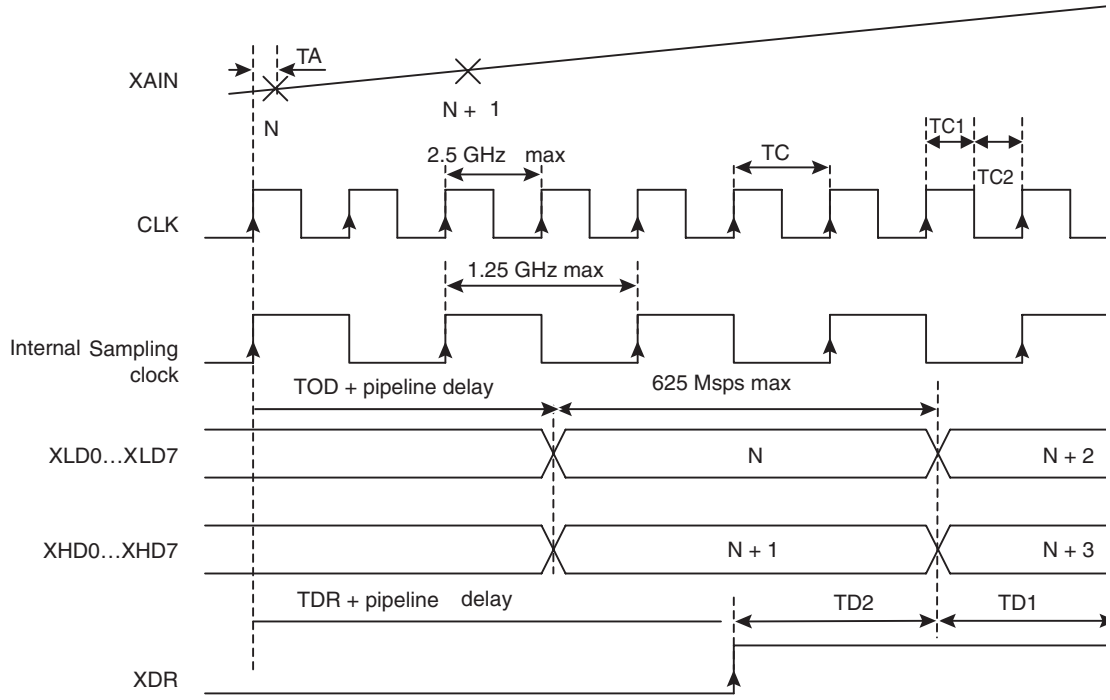
Figure 7-1. ADC Timing in Four-channel Mode, 1:1 DMUX Mode (for Each Channel)



Note: X refers to A, B, C and D

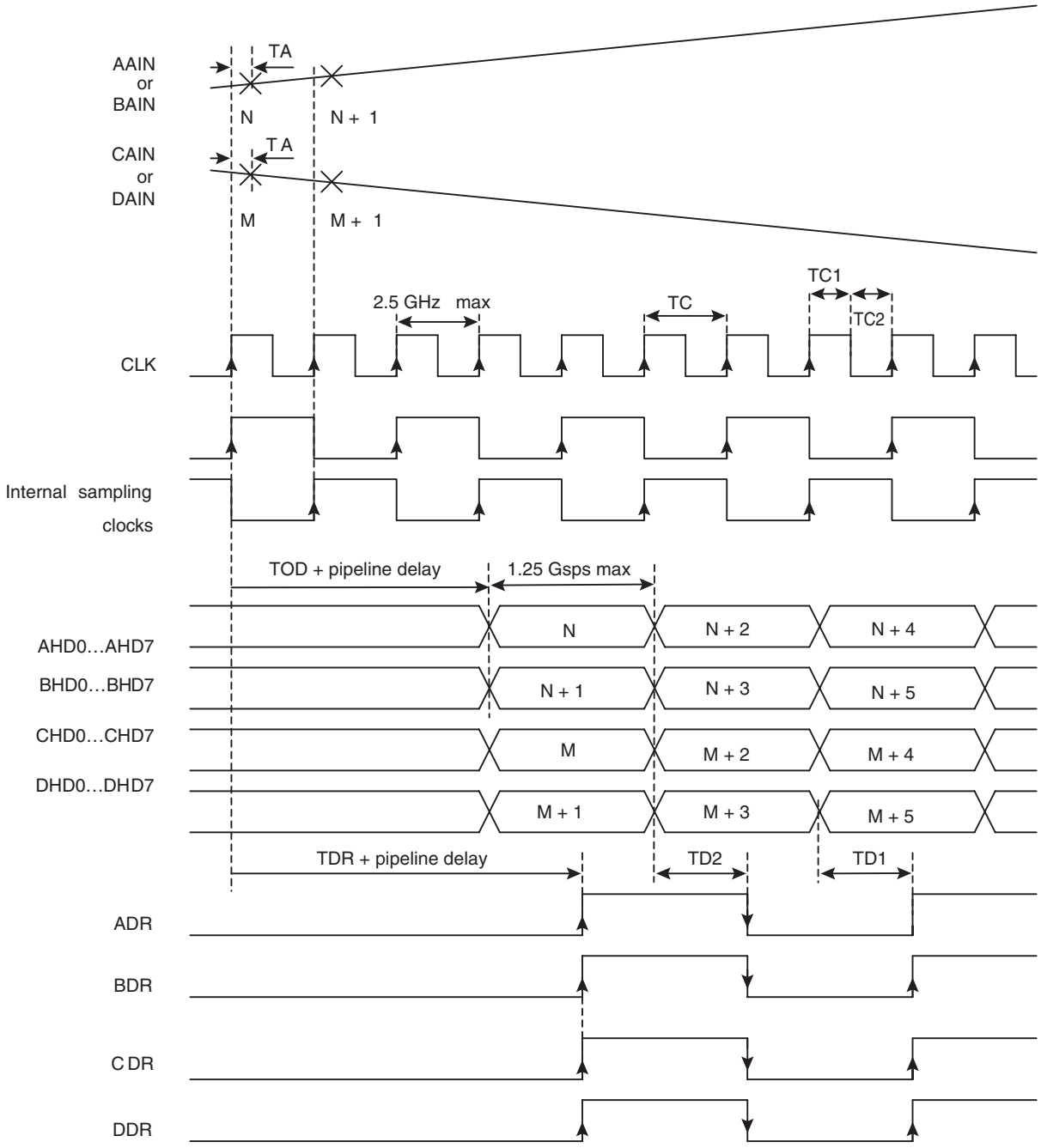
0846BS–BDC–07/07

Figure 7-2. ADC Timing in Four-channel Mode, 1:2 DMUX Mode (for Each Channel)



Note: X refers to A, B, C and D.

Figure 7-3. ADC Timing in Two-channel Mode, 1:1 DMUX Mode

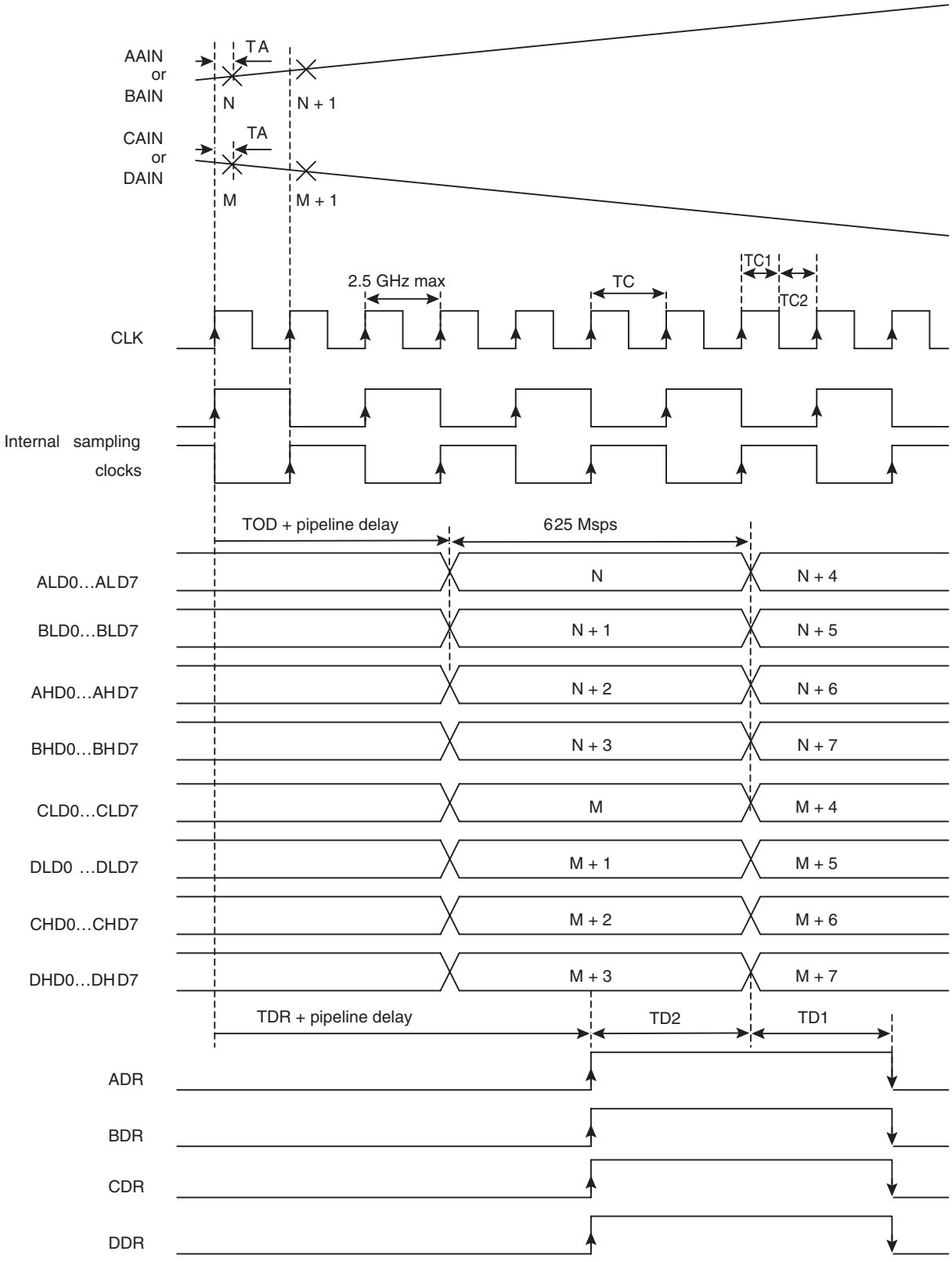


Note: In two-channel mode, the two analog inputs can be applied on:

– (AAI, AAIN) and (CAI, CAIN), in which case, the outputs corresponding to (AAI, AAIN) will be on AHD0…AHD7 and BHD0…BHD7 and the ones corresponding to (CAI, CAIN) on CHD0…CHD7 and DHD0…DHD7

– or (AAI, AAIN) and (DAI, DAIN), in which case, the outputs corresponding to (AAI, AAIN) will be on AHD0…AHD7 and BHD0…BHD7 and the ones corresponding to (DAI, DAIN) on CHD0…CHD7 and DHD0…DHD7
– or (BAI, BAIN) and (CAI, CAIN), in which case, the outputs corresponding to (BAI, BAIN) will be on AHD0…AHD7 and BHD0…BHD7 and the ones corresponding to (CAI, CAIN) on CHD0…CHD7 and DHD0…DHD7
– or (BAI, BAIN) and (DAIN, DAIN), in which case, the outputs corresponding to (BAI, BAIN) will be on AHD0…AHD7 and BHD0…BHD7 and the ones corresponding to (DAI, DAIN) on CHD0…CHD7 and DHD0…DHD7

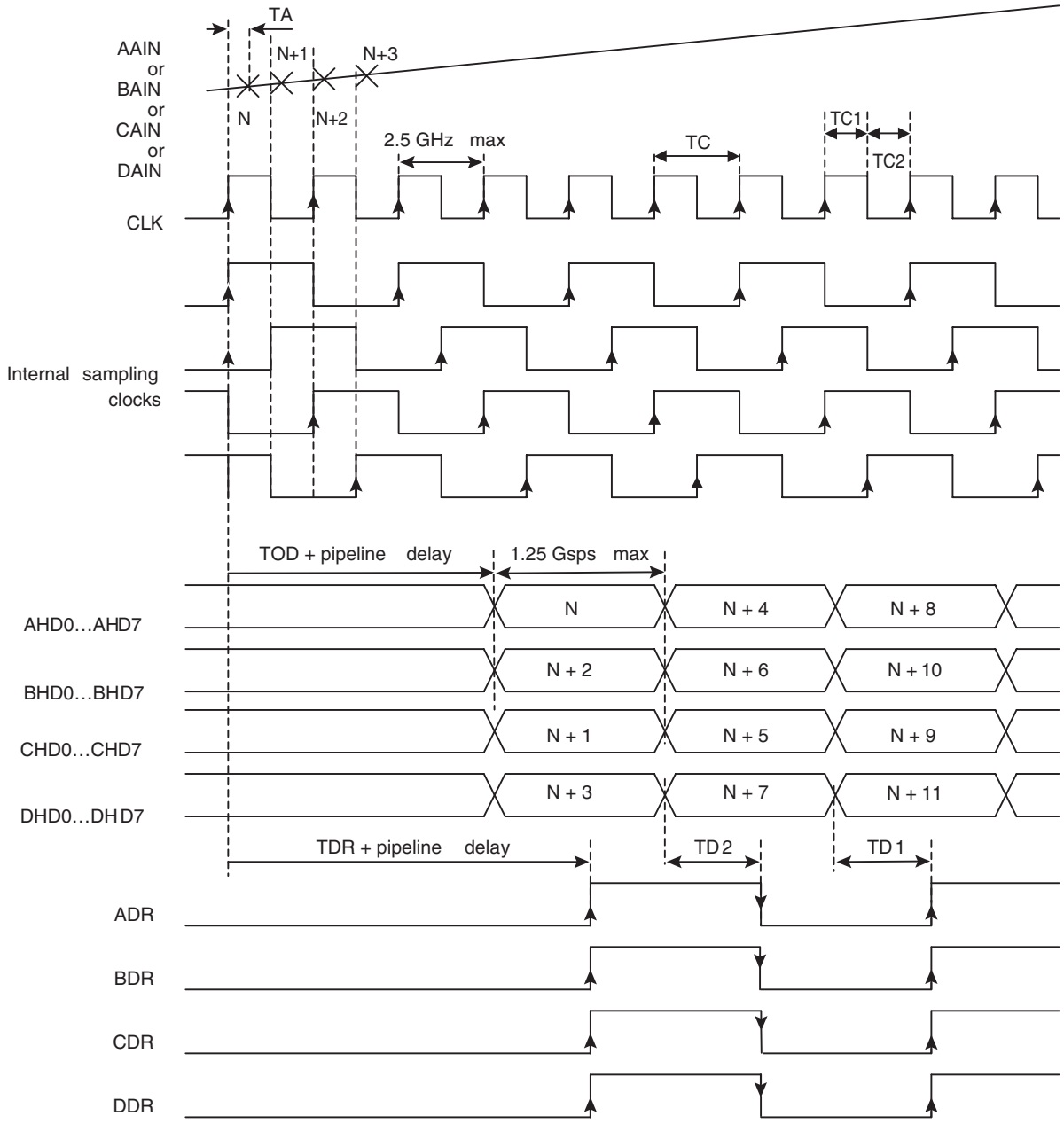
Figure 7-4. ADC Timing in Two-channel Mode, 1:2 DMUX Mode



Note:

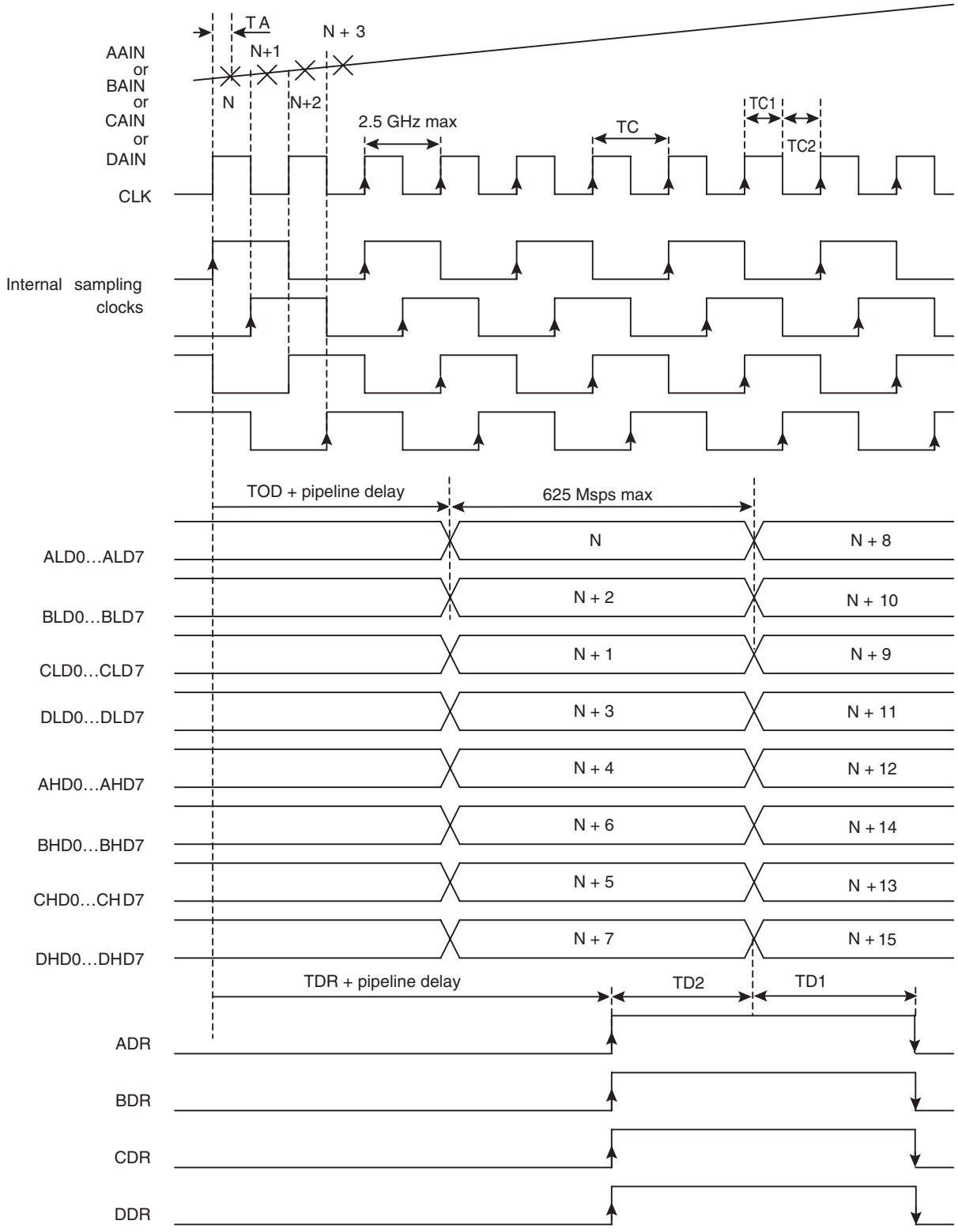
- AAI, AAIN) and (CAI, CAIN), in which case, the outputs corresponding to (AAI, AAIN) will be on ALD0…ALD7, AHD0…AHD7 and BLD0…BLD7, BHD0…BHD7 and the ones corresponding to (CAI, CAIN) on CLD0…CLD7, CHD0…CHD7 and DLD0…DLD7, DHD0…DHD7
- or (AAI, AAIN) and (DAI, DAIN), in which case, the outputs corresponding to (AAI, AAIN) will be on ALD0…ALD7, AHD0…AHD7 and BLD0…BLD7, BHD0…BHD7 and the ones corresponding to (DAI, DAIN) on CLD0…CLD7, CHD0…CHD7 and DLD0…DLD7, DHD0…DHD7
- or (BAI, BAIN) and (CAI, CAIN), in which case, the outputs corresponding to (BAI, BAIN) will be on ALD0…ALD7, AHD0…AHD7 and BLD0…BLD7, BHD0…BHD7 and the ones corresponding to (CAI, CAIN) on CLD0…CLD7, CHD0…CHD7 and DLD0…DLD7, DHD0…DHD7
- or (BAI, BAIN) and (DAIN, DAIN), in which case, the outputs corresponding to (BAI, BAIN) will be on ALD0…ALD7, AHD0…AHD7 and BLD0…BLD7, BHD0…BHD7 and the ones corresponding to (DAI, DAIN) on CLD0…CLD7, CHD0…CHD7 and DLD0…DLD7, DHD0…DHD7

Figure 7-5. ADC Timing in One-channel Mode, 1:1 DMUX Mode



Note: In one-channel mode, the analog input can be applied on (AAI,AAIN), (BAI, BAIN), (CAI, CAIN) or (DAI, DAIN). The choice is made via the SPI in the control register.

Figure 7-6. ADC Timing in One-channel Mode, 1:2 DMUX Mode



Note: In one-channel mode, the analog input can be applied on (AAI,AAIN), (BAI, BAIN), (CAI, CAIN) or (DAI, DAIN). The choice is made via the SPI in the control register.

8. Coding

Table 8-1. ADC Coding Table

Differential analog input	Voltage level	Digital Output			
		Binary		Gray	
		MSB……....LSB	Out-of-range	MSB……....LSB	Out-of-range
> + 250.25 mV	>Top end of full scale + ½ LSB	1 1 1 1 1 1 1 1	1	1 1 1 1 1 1 1 1	1
+250.25 mV + 249.75 mV	Top end of full scale + ½ LSB	1 1 1 1 1 1 1 1	0	1 1 1 1 1 1 1 1	0
	Top end of full scale - ½ LSB	1 1 1 1 1 1 1 0	0	1 1 1 1 1 1 1 0	0
+125.25 mV + 124.75 mV	3/4 full scale + ½ LSB	1 1 0 0 0 0 0 0	0	1 1 0 0 0 0 0 0	0
	3/4 full scale - ½ LSB	1 0 1 1 1 1 1 1	0	1 0 1 1 1 1 1 1	0
+0.25 mV- 0.25 mV	Mid scale + ½ LSB	1 0 0 0 0 0 0 0	0	1 0 0 0 0 0 0 0	0
	Mid scale - ½ LSB	0 1 1 1 1 1 1 1	0	0 1 1 1 1 1 1 1	0
–124.75 mV – 124.25 mV	1/4 full scale + ½ LSB	0 1 0 0 0 0 0 0	0	0 1 0 0 0 0 0 0	0
	1/4 full scale – ½ LSB	0 0 1 1 1 1 1 1	0	0 0 1 1 1 1 1 1	0
–249.75 mV – 250.25 mV	Bottom end of full scale + ½ LSB	0 0 0 0 0 0 0 1	0	0 0 0 0 0 0 0 1	0
	Bottom end of full scale –½ LSB	0 0 0 0 0 0 0 0	0	0 0 0 0 0 0 0 0	0
< – 250.25 mV	< Bottom end of full scale –½ LSB	0 0 0 0 0 0 0 0	1	0 0 0 0 0 0 0 0	1

9. Pin Description

9.1 Pinout View (Bottom View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
AD	GND	VCC	BLD6	BLD7	BLOR	GND	DiodA	tdreadyp	tdcop	trigp	SYNCP	CLK	CLKN	scan0	scan2	sclk	mosi	Res50	GND	CLOR	CLD7	CLD6	VCC	GND
AC	GND	VCC	BLD6N	BLD7N	BLORN	GND	DiodC	tdreadyn	tdcon	trign	SYNCN	GND	GND	scan1	rstn	csn	miso	Res62	GND	CLORN	CLD7N	CLD6N	VCC	GND
AB	BHOR	BHORN	VCC	GND	VCC	GND	VCC	GND	GND	VCC	VCCD	GND	GND	VCC	VCC	GND	GND	VCC	GND	VCC	GND	VCC	CHORN	CHOR
AA	BHD7	BHD7N	VCC	GND	VCCO	VCC	VCC	GND	GND	VCC	VCCD	GND	GND	VCC	VCC	GND	GND	VCC	VCC	VCCO	GND	VCC	CHD7N	CHD7
Y	BHD6	BHD6N	VCCO	GND	GND	VCCO	VCC	GND	GND	VCC	VCCD	GND	GND	VCC	VCC	GND	GND	VCC	VCCO	GND	GND	VCCO	CHD6N	CHD6
W	BHD5	BHD5N	VCCO	GND	GND															GND	GND	VCCO	CHD5N	CHD5
V	BHD4	BHD4N	BLD5	BLD5N	GND															GND	CLD5N	CLD5	CHD4N	CHD4
U	BHD3	BHD3N	BLD4	BLD4N	VCCO															VCCO	CLD4N	CLD4	CHD3N	CHD3
T	BHD2	BHD2N	BLD3	BLD3N	GND															GND	CLD3N	CLD3	CHD2N	CHD2
R	BHD1	BHD1N	BLD2	BLD2N	VCC															VCC	CLD2N	CLD2	CHD1N	CHD1
P	BHD0	BHD0N	BLD1	BLD1N	GND															GND	CLD1N	CLD1	CHD0N	CHD0
N	BDR	BDRN	BLD0	BLD0N	VCC															VCC	CLD0N	CLD0	CDRN	CDR
M	ADR	ADRN	ALD0	ALD0N	VCC															VCC	DLD0N	DLD0	DDRN	DDR
L	AHD0	AHD0N	ALD1	ALD1N	GND															GND	DLD1N	DLD1	DHD0N	DHD0
K	AHD1	AHD1N	ALD2	ALD2N	VCC															VCC	DLD2N	DLD2	DHD1N	DHD1
J	AHD2	AHD2N	ALD3	ALD3N	GND															GND	DLD3N	DLD3	DHD2N	DHD2
H	AHD3	AHD3N	ALD4	ALD4N	VCCO															VCCO	DLD4N	DLD4	DHD3N	DHD3
G	AHD4	AHD4N	ALD5	ALD5N	GND															GND	DLD5N	DLD5	DHD4N	DHD4
F	AHD5	AHD5N	VCCO	GND	GND															GND	GND	VCCO	DHD5N	DHD5
E	AHD6	AHD6N	VCCO	GND	GND	VCCO	VCC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC	VCCO	GND	GND	VCCO	DHD6N	DHD6
D	AHD7	AHD7N	VCC	GND	VCCO	VCC	VCC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC	VCC	VCCO	GND	VCC	DHD7N	DHD7
C	AHOR	AHORN	VCC	GND	VCC	VCC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC	VCC	GND	VCC	DHORN	DHOR
B	GND	VCC	ALD6N	ALD7N	ALORN	GND	GND	GND	GND	GND	GND	CMIRefAB	CMIRefCD	GND	GND	GND	GND	GND	GND	DLORN	DLD7N	DLD6N	VCC	GND
A	GND	VCC	ALD6	ALD7	ALOR	GND	AAI	AAIN	GND	BAI	BAIN	GND	GND	CAI	CAIN	GND	DAI	DAIN	GND	DLOR	DLD7	DLD6	VCC	GND

VCC=3.3V VCCO = 1.8V VCCD = 1.8V

9.2 Pinout Table

Table 9-1. Pinout Table

Pin Label	Pin Number	Description
Power supplies		
GND	A1, A6, A9, A12, A13, A16, A19 A24, B1, B6, B7, B8, B9, B10, B11, B14, B15, B16, B17, B18, B19, B24, C4, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C21, D4, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D21, E8, E9, E10, E11, E12, E13, E14, E15, E16, E17, J5, J20, L5, L20, P5, P20, T5, T20, Y8, Y9, Y12, Y13, Y16, Y17, AA4, AA8, AA9, AA12, AA13, AA16, AA17, AA21, AB4, AB6, AB8, AB9, AB12, AB13, AB16, AB17, AB19, AB21, AC1, AC6, AC12, AC13, AC19, AC24, AD1, AD6, AD19, AD24, E4, E5, E20, E21, F4, F5, F20, F21, G5, G20, V5, V20, W4, W5, W20, W21, Y4, Y5, Y20, Y21	Ground
VCC	A2, A23, B2, B23, C3, C5, C6C19, C20, C22, D3, D6, D7, D18, D19, D22, E7, E18, K5, K20, M5, M20, N5, N20, R5, R20, Y7, Y10, Y15, Y18, AA3, AA6, AA7, AA10, AA15, AA18, AA19, AA22, AB3, AB5, AB7, AB10, AB15, AB18, AB20, AB22, AC2, AC23, AD2, AD23, AA14, AB14, Y14	Analog + SPI pads power supply (3.3V)
VCCD	Y11, AB11, AA11	Digital power supply (1.8V)
VCCO	D5, D20, E3, E6, E19, E22, F3, F22, H5, H20, U5, U20, W3, W22, Y3, Y6, Y19, Y22, AA5, AA20	Output power supply (1.8V)
Clock signal		
CLK	AD12	In phase input clock signal
CLKN	AD13	Out of phase input clock signal
Analog input signals		
AAI	A7	In phase analog input channel A
AAIN	A8	Out of phase analog input channel A
BAI	A10	In phase analog input channel B
BAIN	A11	Out of phase analog input channel B
CAI	A14	In phase analog input channel C
CAIN	A15	Out of phase analog input channel C
DAI	A17	In phase analog input channel D
DAIN	A18	Out of phase analog input channel D

Table 9-1. Pinout Table (Continued)

Pin Label	Pin Number	Description
Digital output signals		
ALD0 ALD1 ALD2 ALD3 ALD4A LD5 ALD6 ALD7	M3 L3 K3 J3 H3 G3 A3 A4	Channel A port L in-phase output data
ALD0N ALD1N ALD2N ALD3N ALD4N ALD5N ALD6N ALD7N	M4 L4 K4 J4 H4 G4 B3 B4	Channel A port L out-of-phase output data
ALOR ALORN	A5 B5	Channel A port L out-of-range bit
AHD0 AHD1 AHD2 AHD3 AHD4 AHD5 AHD6 AHD7	L1 K1 J1 H1 G1 F1 E1 D1	Channel A port H in-phase output data
AHD0N AHD1N AHD2N AHD3N AHD4N AHD5N AHD6N AHD7N	L2 K2 J2 H2 G2 F2 E2 D2	Channel A port H out-of-phase output data
AHOR AHORN	C1 C2	Channel A port H out-of-range bit
ADR ADRN	M1 M2	Channel A output clock

Table 9-1. Pinout Table (Continued)

Pin Label	Pin Number	Description
BLD0 BLD1 BLD2 BLD3 BLD4 BLD5 BLD6 BLD7	N3 P3 R3 T3 U3 V3 AD3 AD4	Channel B port L in-phase output data
BLD0N BLD1N BLD2N BLD3N BLD4N BLD5N BLD6N BLD7N	N4 P4 R4 T4 U4 V4 AC3 AC4	Channel B port L out-of-phase output data
BLOR BLORN	AD5 AC5	Channel B port L out-of-range bit
BHD0 BHD1 BHD2 BHD3 BHD4 BHD5 BHD6 BHD7	P1 R1 T1 U1 V1 W1 Y1 AA1	Channel B port H in-phase output data
BHD0N BHD1N BHD2N BHD3N BHD4N BHD5N BHD6N BHD7N	P2 R2 T2 U2 V2 W2 Y2 AA2	Channel B port H out-of-phase output data
BHOR BHORN	AB1 AB2	Channel B port H out-of-range bit
BDR BDRN	N1 N2	Channel B output clock

Table 9-1. Pinout Table (Continued)

Pin Label	Pin Number	Description
CLD0 CLD1 CLD2 CLD3 CLD4 CLD5 CLD6 CLD7	N22 P22 R22 T22 U22 V22 AD22 AD21	Channel C port L in-phase output data
CLD0N CLD1N CLD2N CLD3N CLD4N CLD5N CLD6N CLD7N	N21 P21 R21 T21 U21 V21 AC22 AC21	Channel C port L out-of-phase output data
CLOR CLORN	AD20 AC20	Channel C port L out-of-range bit
CHD0 CHD1 CHD2 CHD3 CHD4 CHD5 CHD6 CHD7	P24 R24 T24 U24 V24 W24 Y24 AA24	Channel C port H in-phase output data
CHD0N CHD1N CHD2N CHD3N CHD4N CHD5N CHD6N CHD7N	P23 R23 T23 U23 V23 W23 Y23 AA23	Channel C port H out-of-phase output data
CHOR CHORN	AB24 AB23	Channel C port H Out of range bit
CDR CDRN	N24 N23	Channel C Output clock

Table 9-1. Pinout Table (Continued)

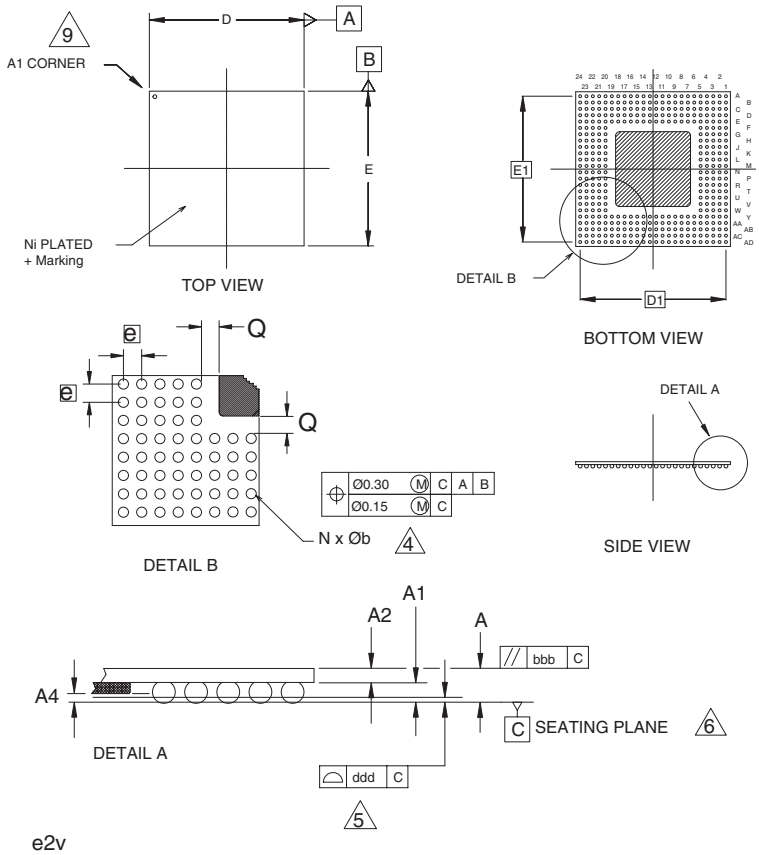
Pin Label	Pin Number	Description
DLD0 DLD1 DLD2 DLD3 DLD4 DLD5 DLD6 DLD7	M22 L22 K22 J22 H22 G22 A22 A21	Channel D port L in-phase output data
DLD0N DLD1N DLD2N DLD3N DLD4N DLD5N DLD6N DLD7N	M21 L21 K21 J21 H21 G21 B22 B21	Channel D port L out-of-phase output data
DLOR DLORN	A20 B20	Channel D port L out-of-range bit
DHD0 DHD1 DHD2 DHD3 DHD4 DHD5 DHD6 DHD7	L24 K24 J24 H24 G24 F24 E24 D24	Channel D port H in-phase output data
DHD0N DHD1N DHD2N DHD3N DHD4N DHD5N DHD6N DHD7N	L23 K23 J23 H23 G23 F23 E23 D23	Channel D port H in-phase output data
DHOR DHORN	C24 C23	Channel D port H out-of-range bit
DDR DDRN	M24 M23	Channel D output clock
SPI signals		
csn	AC16	Chip Select (Active low)
sclk	AD16	SPI Clock
mosi	AD17	Master Out Slave In SPI Input
miso	AC17	Master In Slave Out SPI Output

Table 9-1. Pinout Table (Continued)

Pin Label	Pin Number	Description
Other signals		
rstn	AC15	
scan0 scan1 scan2	AD14 AC14 AD15	Scan mode signals Pull up to VCC
SYNCN SYNCP	AC11 AD11	Synchronization signal
Res50 Res62	AD18 AC18	50Ω and 62Ω reference resistor input
CMIRefAB CMIRefCD	B12 B13	Output reference for channel A-B and C-D Input Common mode
DiodA DiodC	AD7 AC7	Temperature diode Anode and Cathode
trigp trign tdreadyp tdreadyn tdcop tdcon	AD10 AC10 AD8 AC8 AD9 AC9	Reserved pins LEAVE FLOATING

10. QUAD ADC Package Information EBGA 31 × 31

Figure 10-1. EBGA Package



DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	1.25	1.45	1.60
A1	0.50	0.60	0.70
D	30.80	31.00	31.20
D1		29.21 (BSC.)	
E	30.80	31.00	31.20
E1		29.21 (BSC.)	
b	0.70	0.80	0.90
A2	0.75	0.85	0.95
M		24	
N		380	
bbb			0.25
ddd			0.20
e		1.27 TYP.	
A4	0.15		
Q	1.1		
REF: JEDEC MS-034B VARIATION BAK-1			

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "M" REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE, AND SYMBOL "N" IS THE MAXIMUM ALLOWABLE NUMBER OF BALLS AFTER DEPOPULATING.
4. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C.
5. DIMENSION "ddd" IS MEASURED PARALLEL TO PRIMARY DATUM C.
6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. PACKAGE SURFACE SHALL BE Ni PLATED.
8. ENCAPSULANT SIZE MAY VARY WITH DIE SIZE.
9. SMALL ROUND DEPRESSION FOR PIN 1 IDENTIFICATION.
10. "A4" IS MEASURED AT THE EDGE OF ENCAPSULANT TO THE INNER EDGE OF BALL PAD.
11. DIMENSIONING AND TOLERANCING PER ASME Y14.5 1994
12. THIS DRAWING IS FOR QUALIFICATION PURPOSE ONLY.

11. Ordering Information

Table 11-1. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
EVX8AQ160TPY	EBGA380 RoHS	Ambient	Prototype	
EV8AQ160CTPY	EBGA380 RoHS	Commercial *C* grade $0°C < T_{amb} < 70°C$	Standard	
EV8AQ160TPY-EB	EBGA380 RoHS	Ambient	Prototype	Evaluation board

How to reach us

Home page: www.e2v.com

Sales Office:

Northern Europe

e2v ltd

106 Waterhouse Lane

Chelmsford

Essex CM1 2QU

England

Tel: +44 (0)1245 493493

Fax:: +44 (0)1245 492492

E-Mail: enquiries@e2v.com

Southern Europe

e2v sas

16 Burospace

F-91572 Bièvres

Cedex

France

Tel: +33 (0) 16019 5500

Fax: +33 (0) 16019 5529

E-Mail: enquiries-fr@e2v.com

Germany and Austria

e2v gmbh

Industriestraße 29

82194 Gröbenzell

Germany

Tel: +49 (0) 8142 41057-0

Fax:: +49 (0) 8142 284547

E-Mail: enquiries-de@e2v.com

Americas

e2v inc.

4 Westchester Plaza

Elmsford

NY 10523-1482

USA

Tel: +1 (914) 592 6050 or

1-800-342-5338,

Fax:: +1 (914) 592-5148

E-Mail: enquiries-na@e2v.com

Asia Pacific

e2v

Bank of China Tower

30th floor office 7

1 Garden Rd Central

Hong Kong

Tel: +852 2251 8227/8/9

Fax: +852 2251 8238

E-Mail: enquiries-hk@e2v.com

Product Contact:

e2v

Avenue de Rochepleine

BP 123 - 38521 Saint-Egrève Cedex

France

Tel: +33 (0)4 76 58 30 00

Hotline:

hotline-bdc@e2v.com