EV10AS150A

High Linearity ADC 10-bit 2.5 Gsps with 1:4 DMUX

5 GHz Full Power Bandwidth

Datasheet

Features

- ADC 10-bit Resolution
- Up to 2.5 Gsps Sampling Rate
- Selectable 1:4 or 1:2 Demultiplexed Digital LVDS Outputs
- True Single Core Architecture (No Calibration Required)
- External Interleaving Possible Via 3-Wire Serial Interface
  - Gain Adjust
  - Offset Adjust
  - Sampling Delay Adjust
- Full Scale Analog Input Voltage Span 500 mVpp
- 100Ω Differential Analog Input and Clock Input
- Differential Digital Outputs, LVDS Logic Compatibility
- Low Latency Pipeline Delay
- Test Mode for Output Data Registering (BIST)
- Power Supplies: 5.0V, 3.3V, 2.5V
- Power Management (Nap, Sleep Mode)
- EBGA317 (Enhanced Ball Grid Array) Package

Performance

- Single Tone Performance in 1st Nyquist (–1 dBFS)
  - ENOB = 7.7 bit, SFDR = –56 dBFS at 2.5 Gsps, Fin = 500 MHz
  - ENOB = 7.8 bit, SFDR = –58 dBFS at 2.5 Gsps, Fin = 1245 MHz
- Single Tone Performance in 2nd Nyquist (–3 dBFS):
  - ENOB = 7.8 bit, SFDR = –60 dBFS at 2.5 Gsps, Fin = 2495 MHz
- 5 GHz Full Power Input Bandwidth (–3 dB)
- ±0.5 dB Band Flatness from 10 MHz to 2.5 GHz
- Input VSWR = 1.25:1 from DC to 2.5 GHz
- Bit Error Rate: 10^{-12} at 2.5 Gsps
- No Missing Codes at 2.5 Gsps, 1st and 2nd Nyquist

Screening

- Temperature Range
  - Commercial “C” Grade: Tamb > 0°C ; T_J < 90°C
  - Industrial “V” Grade: Tamb > –40°C ; T_J < 110°C

Visit our website: www.e2v.com
for the latest version of the datasheet

Applications

- **Direct Broadband RF Down Conversion**
- **Wide Band Communications Receiver**
- **High Speed Instrumentation**
- **High Speed Data Acquisition Systems**

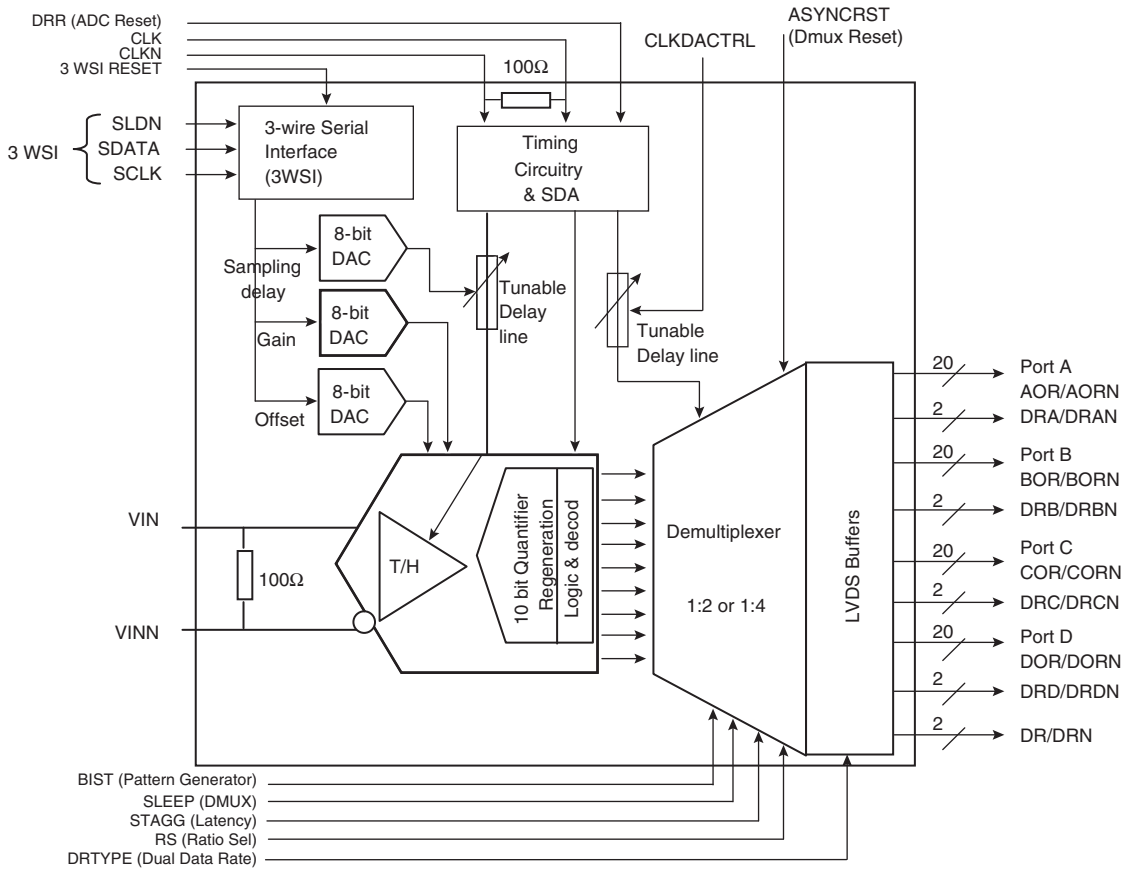
1. Block Diagram

The EV10AS150A combines a 10-bit 2.5 Gsps fully bipolar analog-to-digital converter chip, driving a fully bipolar DMUX chip with selectable Demultiplexing ratio (1:2) or (1:4). The 5 GHz full power input bandwidth of the ADC allows the direct digitization of up to 1 GHz broadband signals in the high IF region, in either L_Band or S_Band. The EV10AS150A features 7.8 effective bit and close to –58 dBFS spurious level at 2.5 Gsps over the full 1st Nyquist for large signals close to ADC Full Scale (–1 dBFS), and 8.1 bit ENOB at –6 dBFS in the 2nd Nyquist zone.

The 1:4 demultiplexed digital outputs are LVDS logic compatible, which allows easy interface with standard FPGAs or DSPs. The EV10AS150A operates at up to 2.5 Gsps in DMUX 1:4 and up to 2.0 Gsps in 1:2 DMUX ratio (The speed limitation with 1:2 DMUX ratio is mainly dictated by external data flow exchange capability at 2 × 1 Gsps with available FPGAs).

The EV10AS150A ADC+DMUX combo device is packaged in a 25 × 35 mm Enhanced Ball Grid Array EBGA317. This Package is based on multiple layers which allows the design of low impedance continuous ground and power supplies planes, and the design of 50Ω controlled impedance lines (100Ω differential impedance). This package has the same Thermal Coefficient of Expansion (TCE) as FR4 application boards, thus featuring excellent long term reliability when submitted to repeated thermal cycles.

Figure 1-1. Functional Block Diagram



2. Specifications

This section describes the device specifications in terms of:

- Absolute max ratings
- Recommended conditions of use
- Electrical operating characteristics
- Timings

2.1 Absolute Maximum Ratings

Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability.

Maximum ratings on I/Os are defined with device powered ON.

All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Table 2-1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Analog 5.0V Power Supply voltage	V_{CCA5}	GND to 6.0	V
Analog 3.3V Power Supply voltage	V_{CCA3}	GND to 3.6	V
Digital 3.3V Power Supply Voltage	V_{CCD}	GND to 3.6	V
Output 2.5V Power Supply voltage	V_{PLUSD}	GND to 3.0	V
Minimum Analog input peak voltage[1] (with differential input)	V_{IN} or V_{INN}	2.0	V
Maximum Analog input peak voltage[1] (with differential input)	V_{IN} or V_{INN}	4.0	V
Maximum difference between V_{IN} and V_{INN}[1] (with differential input)	$\lvert V_{IN} - V_{INN} \rvert$	2.0 (4 Vpp = +13 dBm in 100Ω)	V
Minimum Analog input peak voltage[2] (with single ended input)	V_{IN} with V_{INN} = 50Ω to GND or V_{INN} with V_{IN} = 50Ω to GND	2.0	V
Maximum Analog input peak voltage[2] (with single ended input)	V_{IN} with V_{INN} = 50Ω to GND or V_{INN} with V_{IN} = 50Ω to GND	4.0	V
Maximum amplitude on V_{IN} or V_{INN}[2] (with single ended input)	$\lvert V_{IN} \rvert$ or $\lvert V_{INN} \rvert$	(2 Vpp = +10 dBm in 50Ω)	V
Minimum Clock input peak voltage (with differential clock)	V_{CLK} or V_{CLKN}	1.5	V
Maximum Clock input peak voltage (with differential clock)	V_{CLK} or V_{CLKN}	4.0	V
Maximum difference between V_{CLK} and V_{CLKN} (with differential clock)	$\lvert V_{CLK} - V_{CLKN} \rvert$	1.5 (3 Vpp)	V
3WSI input voltage	SDATA, SLDN, SCLK, RESET	–0.3 to V_{CCA3} + 0.3	V

Table 2-1. Absolute Maximum Ratings (Continued)

Parameter	Symbol	Value	Unit
ADC Reset Voltage	DRR	–0.3 to V_{CCA3} + 0.3	V
DMUX function input voltage	RS, DRTYPE, SLEEP, STAGG, BIST	–0.3 to V_{CCD} + 0.3	V
DMUX Asynchronous Reset	ASYNCRST	–0.3 to V_{CCD} + 0.3	V
DMUX Control Voltage	CLKDACTRL	–0.3 to V_{CCD} + 0.3	V
Maximum input voltage on DIODE	DIODE ADC	700	mV
Maximum input current on DIODE	DIODE ADC	1	mA
Max Junction Temperature	T_J	135	°C
Storage temperature	Tstg	–55 to 150	°C
ESD protection (HBM)		≥ 500 on ADC inputs 500 on DMUX outputs	V

Notes: 1. See Section 2.1.1.
2. See Section 2.1.2.

2.1.1 Analog Input Max Ratings in differential configuration

Internal DC Common mode bias for differential analog inputs is: +3V.

Input impedance on V_{IN} and V_{INN} is: 55Ω // 550Ω = 50Ω

Max rating is ±1V = 2 Vpp on each single ended input, corresponding to 4 Vpp in differential.

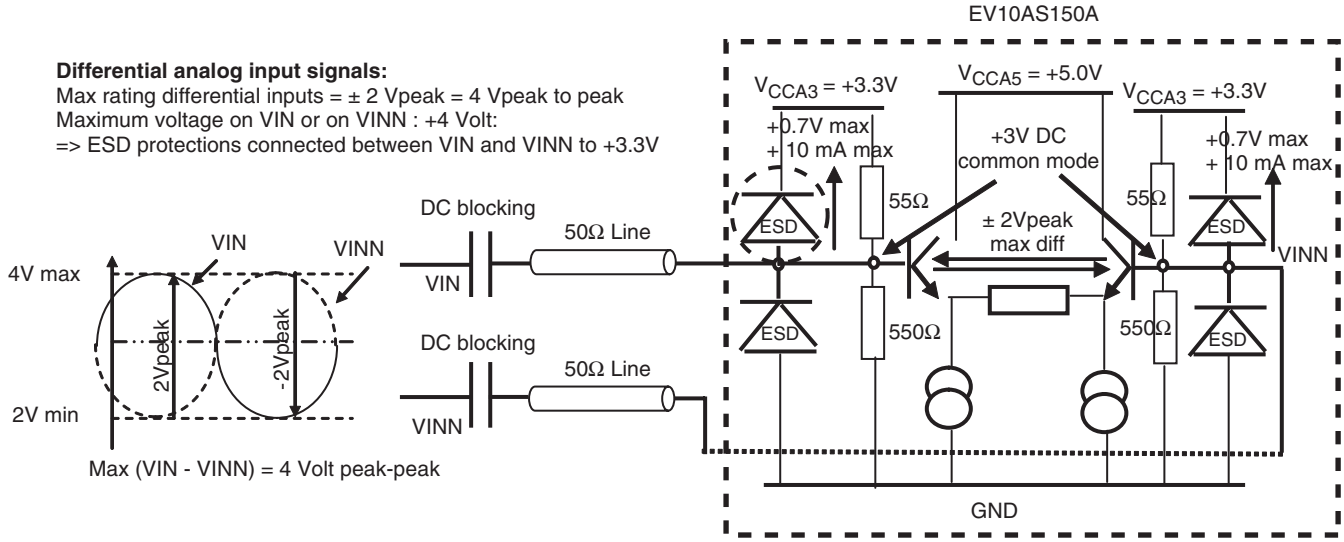
Vinput max = 3V + 1V = 4V

Vinput min = 3V – 1V = 2V

With V_{IN} = +4V and V_{INN} = +2V => $V_{IN} – V_{INN}$ = +2V

With V_{INN} = +4V and V_{IN} = +2V => $V_{IN} – V_{INN}$ = –2V

Figure 2-1. Analog Input Max Ratings in Differential Configuration



2.1.2 Analog Input Max Ratings in Single Ended Configuration

Internal DC common mode bias for differential analog inputs is +3V.

Input impedance on V_{IN} (and V_{INN}) is: 55Ω // 550Ω = 50Ω

Max rating is ±1V on one single ended signal, corresponding to 2 Vpp on 50Ω

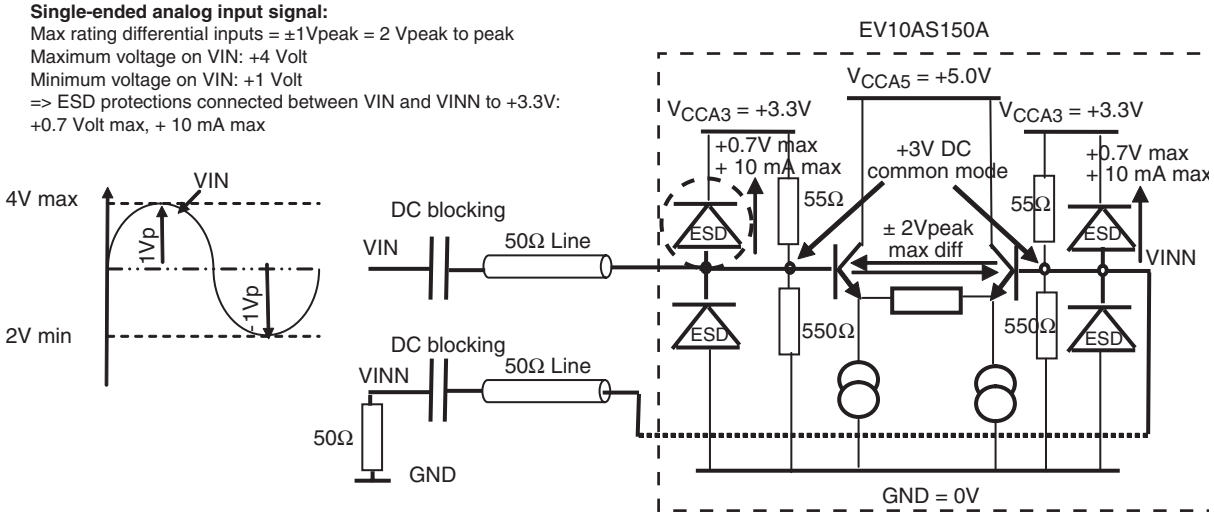
Limiting parameter for maximum rating is not $V_{IN} – V_{INN}$ differential input voltage but V_{IN} peak voltage value which shall not exceed +4V to avoid turning on the ESD protection tied to V_{CCA3} = +3.3V.

Vinput max = 3V (CM) + 1V (ESD) = 4V (If +4 Vp is applied, the ESD protections becomes forward biased: (+4V – 3.3V = +0.7V).

Vinput min = 3V – 1V = 2V

The ESD diode can sustain up to 10 mA forward biasing without damage, but incoming signal will be clipped at +4V = +3V (internal DC common mode) + 1V.

Figure 2-2. Analog Input Max Ratings in Single Ended Configuration



2.2 Recommended Conditions of Use

Table 2-2. Recommended Conditions of Use

Parameter	Symbol	Comments	Recommended	Unit
Power supplies				
Analog 3.3V Power Supply voltage	V_{CCA3}	No specific power supply sequencing required during power ON / OFF	3.3	V
Analog 5.0V Power Supply voltage	V_{CCA5}		5.0	V
Digital 3.3V Power Supply voltage	V_{CCD}		3.3	V
Output 2.5V Power Supply voltage	V_{PLUSD}		2.5	V
Analog Input				
Recommended Configuration			Differential Analog input	
Clock Input				
Recommended Configuration			Differential Clock input	
Clock input power level	P_{CLK} P_{CLKN}	100Ω differential clock	+1 dBm / 50Ω (1Vpp in 100Ω)	dBm
External clock Duty cycle	DCYC		50	%
Control functions input level				
ADC 3WSI Inputs	SDATA, SLDN, SCLK, RESET		0 to V_{CCA3}	V
ADC Reset	DRR		0 to V_{CCA3}	V
DMUX Control Inputs	SLEEP, STAGG, ASYNCRST, BIST, RS, DRTYPE, CLKDACTRL		0 to V_{CCD}	V
Operating Temperature Range	T_{amb}; T_J	Commercial “C” grade Industrial “V” grade	Tamb > 0°C; T_J < 90°C Tamb > –40°C; T_J < 110°C	°C

Table 2-3. Recommended Configuration for Optimum Dynamic Performances

3WSI Register	Recommended value	comment
State register	SDA OFF	For optimum SNR in 2nd Nyquist zone if not used in interleaving mode
Clock duty Cycle adjust register D4….D0	35/65%	For optimum SFDR and THD at high sampling rate in 2nd Nyquist zone.
Clock adjust register D4 … D0	+30 ps	For optimum SFDR and THD in 2nd Nyquist
Gain adjust D7...D0	Gain min to typ	For optimum SNR and SFDR

2.3 Electrical Characteristics for Supplies, Inputs and Outputs

Unless otherwise specified:

Values are given over temperature and power supplies range.

Table 2-4. Electrical Characteristics for Supplies, Inputs and Outputs

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Power requirements						
Power Supply voltages Analog 5.0V Analog 3.3V Digital 3.3V Output 2.5V	 1	 V_{CCA5} V_{CCA3} V_{CCD} V_{PLUSD}	 4.75 3.15 3.15 2.4	 5.0 3.3 3.3 2.5	 5.15 3.45 3.45 2.6	 V V V V
Power Supply current in 1:2 DMUX Analog V_{CCA5}= 5.0V Analog V_{CCA3} = 3.3V Digital V_{CCD} = 3.3V Output V_{PLUSD} = 2.5V	 1	 I_{VCCA5} I_{VCCA3} I_{VCCD} I_{VPLUSD}		 160 840 400 420	 205 990 500 580	 mA mA mA mA
Power Supply current in 1:4 DMUX Analog V_{CCA5}= 5.0V Analog V_{CCA3} = 3.3V Digital V_{CCD} = 3.3V Output V_{PLUSD} = 2.5V	 1	 I_{VCCA5} I_{VCCA3} I_{VCCD} I_{VPLUSD}		 160 840 450 450	 205 990 575 620	 mA mA mA mA
Power Supply current in NAP and SLEEP mode Analog V_{CCA5}= 5.0V Analog V_{CCA3} = 3.3V Digital V_{CCD} = 3.3V Output V_{PLUSD} = 2.5V	 1	 I_{VCCA5} I_{VCCA3} I_{VCCD} I_{VPLUSD}		 140 590 145 390	 180 880 170 535	 mA mA mA mA
Power dissipation - 1:2 DMUX - 1:4 DMUX - NAP & SLEEP mode (1:4 or 1:2)	 1	 P_D		 5.9 6.2 4.2	 7.7 8.1 5.9	 W W W
Analog inputs						
Common mode compatibility for analog inputs			External AC coupling			
Analog inputs common voltage (internal)	4	V_{CM}		3.0		V
Full-Scale input Voltage Range Differential mode	1	V_{IN} V_{INN}	–125 –125		125 125	mV
Full-Scale input Voltage Range Single ended mode with other input connected to ground through 50Ω resistors	1	V_{IN} or V_{INN}	–250		250	mV
Analog Input power Level (in 100Ω differential termination)	1	 $P_{IN, INN}$		–5 0.5		dBm Vpp
Analog Input power Level (in 50Ω single ended termination)	4	P_{IN} or P_{INN}		–2		dBm
Analog input capacitance (die)	4	C_{IN}		0.3		pF
Input leakage current	4	I_{IN}		10		µA

Table 2-4. Electrical Characteristics for Supplies, Inputs and Outputs (Continued)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Input resistance - Single-ended - Differential	4	 R_{IN} $R_{IN, INN}$	 47 94	 50 100	 53 106	 Ω Ω
Clock inputs						
Logic common mode compatibility for clock inputs	4		Low phase noise sinewave at 2.5 GHz (> 155 dBc/Hz) or low jitter LVDS/LVPECL (<100 fs rms)			
ADC intrinsic clock jitter[1]	4			120		fs rms
Clock inputs internal DC common mode voltage	4	V_{CM}		3.0		V
Clock input voltage on each single ended input (2.5 GHz sinewave)	4	V_{CLK} or V_{CLKN}	±0.158	±0.25	±0.5	V
Clock input voltage into 100Ω differential clock input (2.5 GHz sinewave)	4	$\lvert V_{CLK} - V_{CLKN} \rvert$	0.632	1	2	Vpp
Clock input power level (2.5 GHz low phase noise sinewave input) in 50Ω	4	$P_{CLK, CLKN}$	–3	+1	+7	dBm
Sinewave or Square wave Clock signal (minimum) slew-rate	4	$SR_{CLK, CLKN}$	5	8		GV/s
Square Wave differential Clock input voltage on 100Ω input (LVDS & LVPECL compatible)	4	VSQ $_{CLK-CLKN}$	0.25	0.8	2	Vpp
Clock input capacitance (die)	4	C_{CLK}		0.3		pF
Clock input Resistance - Single-ended - Differential	4	 R_{CLK} $R_{CLK, CLKN}$	 47 94	 50 100	 53 106	 Ω Ω
Digital Data Outputs						
Logic compatibility			LVDS			
50Ω transmission lines, 100Ω (2 × 50Ω) differential termination - Logic low - Logic high - Differential output - Common mode	1	 VOL VOH VODIFF VOCM	 1.25 250 1.125	 1.075 1.375 350 1.25	 1.25 450 1.375	 V V mV V
Control Function Inputs						
ASYNCRST (DEMUX Reset) input voltages and currents - Logic Low - Logic High (reset mode)	1	 V_{IL} I_{IL} V_{IH} I_{IH}	 0 –300 1.8	 	 1.4 V_{CCD} 50	 V µA V µA
DRR (ADC reset) [2] Logic low Logic high Threshold	4	 V_{IL} V_{IH} V_{TH}	 0 1.5 	 1.4	 1.1 V_{CCA3} 	 V V V

Table 2-4. Electrical Characteristics for Supplies, Inputs and Outputs (Continued)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
RS, BIST, STAGG, SLEEP, DRTYPE (Control Input Voltages)						
- Logic low[3]						
Resistor to ground		R_{IL}	0		10	Ω
Voltage level		V_{IL}			0.5	V
Input low current	1	I_{IL}	–500			µA
- Logic high[3]						
Resistor to ground		R_{IH}	10k		Infinite	Ω
Voltage level		V_{IH}	2.0			V
Input high current		I_{IH}			10	µA
SDATA, SLDN, SCLK, RESET						
Logic low	4	V_{IL}	0		1.0	V
Logic high		V_{IH}	2.3		V_{CCA3}	V
CLKDACTRL input voltage	4		$1/3 \times V_{CCD}$		$2/3 \times V_{CCD}$	V

Notes: 1. Measured with SDA OFF(ADC Jitter = 120 fs rms). ADC Jitter with SDA = ON is 150 fs rms, and 170 fs rms with SDA = ON and fully tuned.
2. DRR logic programmable with 3WSI interface. Default value is DRR active low.
3. See Section 4.4 on page 35 for control signal settings.

2.4 Converter Characteristics

Unless otherwise specified:

Recommended conditions of use (refer to Table 2-2 and Table 2-3 on page 6). Values are given at ambient temperature (T_J ~ 65°C) and hot temperature.

Table 2-5. DC Converter Characteristics

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
DC Accuracy						
Resolution	1	N		10		bit
DNLrms[1]	1	DNLrms		0.2		LSB
Differential non-linearity [1]	1	DNL+		0.6		LSB
Differential non-linearity[1])	1	DNL-	–0.8	0.5		LSB
Integral non-linearity[1]	1	INL-		–1.8		LSB
Integral non-linearity[1]	1	INL+		1.8		LSB
Gain center value[2]	1	G	0.95	1	1.05	
Gain error drift	4	G(T)		50		ppm/°C
Input offset voltage[3]	1	OFFSET	–20		20	mV

Notes: 1. Histogram testing at Fs = 2.5 Gsps Fin = 1.5 GHz
–0.8 LSB peak value for DNL points out that there are no missing codes up to maximum operating sampling rate (2.5 Gsps).
DNLrms is the deviation from ideal ADC rms quantification noise. For reference, a DNL of 0.2 lsb rms has the same order of magnitude as the 10 Bit rms quantification noise under 0.5V Full Scale: 1 lsb/SQRT(12) = 1 LSB / 3.46 = 0.288 lsb rms.

2. ADC gain with programmed default value.
   This ADC Gain can be fine tuned to “1” by monitoring of the gain adjust function through the 3WSI serial interface.
3. ADC offset with programmed default values.
   The ADC Offset can be compensated through the 3WSI up to ± 20 mV by an 8 Bit embedded control DAC: Resolution: 40 mV/256 = 156 µV (See 3WSI table in Section 4.5.3 ”3WSI Register Description” on page 43).

Table 2-6. Dynamic Converter Characteristics

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
AC Characteristics						
Full Power Input Bandwidth (–3 dB)	4	FPBW	5			GHz
Gain Flatness (10 MHz-1.25 GHz) • Systematic roll-off • AC gain variation Gain Flatness (1.25 GHz-2.5 GHz) • Systematic roll-off • AC gain variation Gain Flatness (2.5 GHz-3.75 GHz) • Systematic roll-off • AC gain variation	4	GF		 –0.5 ±0.1 –0.5 ±0.2 –1.0 ±0.3		dB
Input Voltage Standing Wave Ratio (DC – 2.5 GHz) (DC – 5 GHz)	4	VSWR		 1.25:1 1.50:1		

Table 2-7. Dynamic Converter Characteristics with Differential Analog Input

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
AC Performance with differential analog input						
Ain= –1 dBFS, +1 dBm differential clock (1 Vpp in 100Ω), 50% external duty cycle, Binary output mode						
Signal to Noise and Distortion Ratio Fs = 2.5 Gsps Fin = 500 MHz Fs = 2.5 Gsps Fin = 1245 MHz Fs = 2.5 Gsps Fin = 2495 MHz	 4 4 1	SINAD	 45.0 45.0 45.0	 48.0 48.5 48.0		dBFS
Effective Number of Bits Fs = 2.5 Gsps Fin = 500 MHz Fs = 2.5 Gsps Fin = 1245 MHz Fs = 2.5 Gsps Fin = 2495 MHz	 4 4 1	ENOB	 7.2 7.3 7.3	 7.7 7.8 7.7		Bits
Signal to Noise Ratio Fs = 2.5 Gsps Fin = 500 MHz Fs = 2.5 Gsps Fin = 1245 MHz Fs = 2.5 Gsps Fin = 2495 MHz	 4 4 1	SNR	 48.0 47.0 46.0	 51.0 50.0 49.0		dBFS

Table 2-7. Dynamic Converter Characteristics with Differential Analog Input (Continued)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Total Harmonic Distortion (10 harmonics) Fs = 2.5 Gsps Fin = 500 MHz Fs = 2.5 Gsps Fin = 1245 MHz Fs = 2.5 Gsps Fin = 2495 MHz	 4 4 1	|THD|	 47.0 50.0 50.0	 51.0 54.0 54.0		dBFS
Spurious Free Dynamic Range Fs = 2.5 Gsps Fin = 500 MHz Fs = 2.5 Gsps Fin = 1245 MHz Fs = 2.5 Gsps Fin = 2495 MHz	 4 4 1	|SFDR|	 50.0 52.0 52.0	 56.0 58.0 59.0		dBFS
Two-Tone 3rd order Intermodulation distortion IMD3 (–): (2f1-f2, 2f2-f1) at –7 dBFS each tone, Fs = 2.5Gsps Fin1 = 790 MHz, Fin2 = 800 MHz Fin1 = 1550 MHz, Fin2 = 1560 MHz Fin1 = 2500 MHz, Fin2 = 2510 MHz	4	IMD3(–)	 52.0 52.0 54.0	 58.0 58.0 60.0		dBc
Signal independent Spurious level (Fclk/4 with 1:4 DMUX Ratio) (–1 dBFS Analog Input) Differential driven analog input (100Ω) (ADC full scale input power: –5 dBm) (0.5Vpp in 100Ω Differential analog input)	4	Fclk/4		 –78 –83	 –75 –80	 dBFS dBm
Ain = –3 dBFS, Differential or single ended analog input, + 1 dBm differential clock (1 Vpp in 100Ω), 50% external duty cycle, Binary output mode						
Signal to Noise and Distortion Ratio Fs = 2.5 Gsps Fin = 500 MHz Fs = 2.5 Gsps Fin = 1245 MHz Fs = 2.5 Gsps Fin = 2495 MHz	 4 4 1	SINAD	 46.0 46.0 45.0	 49.0 49.0 48.5		dBFS
Effective Number of Bits Fs = 2.5 Gsps Fin = 500 MHz Fs = 2.5 Gsps Fin = 1245 MHz Fs = 2.5 Gsps Fin = 2495 MHz	 4 4 1	ENOB	 7.4 7.4 7.3	 7.9 7.9 7.8		Bits
Signal to Noise Ratio Fs = 2.5 Gsps Fin = 500 MHz Fs = 2.5 Gsps Fin = 1245 MHz Fs = 2.5 Gsps Fin = 2495 MHz	 4 4 1	SNR	 49.0 47.0 47.0	 51.5 51.0 50.0		dBFS
Total Harmonic Distortion (10 harmonics) Fs = 2.5 Gsps Fin = 500 MHz Fs = 2.5 Gsps Fin = 1245 MHz Fs = 2.5 Gsps Fin = 2495 MHz	 4 4 1	|THD|	 48.0 51.0 51.0	 53.0 54.0 54.0		dBFS
Spurious Free Dynamic Range Fs = 2.5 Gsps Fin = 500 MHz Fs = 2.5 Gsps Fin = 1245 MHz Fs = 2.5 Gsps Fin = 2495 MHz	 4 4 1	|SFDR|	 52.0 53.0 53.0	 59.0 60.0 60.0		dBFS

Table 2-7. Dynamic Converter Characteristics with Differential Analog Input (Continued)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Ain = –13 dBFS, Differential or single ended analog input, +1 dBm differential clock (1 Vpp in 100Ω), 50% external duty cycle, Binary output mode						
Signal to Noise and Distortion Ratio						
Fs = 2.5 Gsps Fin = 500 MHz	4	SINAD	47.0	50.0		dBFS
Fs = 2.5 Gsps Fin = 1245 MHz	4		47.0	50.5		
Fs = 2.5 Gsps Fin = 2495 MHz	4		47.0	50.5		
Effective Number of Bits						
Fs = 2.5 Gsps Fin = 500 MHz	4	ENOB	7.5	8.0		Bits
Fs = 2.5 Gsps Fin = 1245 MHz	4		7.6	8.1		
Fs = 2.5 Gsps Fin = 2495 MHz	4		7.6	8.1		
Signal to Noise Ratio						
Fs = 2.5 Gsps Fin = 500 MHz	4	SNR	51.0	53.0		dBFS
Fs = 2.5 Gsps Fin = 1245 MHz	4		50.0	53.0		
Fs = 2.5 Gsps Fin = 2495 MHz	4		49.0	53.0		
Total Harmonic Distortion (10 harmonics)						
Fs = 2.5 Gsps Fin = 500 MHz	4	|THD|	48.0	53.0		dBFS
Fs = 2.5 Gsps Fin = 1245 MHz	4		50.0	54.0		
Fs = 2.5 Gsps Fin = 2495 MHz	4		50.0	54.0		
Spurious Free Dynamic Range						
Fs = 2.5 Gsps Fin = 500 MHz	4	|SFDR|	51.0	56.0		dBFS
Fs = 2.5 Gsps Fin = 1245 MHz	4		52.0	57.0		
Fs = 2.5 Gsps Fin = 2495 MHz	4		52.0	57.0		

Table 2-8. Dynamic Converter Characteristics with Single Ended Analog Input

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
AC Performance with single ended analog input						
Ain = –1dBFS, +1 dBm differential clock (1Vpp in 100Ω), 50% external duty cycle, Binary output mode						
Signal to Noise and Distortion Ratio						
Fs = 2.5 Gsps Fin = 500 MHz	4	SINAD	44.0	47.5		dBFS
Fs = 2.5 Gsps Fin = 1245 MHz	4		44.0	47.5		
Fs = 2.5 Gsps Fin = 2495 MHz	4		44.0	47.0		
Effective Number of Bits						
Fs = 2.5 Gsps Fin = 500 MHz	4	ENOB	7.2	7.6		Bits
Fs = 2.5 Gsps Fin = 1245 MHz	4		7.2	7.6		
Fs = 2.5 Gsps Fin = 2495 MHz	4		7.2	7.5		
Signal to Noise Ratio						
Fs = 2.5 Gsps Fin = 500 MHz	4	SNR	47.0	51.0		dBFS
Fs = 2.5 Gsps Fin = 1245 MHz	4		47.0	49.0		
Fs = 2.5 Gsps Fin = 2495 MHz	4		47.0	49.0		
Total Harmonic Distortion (10 harmonics)						
Fs = 2.5 Gsps Fin = 500 MHz	4	|THD|	46.0	50.0		dBFS
Fs = 2.5 Gsps Fin = 1245 MHz	4		49.0	53.0		
Fs = 2.5 Gsps Fin = 2495 MHz	4		48.0	51.0		

Table 2-8. Dynamic Converter Characteristics with Single Ended Analog Input (Continued)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Spurious Free Dynamic Range Fs = 2.5 Gsps Fin = 500 MHz Fs = 2.5 Gsps Fin = 1245 MHz Fs = 2.5 Gsps Fin = 2495 MHz	 4 4 4	|SFDR|	 50.0 51.0 50.0	 55.0 57.0 54.0		dBFS
Two-Tone 3rd order Intermodulation distortion IMD3 (–): (2f1-f2, 2f2-f1) at –7 dBFS each tone, Fs = 2.5Gsps Fin1 = 790 MHz, Fin2 = 800 MHz Fin1 = 1550 MHz, Fin2 = 1560 MHz Fin1 = 2500 MHz, Fin2 = 2510 MHz	4	IMD3(–)	 52.0 52.0 54.0	 58.0 58.0 60.0		dBc
Signal independent spurious level (Fclk/4 with 1:4 DMUX Ratio) (–1 dBFS Analog Input) Single-ended driven analog input (50Ω) (ADC full scale input power: –2 dBm)	4	Fclk/4		 –72 –74	 –69 –71	 dBFS dBm
Ain = – 3 dBFS, +1 dBm differential clock (1 Vpp in 100Ω at 2.5 GHz), 50% external duty cycle, Binary output mode -> Refer to Table 2-7 on page 10 (same performance with single ended or differential analog input with –3 dBFS input level)						
Ain = –13 dBFS, +1 dBm differential clock (1 Vpp in 100Ω at 2.5 GHz), 50% external duty cycle, Binary output mode -> Refer to Table 2-7 (same performance with single ended or differential analog input with –13 dBFS input level)						

2.5 Transient and Switching Characteristics

Table 2-9. Transient Characteristics

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
TRANSIENT PERFORMANCE						
Bit Error Rate(1)	4	BER		10^{-12}		Error/sample
ADC settling time (± 2%)	4	TS			350	ps
Overvoltage recovery time	4	ORT			400	ps
ADC step response Rise/Fall Time (10–90%)	4			80	100	ps

Note: 1. Measured with SDA OFF
ADC Bit Error Rate is related to internal regeneration latches indecision (for analog inputs very close to latches threshold), which may produce large amplitude output errors.
The probability of error is measured at 2.5 Gsps maximum operating frequency.

Table 2-10. Switching characteristics

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Switching Performance and Characteristics						
Maximum Clock Frequency DRTYPE = DR/2, 1:2 mode DRTYPE = DR, 1:2 mode DRTYPE = DR/2 1:4 mode DRTYPE = DR 1:4 mode	 4 4 1 1	Fs MAX	 2.0 2.0 2.5 2.5			Gsps
Minimum clock frequency	4	Fs MIN			500	Msps

Table 2-10. Switching characteristics (Continued)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Minimum Clock pulse width (High)	4	TC1	0.2		1.0	ns
Minimum Clock pulse width (Low)	4	TC2	0.2		1.0	ns
External clock Duty cycle(1)	4	DCYC	45	50	55	%
Aperture Delay(2)	4	TA	300	350	400	ps
Aperture Jitter added by the ADC(2)	4	Jitter		120		fs rms
Output Rise/Fall time for Data (20% – 80%)(3))	4	TR/TF		120/120	180/180	ps
Output Rise/Fall time for Output Clock (20% – 80%)(3)	4	TR/TF		120/120	180/180	ps
Digital Data Output propagation delay	4	TOD		2.3		ns
Data Ready Clock Output propagation delay	4	TDR		2.3		ns
Differential propagation delay (Output Data vs. Data clock)	4	TOD – TDR	0	150	200	ps
Tskew (40 digital output data)	4	Tskew		± 15	± 25	ps
Output Data Pipeline delay (Latency) Synchronized 1:2 mode on Port A Synchronized 1:2 mode on Port B Synchronized 1:4 mode on Port A Synchronized 1:4 mode on Port B Synchronized 1:4 mode on Port C Synchronized 1:4 mode on Port D Staggered 1:2 mode or 1:4 mode	4	PD		 5.5 4.5 7.5 6.5 5.5 4.5 4.5		Clock Cycles
ASYNCRST minimum pulse width	5	RSTPW		3		ns
DRR minimum pulse width	5	DRRPW		3.5		ns

Notes: 1. ADC performance are given for optimum value of 50% external clock duty cycle.
2. ADC Aperture delay and Aperture jitter measured with SDA = OFF. (Default setting at Reset).
3. Rise time and fall time are defined for 100Ω differentially terminated output load with 2nH and 2 pF termination parasitics.

2.6 Timing Diagram

2.6.1 Aperture Delay

The analog input is sampled on the rising edge of the differential clock input (CLK, CLKN) after TA (aperture delay) of +350 ps typical. Aperture delay (TA) is measured at package input balls with the assumption that the external trace length of analog input and clock input are well matched (6.6 ps/mm of mismatch with $\varepsilon_r = 4$).

2.6.2 Latency (Simultaneous Mode and Staggered Mode)

In simultaneous output mode with 1:4 DMUX Ratio, the digitized digital output data N, N+1,N+2, N+3 respectively on port A, B, C and D are aligned (on the latest data available N+3 on port D). The data N on port A is available after 7.5 Clock cycles pipeline delay, plus an additional propagation delay TOD (due to Output Buffers + Package propagation delay). Due to data alignment, the pipeline delay is decreased of one clock cycle for each port from port A to D leading to:

- 7.5 clock cycles for port A
- 6.5 clock cycles for port B
- 5.5 clock cycles for port C
- 4.5 clock cycles for port D

In simultaneous output mode with 1:2 DMUX ratio, the latency becomes respectively 5.5 and 4.5 Clock cycles on port A and port B, with same TOD propagation delay.

In staggered output mode, the latency of the 4 Digital output ports A,B,C,D is the same, since data are presented on output port as soon as available.

In staggered mode for 1:4 DMUX ratio and 1:2 DMUX ratio latency is only 4.5 Clock cycles for port A, B, C and D (see Timing Diagram).
The output propagation delays TOD1, TOD2, TOD3, and TOD4 of the 4 outputs ports in staggered mode can be considered as identical to TOD.

2.6.3 Data Ready Positioning Versus Output Data (DR/2 Mode and DR Mode)

The Data Ready output clock signal (DR, DRN) is synchronized with ADC (CLK, CLKN) differential clock falling edges to be synchronous with Digital output data (since digital data are output on falling edge of sampling Clock after a latency of 7.5 Clock cycles).

In 1:4 DMUX Ratio, the (DR, DRN) signal is shifted by 2 clock cycles in order to be located at center of data pulse.

In 1:2 DMUX Ratio, the (DR, DRN) signal is shifted by 1 clock cycle to be located at center of data pulse.

Furthermore, the output propagation delay (TDR) of the Data Ready signal and the output propagation delay of the digital data (TOD) are matching very closely, and track each other over full operating temperature range.

Therefore the Data signals and Data clock signals are synchronized at Package output, with the differential Data Ready output clock pulse rising edge being centered within Data pulse, in either dual Data rate mode (DR/2) or DR mode.

In dual data rate (DR/2 mode), the Data clock switches at the same rate as the digital data, and therefore both the rising and falling edges of (DR, DRN) data clock are located at the center of the data pulse over temperature (with max TOD-TDR = 100 ps).

In DR mode, the Data clock switches at twice the rate of the digital data, with the differential Data Ready pulse rising edge being centered within Data pulse and differential falling edges being synchronous with Data transitions.

2.6.4 Differential Timing Values TOD-TDR Versus Absolute Timing Values TOD and TDR

The absolute values for TOD and TDR are given for information only, and are corresponding to the digital output data propagation delay and to the Data Ready output propagation delay, related to ADC output buffers throughput delay and package propagation times.

TOD and TDR are measured at Package I/Os level, (Input/Outputs Balls), taking out the board extra propagation delays of the 50Ω/100Ω controlled impedance lines.

Assuming the application board trace lengths are matched for digital data and data ready lines (within skew limit), one has only to consider the time difference between differential digital data outputs and differential Data clock signals TOD-TDR in simultaneous mode.

In staggered mode, the differential delays are (TOD1-TDR1), (TOD2-TDR2), (TOD3-TDR3), (TOD4-TDR4). See Figure 2-4 on page 19.

Therefore the absolute delay values TOD and TDR are not actually of interest: only the time difference TOD-TDR has to be actually considered.

The measurement of the relative time difference is easy with matches probes, whereas absolute timings are very difficult to measure.

If the propagation time delays (trace lengths for digital data outputs and Data Ready outputs are well matched, together with ideal TOD = TDR, we shall measure ideally TOD-TDR = 0 at application board outputs (FPGA or DSP incoming signals).

2.6.5 Alignment Between Data Ready and Data Including Skew Management

Real TOD-TDR excluding skew between different data is ± 50 ps typical, and ± 100 ps max.

In simultaneous mode, one common Data Ready pulse (DR, DRN) is output for all 4 differential Output Ports A,B,C,D. Therefore the skews of the 4 differential data ports have to be as low as possible:
the skews of the 4 differential output ports due to ADC Package and internal ADC Buffers is less than ± 25 ps max (measured at Package output Balls).
The external skews due to track length differences of the external 100Ω controlled impedance lines), shall be kept as low as possible.
For example, (considering 3.3 ps/mm propagation time in vacuum), the signal propagation time in a different medium of dielectric constant ε_r = 4 (at 10 GHz), is yielding to SQRT(ε_r) × 3.3 ps/mm = 6.6 ps/mm: a 3 mm skew in length between the 40 differential data will result in a 3 mm × 6.6 ps/mm = ~ 20 ps skew, to be added to the ±25 ps skew due to the ADC (Package outputs).
The total skew (ADC + board) will be in this case 50 ps + 20 ps = 70 ps = ± 35 ps in actual skew at FPGA incomings.
Since TOD-TDR is ± 50 ps typical, and ± 100 ps max, TOD-TDR shall be added to the total data skew, (ADC and board), leading to:
(TOD-TDR) + Tskew(total) = (± 100 ps) + (± 35 ps) = (± 135 ps) maximum uncertainty on positioning of differential Data Ready signal rising edge (DR, DRN), pulse within Data pulse.

In staggered mode, the 4 (four) out-of-range bit function for the 4 (four) Ports A,B,C,D are respectively re-allocated to the Data Ready function, available for each output Port, since latency is different, namely:
Port A (AOR, AORN); Port B (BOR, BORN); Port C (COR, CORN); Port D (DOR, DORN)
is respectively replaced by: (DRA, DRAN), (DRB, DRBN), (DRC, DRCN), (DRD, DRDN).

The output propagation delays of the 4 Data Ready pulses (TDR1, TDR2, TDR3, TDR4) are identical to the TDR output propagation delay in simultaneous mode, and are matching the Digital Data propagation delays of the 4 Output Ports over temperature.
The relative differential timing values (TOD1-TDR1), (TOD2-TDR2), (TOD3-TDR3), (TOD4-TDR4) are identical to the TOD - TDR differential timing of the simultaneous mode. Skew for port A, B, C, D are considered for 10 bit data in staggered instead of 44 bit of data in simultaneous. Skew between 10 data is slightly better in staggered mode. To simplify calculation skew values of previous section shall be applied.

2.6.6 Minimum Available Time Width Between Data and Data Ready (TD1, TD2)

At 2.5 GHz sampling rate, the time difference between zero crossing point of change of differential data and differential Data Ready output clock rising edge (centered within data pulse) is defined by TD1. The time difference between differential data clock rising edge and next point of change of the differential data output is defined by TD2.

The order of magnitude of time difference TD1-TD2 is identical to TOD-TDR:

Except that TOD-TDR is frequency independent, whereas TD1 and TD2 are sampling frequency dependent:
For example at 1:4 DMUX ratio, the data pulse width at maximum operating frequency of 2.5 GHz is 4 × 400 ps = 1.6 ns. Assuming TOD = TDR, the rising edge of differential data clock is ideally located at center of data pulse, with TD1 = TD2 = 800 ps. With a maximum difference of TOD-TDR of ±100 ps over temperature, and a total of ± 50 ps output Data skew (ADC + Board), this is yielding to a minimum available time width for TD1 or TD2 pulses of: 800 ps – 150 ps = 650 ps (with 50/50 duty cycle).

2.6.7 Timing Diagram in Simultaneous and Staggered Mode

Figure 2-3. Timing Diagram Simultaneous mode, 1:4 DMUX Ratio

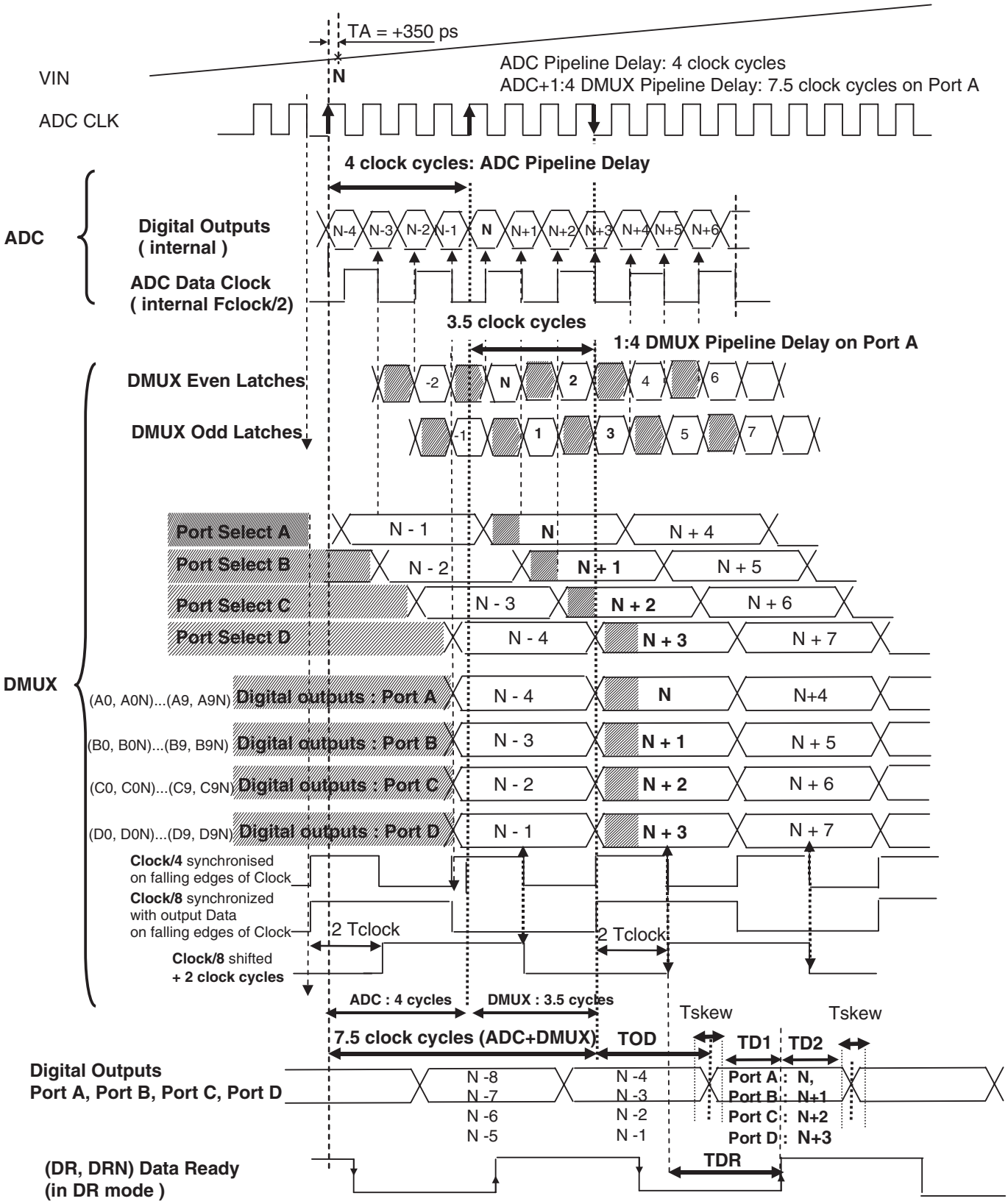
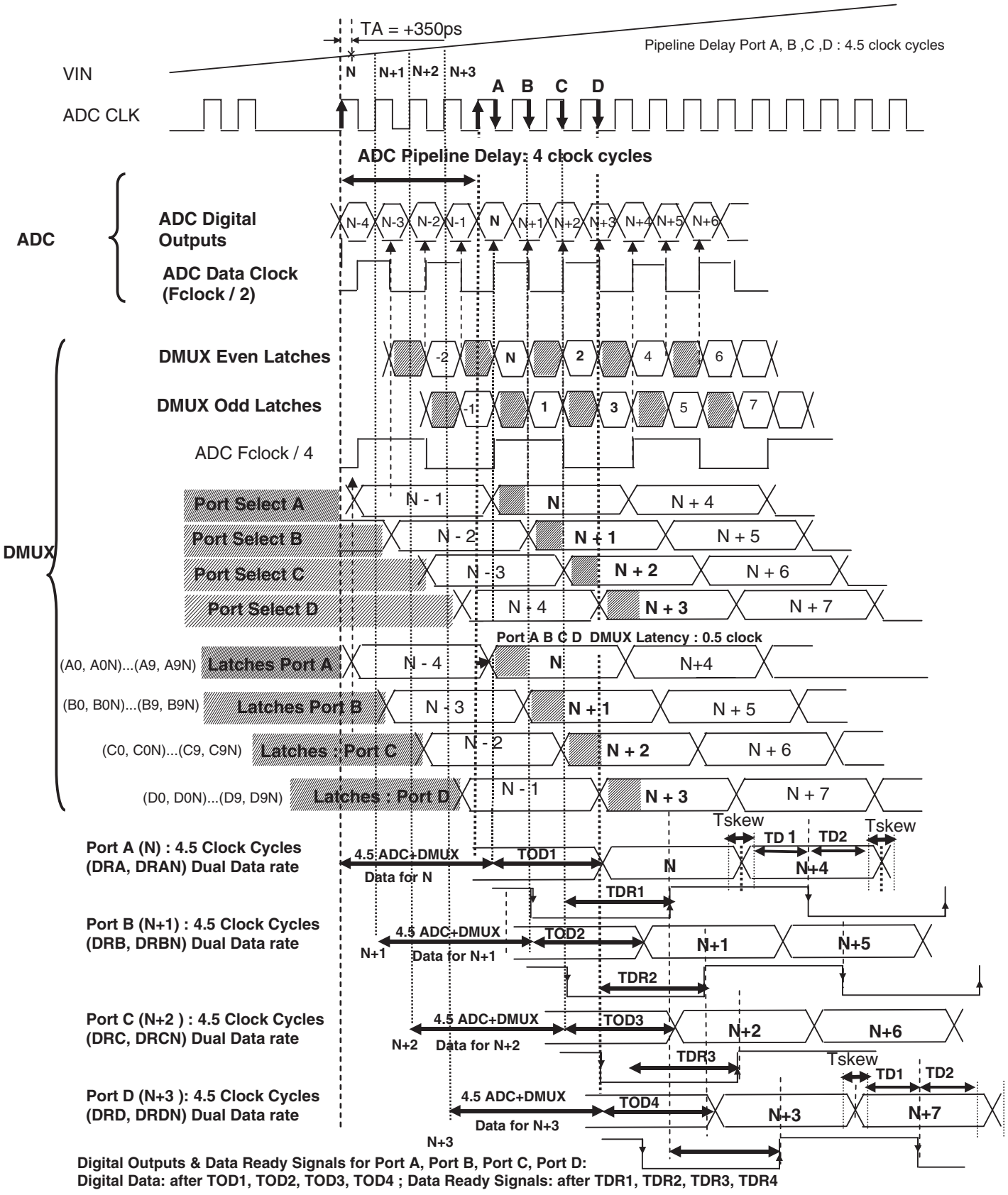


Figure 2-4. Timing Diagram Staggered mode, 1:4 DMUX Ratio



2.7 Digital Output Data Coding

Table 2-11. Digital Output Data Coding Table

Differential analog input	Voltage level	Digital output		
		Natural Binary[1] MSB……LSB OR	Binary 2's Complement[1] MSB……..LSB OR	GRAY Coding[1] MSB……..LSB OR
> 250.25 mV	>Top end of full scale + ½ LSB	1 1 1 1 1 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0 0 0 0 1
250.25 mV	Top end of full scale + ½ LSB	1 1 1 1 1 1 1 1 1 1 1 0	0 1 1 1 1 1 1 1 1 1 1 0	1 0 0 0 0 0 0 0 0 0 0 0
249.75 mV	Top end of full scale – ½ LSB	1 1 1 1 1 1 1 1 1 1 0 0	0 1 1 1 1 1 1 1 1 1 0 0	1 0 0 0 0 0 0 0 0 0 1 0
125.25 mV	$^3/_4$ full scale + ½ LSB	1 1 0 0 0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0 0 0 0 0	1 0 1 0 0 0 0 0 0 0 0 0
124.75 mV	$^3/_4$ full scale – ½ LSB	1 0 1 1 1 1 1 1 1 1 1 0	0 0 1 1 1 1 1 1 1 1 1 0	1 1 1 0 0 0 0 0 0 0 0 0
0.25 mV	Mid scale + ½ LSB	1 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	1 1 0 0 0 0 0 0 0 0 0 0
–0.25 mV	Mid scale – ½ LSB	0 1 1 1 1 1 1 1 1 1 1 0	1 1 1 1 1 1 1 1 1 1 1 0	0 1 0 0 0 0 0 0 0 0 0 0
–124.75 mV	$^1/_4$ full scale + ½ LSB	0 1 0 0 0 0 0 0 0 0 0 0	1 1 0 0 0 0 0 0 0 0 0 0	0 1 1 0 0 0 0 0 0 0 0 0
–124.25 mV	$^1/_4$ full scale – ½ LSB	0 0 1 1 1 1 1 1 1 1 1 0	1 0 1 1 1 1 1 1 1 1 1 0	0 0 1 0 0 0 0 0 0 0 0 0
–249.75 mV	Bottom end of full scale + ½ LSB	0 0 0 0 0 0 0 0 0 0 0 1	1 0 0 0 0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0 0 0 0 1
–250.25 mV	Bottom end of full scale – ½ LSB	0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0
< –250.25 mV	< Bottom end of full scale – ½ LSB	0 0 0 0 0 0 0 0 0 0 0 1	1 0 0 0 0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0 0 0 0 1

A9 = B9 = C9 = D9 = MSB

A0 = B0 = C0 = D0 = LSB

Note: 1. Refer to Table 4-9 on page 44 for selection between Natural Binary, Binary two's complement or Gray coding.

2.8 Explanation of Test Levels

Table 2-12. Test Levels

1	100% production tested at +25°C[1] (for C temperature range[2])
2	100% production tested at +25°C[1], and sample tested at specified temperatures for V temperature ranges[2].
3	Sample tested only at specified temperature
4	Parameter is guaranteed by design and characterization testing (thermal steady-state conditions at specified temperature)
5	Parameter is a typical value only guaranteed by design only

Only MIN and MAX values are guaranteed (typical values are issuing from characterization results).

Notes: 1. Unless otherwise specified.
2. Refer to Section 7. "Ordering Information" on page 64.

2.9 Definition of Terms

(Fs max)	Maximum Sampling Frequency	Performances are guaranteed up to Fs max	
(Fs min)	Minimum Sampling frequency	Performances are guaranteed for clock frequency higher than Fs min	
(BER)	Bit Error Rate	Probability to exceed a specified error threshold for a sample at maximum specified sampling rate. An error code is a code that differs by more than ± 32 LSB from the correct code.	
(FPBW)	Full power input bandwidth	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at Full Scale –1 dB (–1 dBFS).	
(SSBW)	Small Signal Input bandwidth	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at Full Scale –10 dB (–10 dBFS).	
(SINAD)	Signal to noise and distortion ratio	Ratio expressed in dB of the RMS signal amplitude, set to 1 dB below Full Scale (–1 dBFS), to the RMS sum of all other spectral components, including the harmonics except DC.	
(SNR)	Signal to noise ratio	Ratio expressed in dB of the RMS signal amplitude, set to 1 dB below Full Scale, to the RMS sum of all other spectral components excluding the ten first harmonics.	
(THD)	Total harmonic distortion	Ratio expressed in dB of the RMS sum of the first ten harmonic components, to the RMS input signal amplitude. It may be reported in dBFS (i.e, related to converter Full Scale), or in dBc (i.e, related to input signal level).	
(SFDR)	Spurious free dynamic range	Ratio expressed in dB of the RMS signal amplitude to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic. It may be reported in dBFS (i.e., related to converter Full Scale), or in dBc (i.e, related to input signal level).	
(ENOB)	Effective Number Of Bits	$ENOB = \frac{SINAD - 1.76 + 20 \log (A / FS/2)}{6.02}$	Where A is the actual input amplitude and FS is the full scale range of the ADC under test
(DNL)	Differential non linearity	The Differential Non Linearity for an output code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic.	
(INL)	Integral non linearity	The Integral Non Linearity for an output code i is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.	
(TA)	Aperture delay	Delay between the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point), and the time at which (V_{IN},V_{INN}) is sampled.	
(JITTER)	Aperture uncertainty	Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.	
(TS)	Settling time	Time delay to achieve 0.2% accuracy at the converter output when a 80% Full Scale step function is applied to the differential analog input.	
(ORT)	Overvoltage recovery time	Time to recover 0.2% accuracy at the output, after a 150% full scale step applied on the input is reduced to midscale.	
(TOD)	Digital data Output delay	Delay from the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.	
(TDR)	Data ready output delay	Delay from the falling edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.	
(TD1)	Time delay from Data transition to Data Ready	Time delay between Data transition to output clock (Data Ready). If output clock is in the middle of the Data, TD1 = Tdata/2	
(TD2)	Time delay from Data Ready to Data	Time delay between output clock (Data Ready) to Data transition. If output clock is in the middle of the Data, TD2 = Tdata/2.	

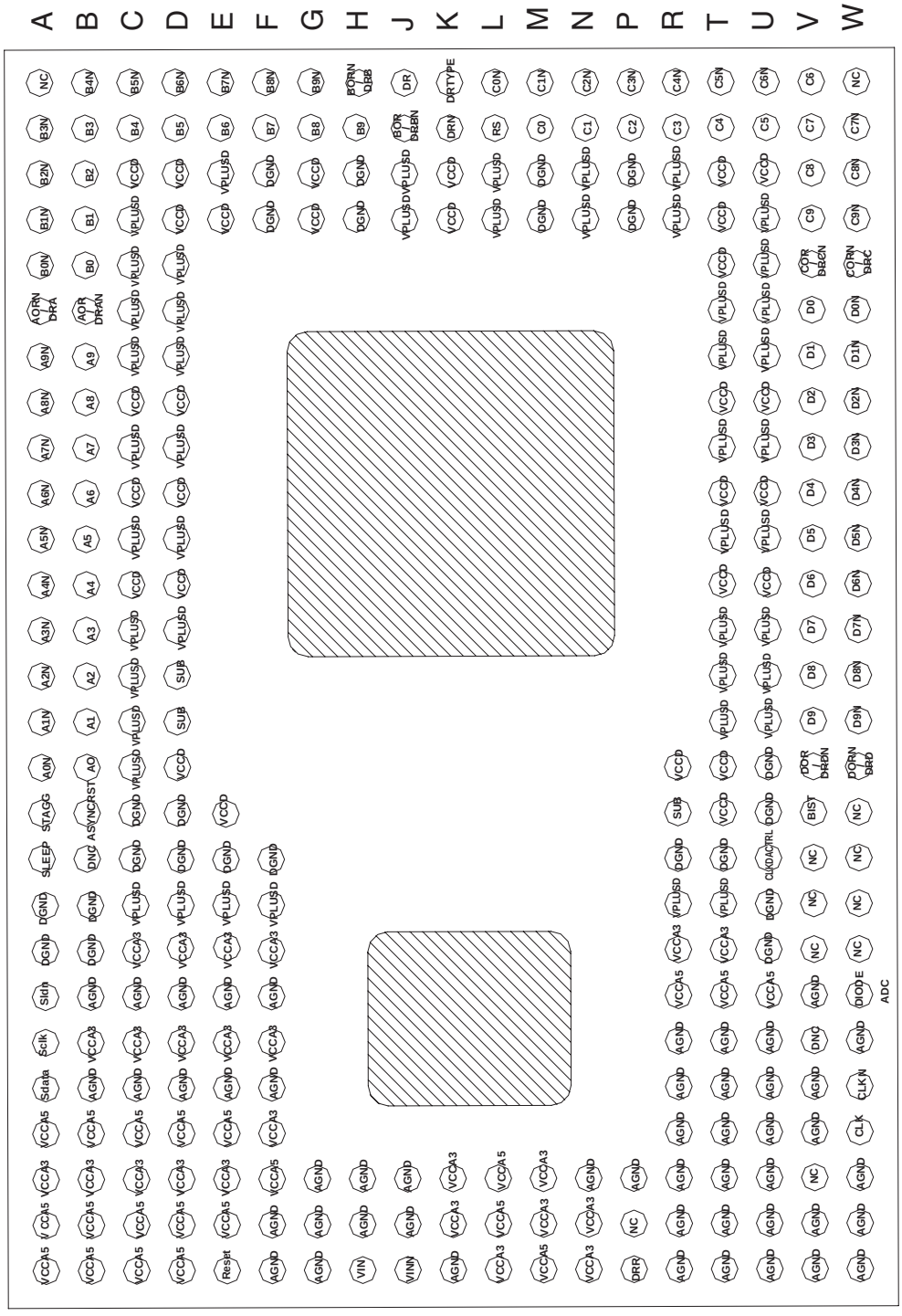
2.9 Definition of Terms (Continued)

TD1-TD2		The difference TD1-TD2 gives an information if the output clock is centered on the output data. If output clock is in the middle of the data TD1 = TD2 = Tdata/2.
(TC)	Encoding clock period	TC1 = Minimum clock pulse width (high) TC = TC1 + TC2 TC2 = Minimum clock pulse width (low)
(TPD)	Pipeline Delay	Number of clock cycles between the sampling edge of an input data and the associated output data being made available, (not taking in account the TOD).
(TR)	Rise time	Time delay for the output DATA signals to rise from 20% to 80% of delta between low level and high level.
(TF)	Fall time	Time delay for the output DATA signals to fall from 20% to 80% of delta between low level and high level.
(PSRR)	Power supply rejection ratio	Ratio of input offset variation to a change in power supply voltage.
(IMD)	Intermodulation Distortion	The two tones intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products.
(NPR)	Noise Power Ratio	The NPR is measured to characterize the ADC performance in response to broad bandwidth signals. When applying a notch-filtered broadband white-noise signal as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test.
(VSWR)	Voltage Standing Wave Ratio	The VSWR corresponds to the ADC input insertion loss due to input power reflection. For example a VSWR of 1.2 corresponds to a 20 dB return loss (that is, 99% power transmitted and 1% reflected).

3. Pin Description

3.1 Pinout View

Figure 3-1. EBGA 317 Pinout Table (View from Bottom of the Package)



Note: Area in dashed line corresponds to dam & fill (note an exposed pad)

3.2 Pin Description Table

Table 3-1. Pin Description Table

Signal Name	Pin Number	Description	Dir.	Equivalent Simplified Schematics
POWER SUPPLIES				
V_{CCA5}	A24, A26, A27, B24, B26, B27, C24, C26, C27, D24, D26, D27, E24, E26, F25, L25, L26, M27, R21, T21, U21	Analog 5.0V Power Supply (ADC)		
V_{CCA3}	A25, B22, B25, C20, C22, C25, D20, D22, D25, E20; E22, E25, F20, F22, F24, K25, K26, L27, M25, M26, N26, N27, R20, T20	Analog 3.3V Power Supply (ADC)		
V_{PLUSD}	C4, C5, C6, C7, C9, C11, C13, C14, C15, C16, C19, D5, D6, D7, D9, D11, D13, D19, E3, E19, F19, J3, J4, L3, L4, N3, N4, R3, R4, R19, T6, T7, T9, T11, T13, T14, T15, T19, U4, U5, U6, U7, U9, U11, U13, U14, U15	Output 2.5V Power Supply (ADC and DMUX)		
V_{CCD}	C3, C8, C10, C12, D3, D4, D8, D10, D12, D16, E4, E17, G3, G4, K3, K4, R16, T3, T4, T5, T8, T10, T12, T16, T17, U3, U8, U10, U12	Digital 3.3V Power Supply (DMUX)		
SUB	D14, D15, R17	Substrate connect to Board Ground Plane (DGND)		
DGND	A19, A20, B19, B20, C17, C18, D17, D18, E18, F3, F4, F18, H3, H4, M3, M4, P3, P4, R18, T18, U16, U17, U19, U20	Digital Ground, connect to Board Ground Plane		

Table 3-1. Pin Description Table (Continued)

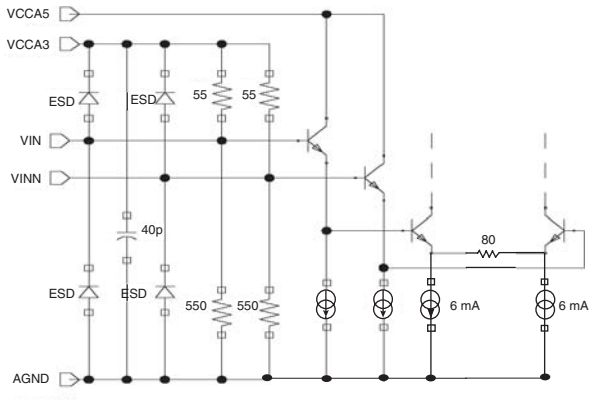
Signal Name	Pin Number	Description	Dir.	Equivalent Simplified Schematics
AGND	B21, B23, C21, C23, D21, D23, E21, E23, F21, F23, F26, F27, G25, G26, G27, H25, H26, J25, J26, K27, N25, P25, R22, R23, R24, R25, R26, R27, T22, t23, T24, T25, T26, T27, U22, U23, U24, U25, U26, U27, V21, V23, V24, V26, V27, W22, W25, W26, W27	Analog Ground, connect to Board Ground Plane		
NO CONNECT				
DNC	B18	Do Not connect (Leave this pin floating)		
NC	W1, W18, W17, W19, V19, W20, V20, A1, V18, P26, V22, V25	Pins can be left no connect or grounded.		
ANALOG INPUTS				
V_{IN} V_{INN}	H27 J27	ADC In-Phase Analog input ADC Inverted-Phase Analog input (On chip 2 × 50Ω terminated, 3V biased)	I	

Table 3-1. Pin Description Table (Continued)

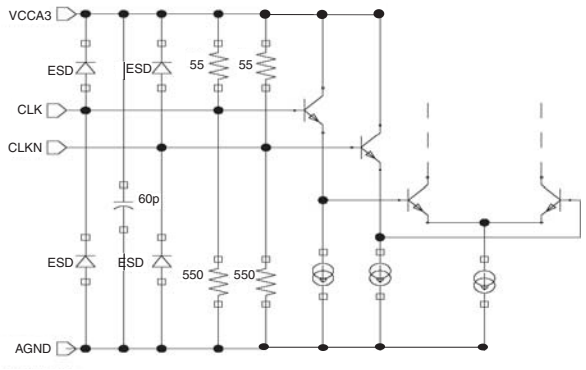
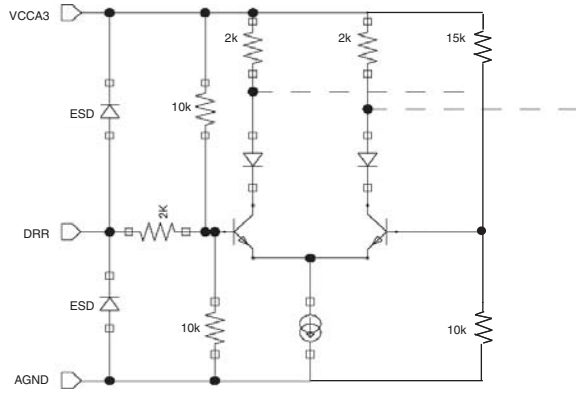
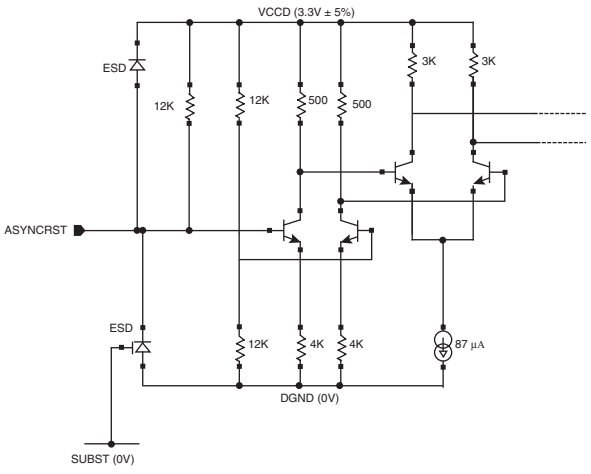
Signal Name	Pin Number	Description	Dir.	Equivalent Simplified Schematics
CLOCK INPUTS				
CLK CLKN	W24 W23	ADC Clock Differential Inputs (On chip 50Ω terminated, 3V biased)	I	
RESET INPUT				
DRR	P27	ADC Data Ready reset (active High or Low depending on bit D8 of state register at address 0110)	I	
ASYNCRST	B17	DMUX Asynchronous Reset • Leave floating or connect to V_{CCD} for RESET mode • Connect to Ground for normal mode	I	

Table 3-1. Pin Description Table (Continued)

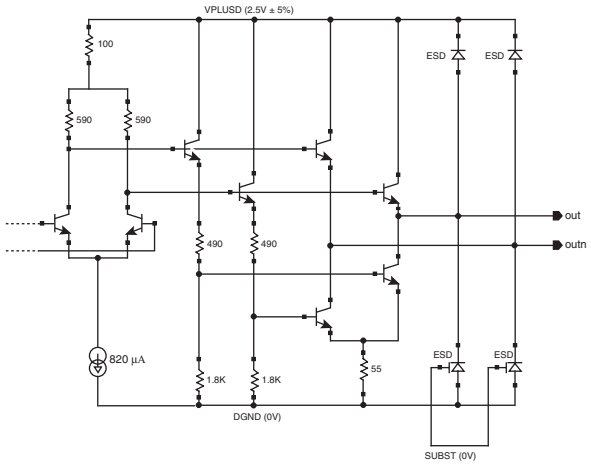
Signal Name	Pin Number	Description	Dir.	Equivalent Simplified Schematics
DIGITAL OUTPUTS				
A0…A9	B16, B15, B14, B13, B12, B11, B10, B9, B8, B7	In-Phase Digital Outputs Port A LVDS compatible A0 = LSB, A9 = MSB	O	
A0N…A9N	A16, A15, A14, A13, A12, A11, A10, A9, A8, A7	Inverted-Phase Digital Outputs Port A LVDS compatible A0N = LSB, A9N = MSB	O	
AOR/DRAN AORN/DRA	B6 A6	Port A Out of Range in simultaneous mode or Port A Data Ready Output Clock in staggered mode	O	
B0…B9	B5, B4, B3, B2, C2, D2, E2, F2, G2, H2	In-Phase Digital Outputs Port B LVDS compatible B0 = LSB, B9 = MSB	O	
B0N…B9N	A5, A4, A3, A2, B1, C1, D1, E1, F1, G1	Inverted-Phase Digital Outputs Port B LVDS compatible B0N = LSB, B9N = MSB	O	
BOR/DRBN BORN/DRB	J2 H1	Port B Out of Range in simultaneous mode or Port B Output Clock in staggered mode	O	

Table 3-1. Pin Description Table (Continued)

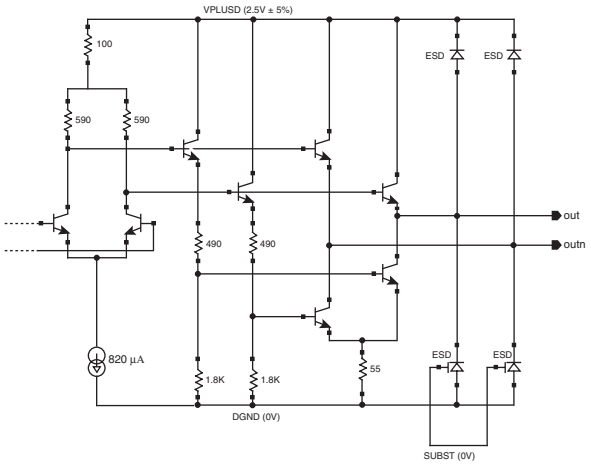
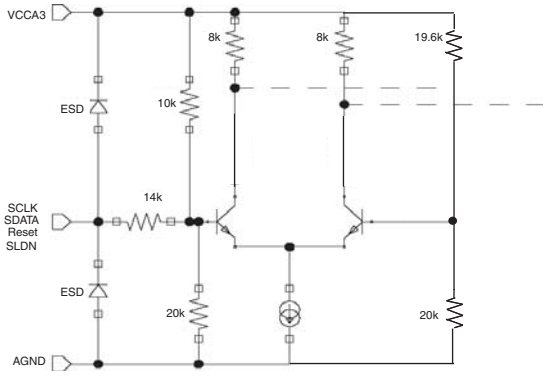
Signal Name	Pin Number	Description	Dir.	Equivalent Simplified Schematics
C0…C9	M2, N2, P2, R2, T2, U2, V1, V2, V3, V4	In-Phase Digital Outputs Port C LVDS compatible C0 = LSB, C9 = MSB	O	
C0N…C9N	L1, M1, N1, P1, R1, T1, U1, W2, W3, W4	Inverted-Phase Digital Outputs Port C LVDS compatible C0N = LSB, C9N = MSB	O	
COR/DRCN CORN/DRC	V5 W5	Port C Out of Range in simultaneous mode Or Port C Data Ready Output Clock in staggered mode	O	
D0…D9	V6, V7, V8, V9, V10, V11, V12, V13, V14, V15	In-Phase Digital Outputs Port D LVDS compatible D0 = LSB, D9 = MSB	O	
D0N…D9N	W6, W7, W8, W9, W10, W11, W12, W13, W14, W15	Inverted-Phase Digital Outputs Port D LVDS compatible D0N = LSB, D9N = MSB	O	
DOR/DRDN DORN/DRD	V16 W16	Port D Out of Range in simultaneous mode or Port D Data Ready Output Clock in staggered mode	O	
DR DRN	J1 K2	Differential Data Ready Output Clock LVDS compatible	O	
CONTROL INPUT FUNCTIONS				
RESET	E27	Reset for fast programming of 3WSI to default values.	I	
SDATA	A23	Data input of 3WSI (3 Wires Serial Interface)	I	
SLDN	A21	Load Enable input of 3WSI	I	
SCLK	A22	Clock input of 3WSI	I	

Table 3-1. Pin Description Table (Continued)

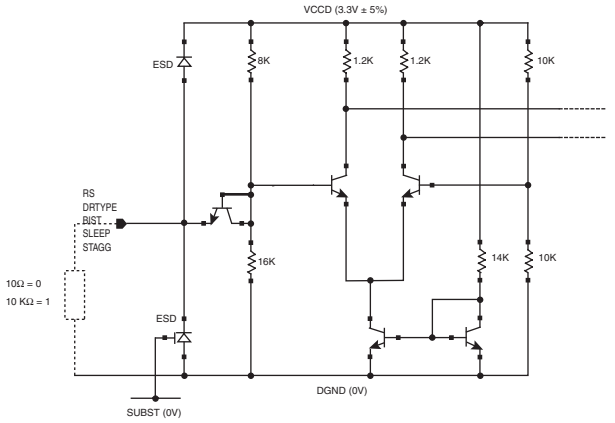
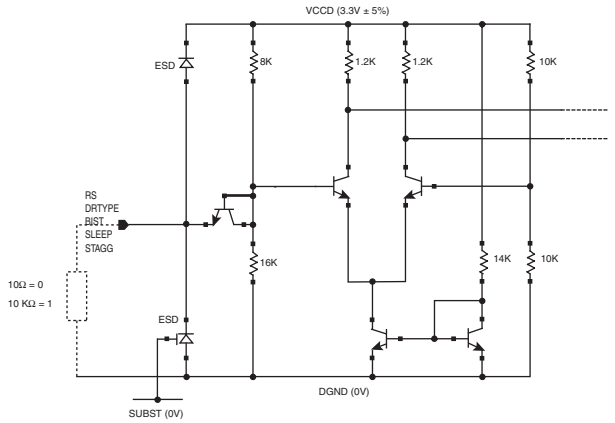
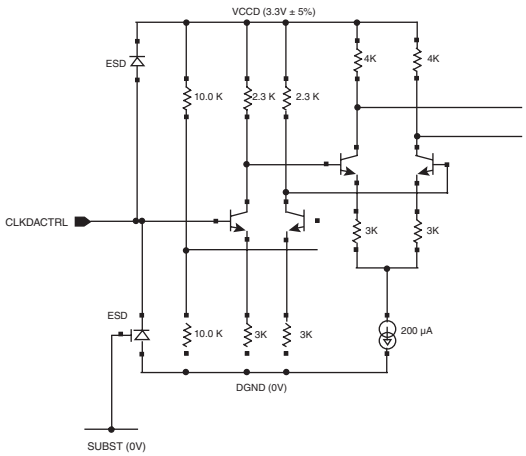
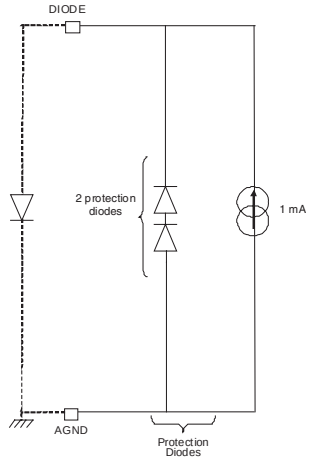
Signal Name	Pin Number	Description	Dir.	Equivalent Simplified Schematics
SLEEP	A18	DMUX SLEEP mode Enable ▪ Leave floating or connect to V_{CCD} for normal mode ▪ Connect to Ground for SLEEP mode	I	
STAGG	A17	DMUX Staggered mode Enable ▪ Leave floating or connect to V_{CCD} for normal mode ▪ Connect to Ground for STAGG mode	I	
DRTYPE	K1	DMUX Output Clock mode selection ▪ Connect to Ground for DR/2 type ▪ Leave floating or connect to V_{CCD} for DR type	I	
RS	L2	DMUX Ratio mode selection ▪ Connect to Ground for 1:2 ratio ▪ Leave floating or connect to V_{CCD} for 1:4 ratio	I	
BIST	V17	DMUX BIST mode ▪ Leave floating or connect to V_{CCD} for normal mode ▪ Connect to Ground for BIST mode	I	

Table 3-1. Pin Description Table (Continued)

Signal Name	Pin Number	Description	Dir.	Equivalent Simplified Schematics
CLKDACTRL	U18	DMUX clock Delay control (from 1/3 × V_{CCD} to 2/3 × V_{CCD})	I	
CONTROL OUTPUT FUNCTIONS				
DIODE ADC	W21	ADC Die Junction Temperature monitoring	I/O	

4. Theory of Operation

4.1 Overview

The EV10AS150A is a 10-bit 2.5 Gsps ADC combined with a 1:4 demultiplexer (DMUX) allowing to lower the output Data stream (10-bit data and one out-of-range bit) by a selectable factor of 2 or 4. (Please note that for maximal operating speed, the DMUX has to be used in 1:4 mode).

The ADC works in fully differential mode from analog input up to digital outputs. The ADC differential Analog Inputs and Clock Inputs are on chip 100Ω terminated.

The ADC analog input can be driven in either single ended or differential configuration without significant impact on dynamic performances (SFDR), but slight degradation on THD since the weighting of second and third harmonics are similar in single-ended.

The output Data clock and Digital output data are LVDS logic compatible, and should be 100Ω differentially terminated (2nH // 2 pF maximum output loading parasitics).

The main functions of the EV10AS150A ADC are digitally controlled via on-chip DACs controlled by 3-wire serial interface (3WSI):

- Sampling Delay Adjust, with a tuning range of ~ 120 ps, with a coarse and a fine tuning available (8-bit resolution on the fine tuning of ~30 ps);
- Offset Control, ± 20 mV, 8-bit resolution.
- Gain Control, ±0.5 dB, 8-bit resolution
- Delay adjustment between the logical clock and the T/H clock, 0 to 30 ps (5-bit resolution).
- Internal clock duty cycle adjust from 60% to 70% at 2.5 Gsps (5-bit resolution).
- Selectable Binary or the Gray coding mode.
- Selectable inversion of MSB for Binary two's complement.
- Reset to program quickly all registers to default values.
- NAP (ADC part) mode to save power when device is not used.

The Sampling Delay Adjust function (controlled through the 3WSI) may be used to fine-tune the ADC aperture delay from 0 to 120 ps. The SDA function is very useful when interleaving multiple ADCs.

The output demultiplexing ratio 1:4 or 1:2 can be selected by the means of RS digital control input.

The data outputs are available at the output of the EV10AS150A with two different latency modes:

- Staggered (Low latency): data output on ports A, B, C and D are shifted from one clock cycle between two successive ports.
- Simultaneous: data output on all ports A, B, C and D are aligned.

A Built-In Test (BIST) is provided for quick debug or acquisition setup: activation of checker board like pattern generator.

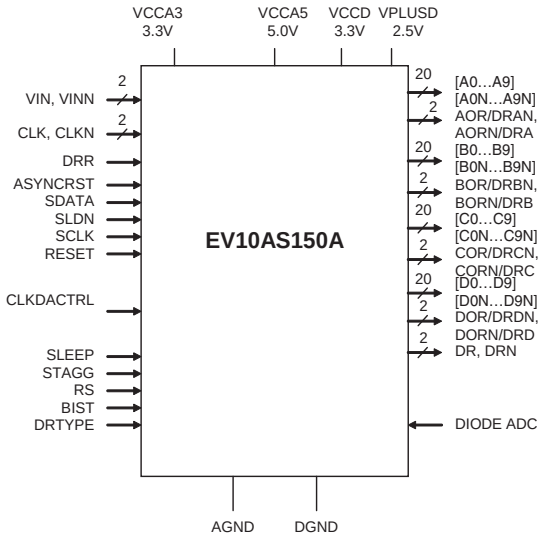
The ADC junction temperature monitoring is made possible through the DIODE ADC input by sensing the voltage drop across a diode implemented on the ADC close to chip hot point.

The EV10AS150A is delivered in an Enhanced Ball Grid Array (EBGA), suitable for applications subjected to large thermal variations (thanks to its TCE which is similar to FR4 material TCE).

4.2 Functional Pin Table

Table 4-1. Functional Pin Table

Name	Function
V_{CCA5}	Analog 5.0V Power Supply
V_{CCA3}	Analog 3.3V Power supply
V_{CCD}	Digital 3.3V Power supply
V_{PLUSD}	Output 2.5V Power Supply
AGND	Analog Ground
DGND	Digital Ground
CLK, CLKN	ADC clock input signal
V_{IN}, V_{INN}	ADC Analog Input signal
DRR	ADC Data Ready reset
ASYNCRST	DMUX Asynchronous Reset
DR/DRN	Data Ready output clock
A0… A9 A0N…A9N	Digital Output Data Port A
AOR/DRAN, AORN/DRA	Out-of-range bit Port A or Data Ready output clock in staggered mode Port A
B0… B9 B0N…B9N	Digital Output data Port B
BOR/DRBN, BORN/DRB	Out-of-range bit Port B or Data Ready output clock in staggered mode Port B
C0… C9 C0N…C9N	Digital Output data Port C
COR/DRCN, CORN/DRC	Out-of-range bit Port C or Data Ready output clock in staggered mode Port C
D0… D9 D0N…D9N	Digital Output data Port D
DOR/DRDN, DORN/DRD	Out-of-range bit Port D or Data Ready output clock in staggered mode Port D
RS	DMUX Ratio Selection signal (1:2 or 1:4)
CLKDACTRL	Control signal input for fine tuning of internal ADC Data Clock Delay line.
DIODE ADC	Diode for die Junction Temperature monitoring (ADC)



Name	Function
BIST	Built In output checker board Pattern generation
SLEEP	DMUX Sleep mode input pin selection signal
DRTYPE	Data Ready Output Clock Type selection (Dual Data Rate DR/2 or DR)
STAGG	Staggered mode selection for Data outputs (low latency)
SCLK	3 Wire Serial Interface (3WSI) Clock input
SDATA	3 Wire Serial Interface (3WSI) serial Input Data
SLDN	3 Wire Serial Interface (3WSI) Load Enable signal (Active low)
RESET	3WSI Reset input (force registers default settings).

4.3 RESETs and ADC Synchronization

There are three reset signals available on the device to start the device properly:

- DRR (Data Ready Reset) is used to reset and synchronize the Data Ready Output Clock of the ADC. DRR ensures that the first edge of the ADC output Data clock after DRR reset pulse is always a rising edge. This ensures that the first Data for N sampled after ADC reset corresponds to the first acquisition in the DMUX.
- ASYNCRST is an asynchronous reset used to synchronize the DMUX so that the data are outputted on the right order (Port A, then Port B, then Port C and then Port D). It is also necessary to have a deterministic sequence in BIST mode.
- RESET is a signal used to reset (load default settings) the 3 Wire Serial Interface (3WSI), see Section 4.5.2.

DRR, RESET and ASYNCRST are mandatory for proper device initialization.

Please refer to the paragraph 5.5 for more information on how to implement these reset functions.

DRR is active high or low depending on bit D8 of state register at address 0110 while ASYNCRST is active high.

It is mandatory to apply ASYNCRST while DRR is active.

2 sequences are recommended depending on the applications.

- **Sequence 1: to be used in the case where multiples ADCs synchronization is not needed**

1. Perform a RESET on ADC (DRR active low or high depending on 3WSI settings). Maintain DRR active up to step 4.
2. While DRR is active, perform an asynchronous reset of the DEMUX (ASYNCRST high).
3. Release ASYNCRST (ASYNCRST low) (minimum pulse width is 3ns)
4. Release DRR (minimum DRR pulse width is 3.5ns)
5. 3WSI interface can then be programmed if needed.

During this sequence 1, the clock can be running or not running. But pipeline delay up to ADC outputs will not be deterministic.

- **Sequence 2: to be used in the case where multiples ADCs synchronization is needed**

1. Apply a running clock in order to initialize ADC clock path
2. Stop ADC clock at low level
3. Perform a RESET on ADC (DRR active low or high depending on 3WSI settings).
4. Maintain DRR active up to step 7.
5. While DRR is active, perform an asynchronous reset of the DEMUX (ASYNCRST high).
6. Release ASYNCRST (ASYNCRST low) (minimum pulse width is 3ns)
7. Release DRR (minimum DRR pulse width is 3.5ns)
8. Restart ADC clock
9. 3WSI interface can then be programmed if needed.

With this sequence 2, all ADCs will start on the first rising edge of the clock and they will be synchronized.

Figure 4-1. Asynchronous Reset Timing Diagram, 1:2 Mode, Simultaneous Mode (Principle of Operation)

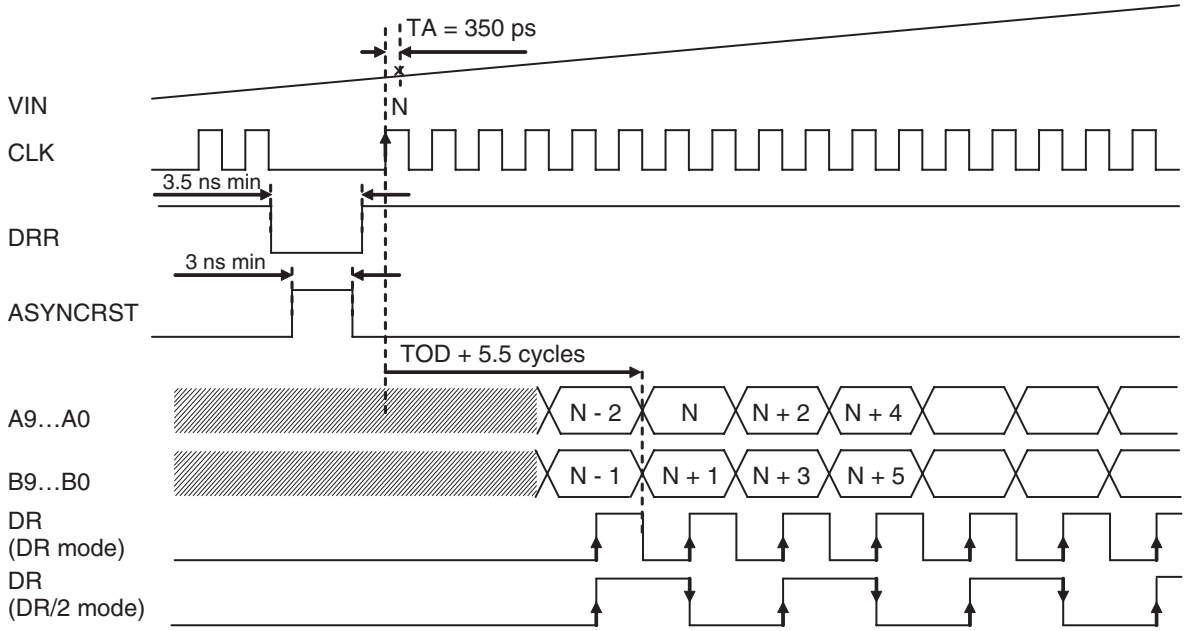
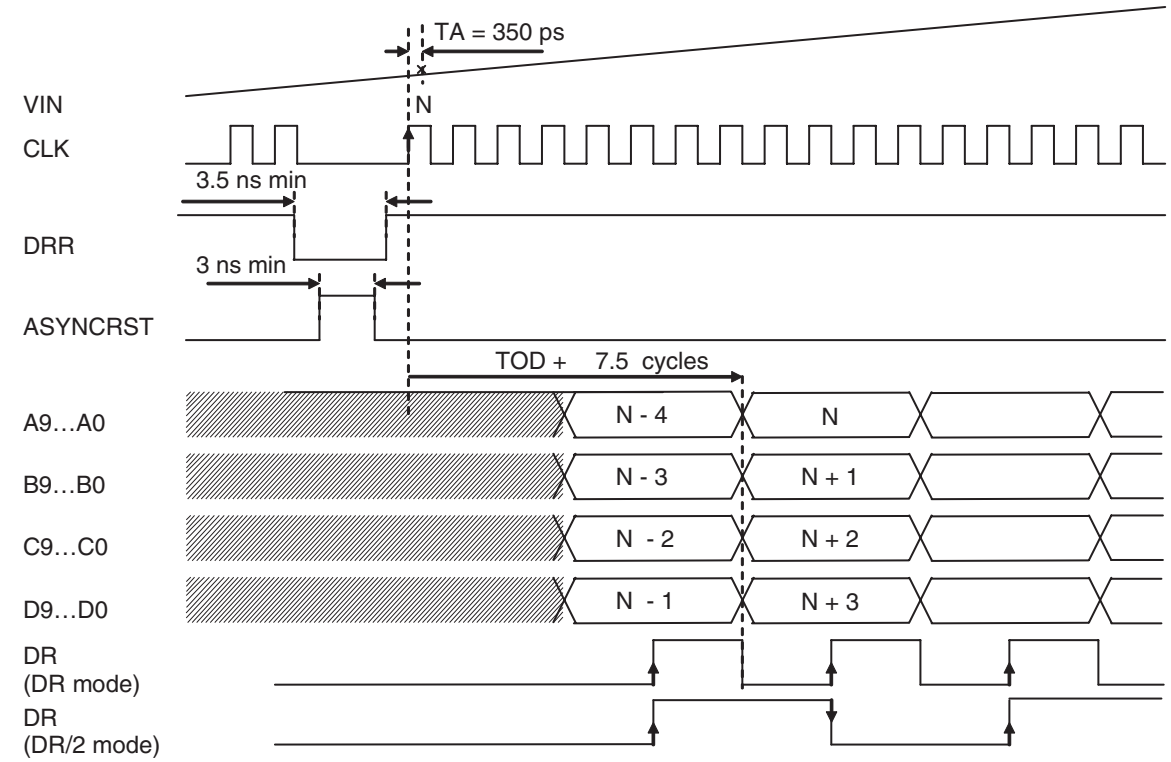


Figure 4-2. Asynchronous Reset Timing Diagram, 1:4 mode, simultaneous mode (Principle of operation)



4.4 Control Signal Settings (DMUX)

The SLEEP, RS, STAGG, BIST and DRTYPE control signals use the same input buffer.

SLEEP, STAGG, BIST are activated on Logic Low (10Ω Grounded), and deactivated on Logic High (10 KΩ to Ground, or tied to V_{CCD} = 3.3V, or left floating).

This is illustrated in Figure hereafter:

Figure 4-3. Control Signal Settings (SLEEP, RS, STAGG, BIST and DRTYPE)

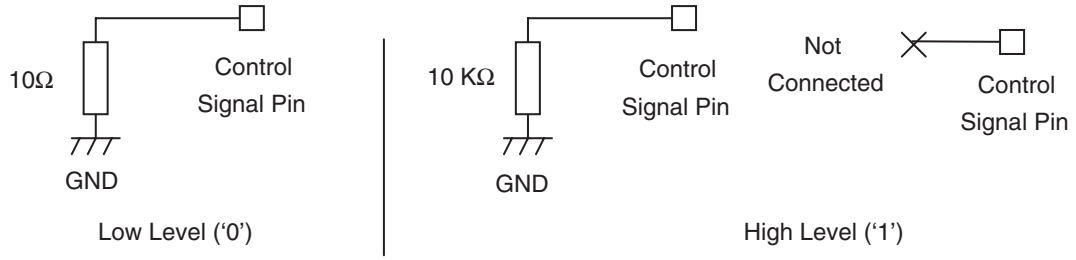


Table 4-2. DMUX Mode Settings - Summary

Function	Logic Level	Electrical Level		Description
		Static drive	Dynamic drive[(1)]	
BIST	0	10Ω to ground	V(BIST) = V_{IL}	BIST: Checker board on output data
	1	10 KΩ to ground	V(BIST) ≥ V_{IH}	Normal conversion
		N/C		
SLEEP	0	10Ω to ground	V(SLEEP) = V_{IL}	Power reduction mode (the outputs are fixed at an arbitrary LVDS level)
	1	10 KΩ to ground	V(SLEEP) ≥ V_{IH}	Normal conversion
		N/C		
STAGG	0	10Ω to ground	V(STAGG) = V_{IL}	Staggered mode
	1	10 KΩ to ground	V(STAGG) ≥ V_{IH}	Simultaneous mode
		N/C		
RS	0	10Ω to ground	V(RS) = V_{IL}	1:2 ratio
	1	10 KΩ to ground	V(RS) ≥ V_{IH}	1:4 ratio
		N/C		
DRTYPE	0	10Ω to ground	V(DRTYPE) = V_{IL}	DR/2 mode
	1	10 KΩ to ground	V(DRTYPE) ≥ V_{IH}	DR mode

Note: 1. Refer to Table 2-4 on page 7 for logical levels.

4.4.1 DMUX Ratio

The demultiplexer ratio is programmable thanks to the RS Ratio selection signal.

Table 4-3. DMUX Ratio Selection Settings

RS	DMUX Ratio
0	1:2
1	1:4

Figure 4-4. DMUX in 1:2 Ratio

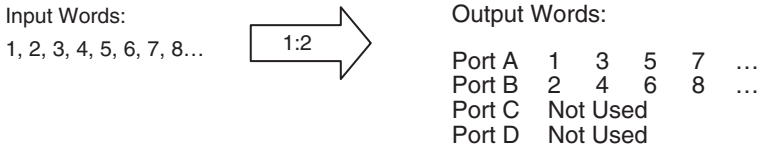
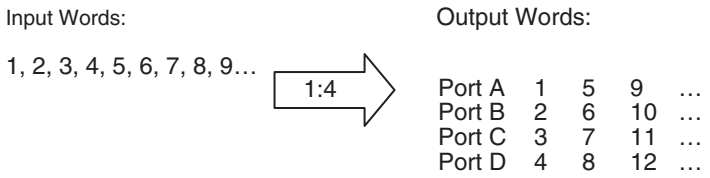


Figure 4-5. DMUX in 1:4 Ratio



4.4.2 DMUX Data Ready Output Clock Selection (DRTYPE)

DMUX Data Ready Output Clock is used to latch EV10AS150A output data.

Two modes for the output Data clock rate can be selected (via DRTYPE):

- DR mode: The output data clock frequency is 1/4th the ADC Clock frequency (assuming 1:4 DMUX Ratio), and switches at twice the output data rate. Therefore only the rising edge is considered as active for output data registering (Rising edge of differential output Data clock (DR, DRN) is located at center of the digital data pulse).
- DR/2 mode: The output data clock frequency is 1/8th the ADC Clock frequency (assuming 1:4 DMUX Ratio), the output clock switches at same rate as the digital data. Therefore, both output Data clock rising and falling edges are active for output data registering (Rising and Falling edge of differential output Data clock (DR, DRN) are located at center of the digital data pulse).

This is illustrated in the following figures:

Figure 4-6. DR Mode

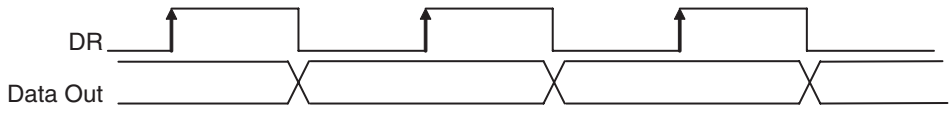


Figure 4-7. DR/2 Mode

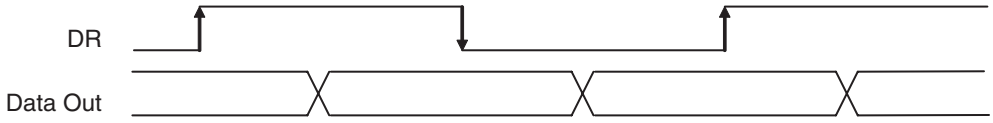


Table 4-4. DMUX Output Clock Type Selection Settings

DRTYPE	DMUX Output Clock Type
1	DR
0	DR/2

When DRTYPE is left floating, the default mode is DR.

4.4.3 DMUX Output Data Mode (STAGG)

Two output modes are provided:

- Staggered: the output data come out of the DMUX the one after the other;
- Simultaneous: the output data come out of the DMUX at the same time.

In staggered mode, the output clock for each port is provided by the DRA, DRAN, DRB, DRBN, DRC, DRCN and DRD, DRDN signals which corresponds respectively to the AORN, AOR, BORN, BOR, CORN, COR, DORN and DOR.

The Simultaneous mode is the default mode (STAGG left floating or at logic “1”).

The Staggered mode is activated by the means of the STAGG input (active low).

Figure 4-8. Simultaneous Mode in 1:4 Ratio (STAGG = 1)

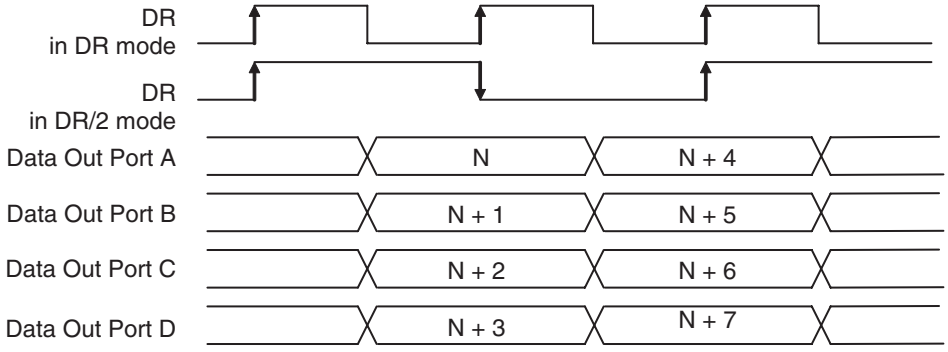


Figure 4-9. Simultaneous Mode in 1:2 Ratio (STAGG = 1)

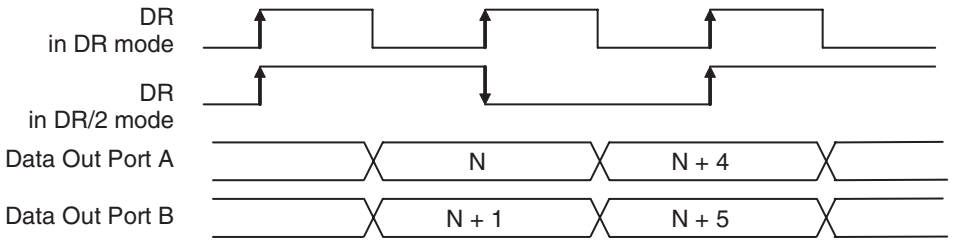


Figure 4-10. Staggered Mode in 1:2 Ratio (STAGG = 0)

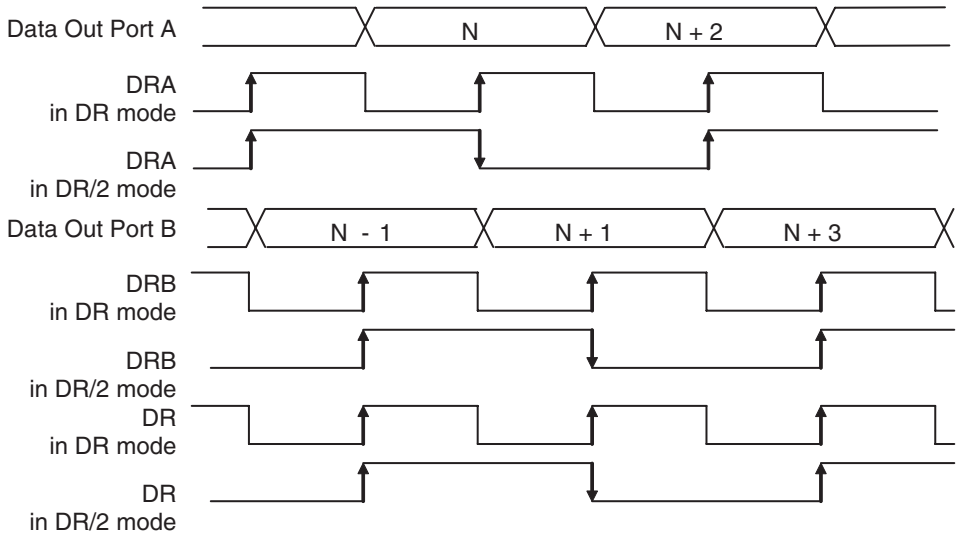
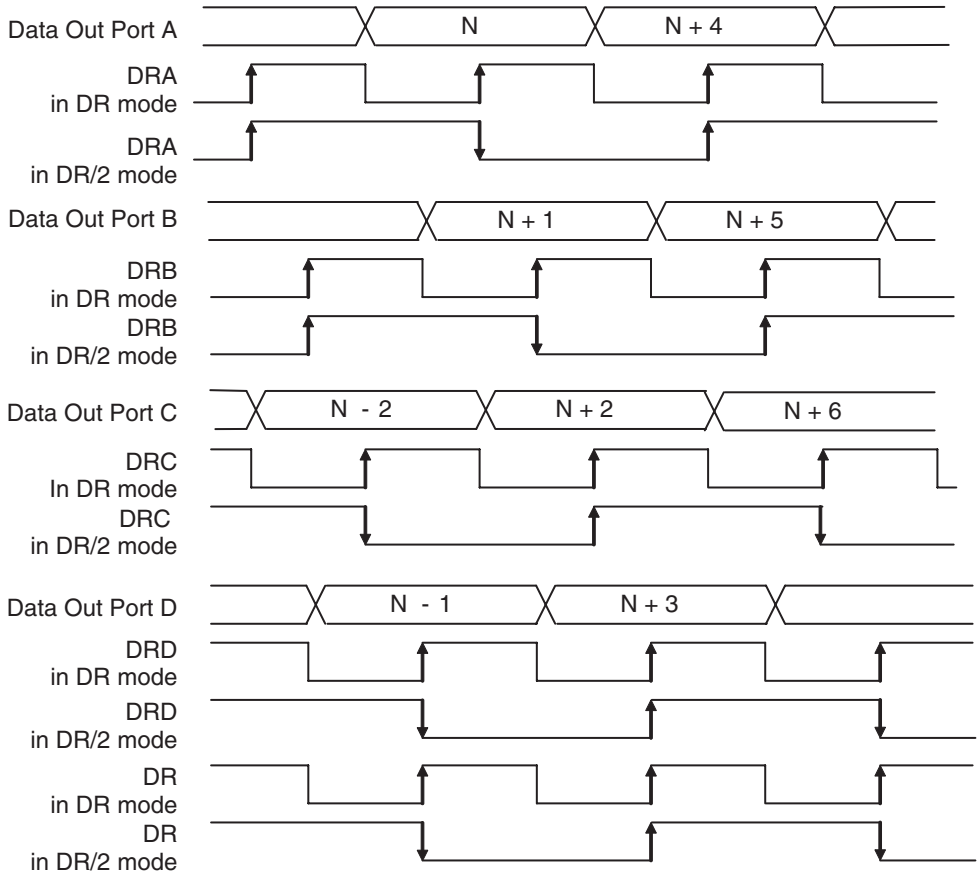


Figure 4-11. Staggered Mode in 1:4 Ratio (STAGG = 0)



4.4.4 Out-of-range Bit and Data Ready Output Clocks

In simultaneous output mode:

The (AOR/DRAN, AORN/DRA), (BOR/DRBN, BORN/DRB), (COR/DRCN, CORN/DRC) and (DOR/DRDN, DORN/DRD) signals are used to add the out-of-range bit to the ADC output data.

On each port (A, B, C, D) the out-of-range bit (*OR/*ORN) indicates (logic “1”) when the analog input overrides the ADC 0.5 Vpp Full Scale voltage span, in case of underflow or overflow.

When the analog input exceeds the positive full scale, the 10 bit digital outputs data remain at high logical state, with (*OR,*ORN) at logical one. When the analog input falls below the negative full scale, the 10 bit digital outputs data remain at logical low state, with (*OR,*ORN) at logical one again.

In Staggered output mode:

The (AOR/DRAN, AORN/DRA), (BOR/DRBN, BORN/DRB), (COR/DRCN, CORN/DRC) and (DOR/DRDN, DORN/DRD) signals will output the Data Ready Output Clock signal (one for each port), centered on the corresponding Data.

In this case, the overflow can be computed with all 10 digital output data detection at logic “1”, (Binary mode), and underflow can be computed with all 10 digital output data detection at logic “0” (Binary mode).

In 1:2 DMUX Ratio, DR/DRN and DRB/DRBN are identical.

In 1:4 DMUX Ratio, DR/DRN and DRD/DRDN are identical.

4.4.5 DMUX Power Reduction Mode (SLEEP)

The power reduction (SLEEP) mode allows the user to reduce the power consumption of the device (DMUX part in Sleep mode). In this mode, the DMUX part consumption is reduced by 0.9W.

The Power reduction mode is active when SLEEP is low.

The device is in normal mode when SLEEP is high.

When the device is not used, minimal Power consumption is obtained with NAP (ADC part) and SLEEP (DMUX part) modes used simultaneously.

4.4.6 DMUX Clock input Delay Cell (CLKDACTRL)

A tunable delay cell (CLKDACTRL) is in serial on the 11 Bit DMUX Data path to fine tune the data vs. clock alignment at the interface between the ADC and the DMUX.

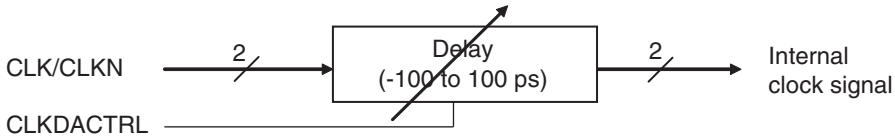
The delay is controlled via the CLKDACTRL pin. This delay can be tuned around default center value. It ranges from –100 ps to 100 ps for CLKDACTRL varying from V_{CCD} / 3 to 2 × V_{CCD} / 3.

This function results in a delayed internal clock signal.

This pin must always be biased and it is recommended to set CLKDACTRL at V_{CCD}/3.

With the recommended value, it is normally not necessary to tune the CLKDACTRL voltage over the full specified clock rate, temperature range and power supply voltage range.

Figure 4-12. DMUX Clock Input Cell Block Diagram



4.4.7 DMUX Built-In Test

The Built-In Self Test allows to test rapidly the DMUX block of the device.

It is activating via the BIST bit (active low) a checker board like pattern generator.

When this signal is left floating, the BIST is inactive.

When in BIST mode, a clock must be applied to the device, which can be set to 1:2 or 1:4 mode. The output clock mode DRTYPE can be either DR or DR/2.

In the BIST mode, all the bits are either all at low or high level (even and odd bits are in phase opposition) and transition every new cycle.

In order to have a deterministic output sequence, it is necessary to perform an asynchronous reset.

The output sequence is then:

Table 4-5. BIST Output Sequence in 1:4 Mode

BIST sequence	Binary (D9 …. D0)	Hexa (D9…D0)	Out-of-range Bit
DATA N on Port A	10 1010 1010	0x2AA	0
DATA N+1 on Port B	01 0101 0101	0x155	1
DATA N+2 on Port C	10 1010 1010	0x2AA	0
DATA N+3 on Port D	01 0101 0101	0x155	1
DATA N+4 on Port A	01 0101 0101	0x155	1
DATA N+5 on Port B	10 1010 1010	0x2AA	0
DATA N+6 on Port C	01 0101 0101	0x155	1
DATA N+7 on Port D	10 1010 1010	0x2AA	0
DATA N+8 on Port A	10 1010 1010	0x2AA	0
...	...	...	...

Table 4-6. BIST Output Sequence in 1:2 Mode

BIST sequence	Binary (D9 …. D0)	Hexa (D9…D0)	Out-of-range Bit
DATA N on Port A	10 1010 1010	0x2AA	0
DATA N+1 on Port B	01 0101 0101	0x155	1
DATA N+2 on Port A	01 0101 0101	0x155	1
DATA N+3 on Port B	10 1010 1010	0x2AA	0
DATA N+4 on Port A	10 1010 1010	0x2AA	0
...	...	...	...

4.5 ADC 3 Wire Serial Interface (ADC Controls)

4.5.1 3WSI Address and Data Format

The 3WSI is a synchronous write only serial interface made of 3 wires.

This 3 wire bus is activated with the SLDN control pin going low (please refer to “write timing” in next section).

The length of the word is 14 bits: 10 for the data and 4 for the address.

Bit D[9] of Data is MSB and bit D[3] of address is MSB.

The maximum serial logic clock frequency is 100MHz.

4.5.2 3WSI Timing

The 3WSI is a synchronous write only serial interface made of 3 wires:

- SCLK: serial clock input
- SLDN: serial load enable input
- SDATA: serial data input.

Please refer to Table 2-4 on page 7 for logical levels of SLCK, SLDN, SDATA and RESET.

The 3WSI gives a “write-only” access to up to 16 different internal registers of up to 10 bits each.

The input format is fixed with always 4 bits of register address followed by always 10 bits of data.

Address and data are entered MSB first.

The write procedure is fully synchronous with the clock rising edge of SCLK and described in the write chronogram Figure 4-13 on page 43.

For proper initialization of 3WSI default settings, an asynchronous reset pulse on pin RESET is required.

The RESET pin combined with the SLDN pin must be used as a reset to program the chip to the “reset setting”.

- RESET high: no effect
- RESET low and SLDN low: programming of registers to default values

SLDN and SDATA are sampled on each rising edge of SCLK clock (clock cycle).

SLDN must be set at “1” when no write procedure is done.

A minimum of one clock rising edge (clock cycle) with SLDN at “1” is required for a correct start of the write procedure.

A write starts on the first clock cycle with SLDN at “0”. SLDN must stay at “0” during the complete write procedure.

In the first 4 clock cycles with SLDN at “0”, 4 bits of register address from MSB (a[3]) to LSB (a[0]) are entered.

In the next 10 clock cycles with SLDN at “0”, 10 bits of data from MSB (d[9]) to LSB (d[0]) are entered.

An additional clock cycle with SLDN at “0” is required for parallel transfer of the serial data d[9:0] in the register addressed with address a[3:0].

This gives 15 clock cycles with SLDN at “0” for a normal write procedure.

A minimum of one clock cycle with SLDN returned at “1” is requested to end the write procedure, before the interface is ready for a new write procedure.

Any clock cycle with SLDN at “1” before the write procedure is completed, interrupts this procedure and no data transfer to internal registers is done.

Additional clock cycles with SLDN at “0” after the parallel data transfer to the register (done at 15^{th} consecutive clock cycle with SLDN at “0”) do not affect the write procedure and are ignored.

It is possible to have only one clock cycle with SLDN at “1” between two successive write procedures.

10 bits of data must always be entered even if the internal addressed register has less than 10 bits. Unused bits (usually MSB’s) are ignored. Bit signification and bit position for the internal registers are detailed in the Section 4.5.3.

Figure 4-13. 3WSI Timing Diagram

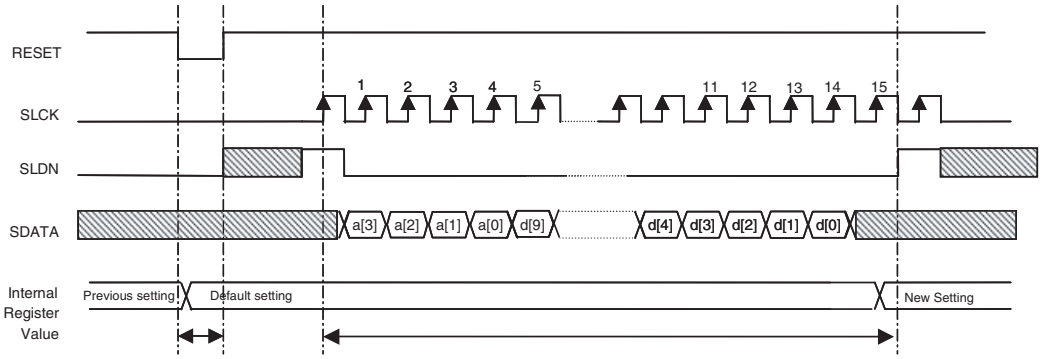


Table 4-7. Timings Related to Serial 3 Wire Serial Interface

Name	Parameter	Min	Typ	Max	Unit	Note
Tsclk	Period of SCLK	10			ns	
Twsclk	High or low time of SCLK	5			ns	
Tssldn	Setup time of SLDN before rising edge of SCLK	4			ns	
Thsldn	Hold time of SLDN after rising edge of SCLK	2			ns	
Tssdata	Setup time of SDATA before rising edge of SCLK	4			ns	
Thsdata	Hold time of SDATA after rising edge of SCLK	2			ns	
Twlreset	Minimum low pulse width of RESET	5			ns	
Tdreset	Minimum delay between an edge of RESET and the rising edge of SCLK	10			ns	

4.5.3 3WSI Register Description

Note: Addresses and/or data bits not described herein are not accessible via Graphical User Interface (GUI).

Table 4-8. 3WSI Settings

Address	Description		Default Value	Recommended Value	Max Value	Min Value	Step
0000	Clock Duty Cycle adjust[1]	**register D4:D0**	10000	10000	11111	00000	0.3%
		parameter value	35/65%	35/65%	30/70%	40/60%	
0001	Clock Adjust[2]	**Register D4:D0**	10000	11111	11111	00000	1 ps
		parameter value	15 ps	+30 ps	+30 ps	0 ps	
0010	Sampling Delay Adjust **Coarse**[3]	**Register D9:D8**	10	SDA OFF (See state register description below)	11	00	30 ps
		parameter value	60 ps		90 ps	0 ps	
	Sampling Delay Adjust **Fine**[3]	**register D7:D0**	00000000		11111111	00000000	120 ps
		parameter value	0 ps		30 ps	0 ps	
0011	Gain Adjust	**register D7:D0**	10000000		11111111	00000000	0.004 dB
		parameter value	0 dB		+0.5 dB	–0.5 dB	

Table 4-8. 3WSI Settings (Continued)

Address	Description		Default Value	Recommended Value	Max Value	Min Value	Step
0100	Offset Adjust	**register D7:D0**	10000000		11111111	00000000	156 µV
		parameter value	0mV		+20mV	–20mV	
0110	State Register	**register D9:D0**	0000000000	See description hereafter			

Notes: 1. It is recommended to adjust clock duty cycle at 35/65% to optimize SFDR and THD at high sampling rate in 2nd Nyquist zone.
2. It is recommended to adjust clock adjust to +30 ps to optimize SNR in 2nd Nyquist zone if not used in interleaving mode.
3. SDA Coarse & SDA fine: Total possible = total Coarse + total Fine = 90 + 30 ps = 120 ps

Table 4-9. State Register Description

Setting for Address :0110	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mode SDA OFF	X	X	X	X	X	X	0	X	X	X
Mode SDA ON	X	X	X	X	X	X	1	X	X	X
Mode binary output	X	X	X	X	0	X	X	X	X	X
Mode gray output	X	X	X	X	1	X	X	X	X	X
Two's complement OFF	X	X	X	0	0	X	X	X	X	X
Two's Complement ON	X	X	X	1	0	X	X	X	X	X
Data Ready Reset (DRR) inactive High	X	0	X	X	X	X	X	X	X	X
Data Ready Reset (DRR) inactive Low	X	1	X	X	X	X	X	X	X	X
NAP Mode OFF	0	X	X	X	X	X	X	X	X	X
NAP mode ON	1	X	X	X	X	X	X	X	X	X

Comments:

1. SDA Mode: to take into account the value of the Sampling Delay Adjust register, bit D3 of the state register should be asserted to 1. For applications requiring extremely low clock jitter and no interleaving of several ADCs, it is recommended to assert bits D3 of state register to 0.
2. NAP mode of the ADC part reduces its power dissipation (in standby mode, both terminations of the differential data output buffers of the ADC are driven at same value).

4.5.4 NAP Mode

The NAP mode is controlled via the 3WSI serial interface, reducing the ADC power dissipation by 0.9W.

When the device is not used, minimal Power consumption for the combined ADC and 1:4 DMUX chips is obtained by turning on the NAP mode (on ADC part) and the SLEEP mode (DMUX) simultaneously.

4.5.5 Binary or Gray Output Mode

It is possible for the user to choose between the Binary or Gray output data format. Gray coding may be used in order to reduce the effect of BER when occurring, by storing Gray output codes.

Digital Data format selection is made using the 3WSI (default selection is Binary), programming the state register at address "0110".

Binary two's complement is also available asserting bit D6 at 1 of state register at address "0110".(only taken in account if bit D5 is asserted at 0, i.e. in Binary output mode).

4.5.6 Sampling Delay Adjust Function (SDA) – ADC Interleaving

This function is of most importance for applications based on time interleaving of multiple ADCs, in order to increase the actual sampling rate. In interleaved system the channels relative phasing has to be matched finely to avoid intermodulation spurs. The SDA function is monitored through the 3 Wire Serial Interface (3WSI), for remote fine alignment of ADC Aperture delays.

The SDA fine tuning has to be done after proper alignment of ADC Gains and Offsets, also monitored by the 3WSI.

A control voltage is applied on the tunable delay line, through embedded control DACs: 2 Bit DAC (coarse tuning) and 8 Bit DAC (fine tuning). The coarse 2 Bit DAC allows for coarse alignment of the ADCs aperture delays, with a step (resolution) of 30 ps. The 8 Bit control DACs allows for fine phase alignment of ADCs, with a resolution of 30 ps/256 = 117 fs. This is more than enough for very fine phase alignment of multiple ADCs. Once tuned, the ADCs track each other versus temperature.

It is reminded that the ADC intrinsic jitter is 120 fs rms, (with SDA = OFF).

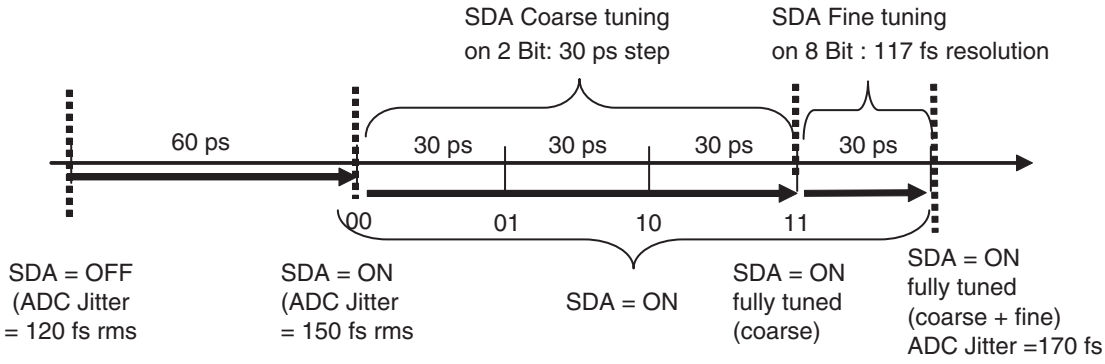
The sampling delay adjust enables a tuning of the aperture delay of each channel over a range of 120 ps with a first coarse tuning over a range of 90 ps and then a fine tuning on 8 bit over a range of 30 ps for better accuracy of the settings.

It is pointed out that the ADC intrinsic jitter is 120 fs rms if SDA is turned OFF, and becomes 150 fs rms if SDA is turned ON, and 170 fs rms if SDA is fully tuned. This is related to extra delay cells in the sampling clock path, which are bypassed if SDA is OFF. If the SDA is turned on, an amount of + 60 ps extra time delay adds onto the sampling clock path.

For reference, the measured SNR at Fin = 2500 MHz (–1 dBFS) is 50 dB with SDA = OFF, 49.2 dB with SDA turned on, and 48.5 dB with SDA turned ON and fully tuned.

For optimum dynamic performance (low jitter), it is recommended to disable SDA (Mode SDA OFF).

Figure 4-14. Programming the SDA Tunable Delay Line Through the 3WSI



4.5.7 ADC Gain Control

The 3-Wire bus interface also allows for adjusting the gain by enabling a fine tuning by ±0.5 dB and an 8-bit resolution.

4.5.8 Offset Control

The 3WSI allows to control the offset of the ADC with a tuning range of ± 20mV, and an 8 bit resolution.

An accurate tuning of aperture delay, gain and offset allows to interleave two ADCs with minimum number of external analog components, thus providing an equivalent 5 Gsps ADC. Due to matching difficulties of the roll off of the input frequency response beyond 4 GHz, it is not recommended to use the ADC in interleaved mode for coding of broadband signal beyond 4 GHz.

4.6 Die Junction Temperature Monitoring

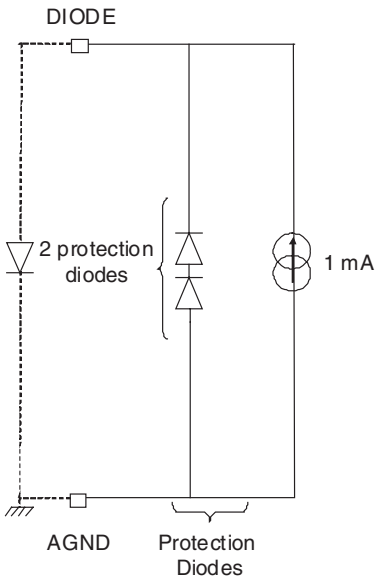
A die junction temperature measurement setting is available, for maximum junction temperature monitoring (hot point measurement).

The measurement method consists in forcing a 1 mA current into a diode mounted transistor and sensing the voltage across the DIODE pin and the closest available ground pin.

The measurement setup is described in the Figure hereafter:

Note: If not used, DIODE pin can be left floating.

Figure 4-15. ADC Diode for Die Junction Temperature Monitoring Setup (2 Reverse Diodes for Protection)

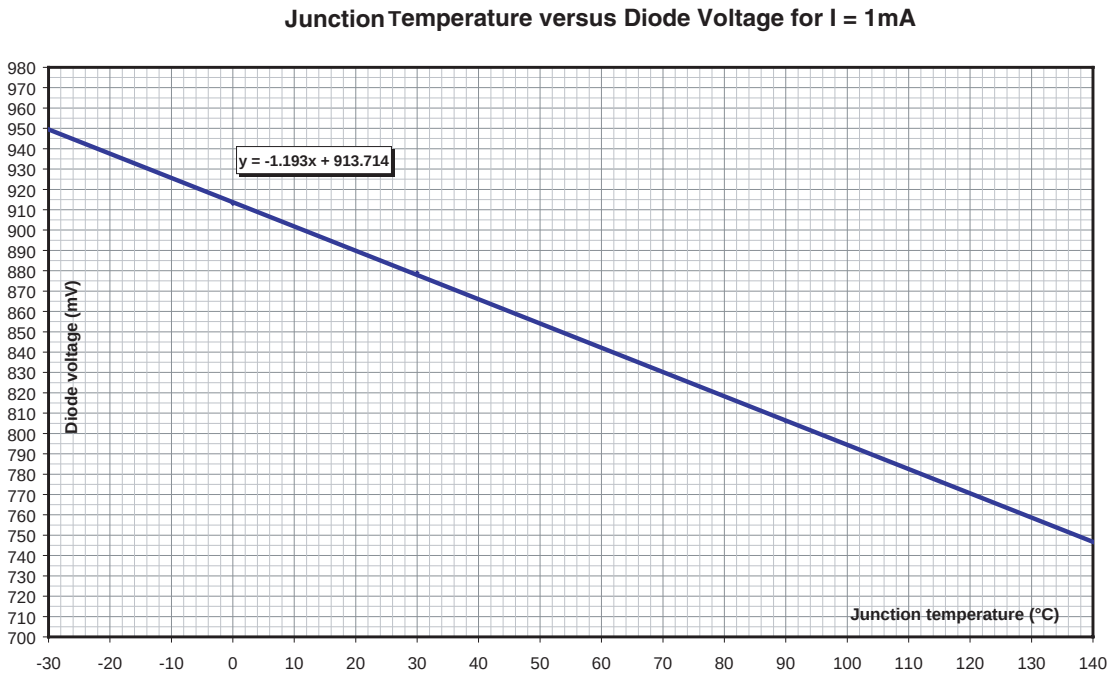


CAUTION:

Respect the current source polarity and the current flow of 1 mA through the diode.

The forward voltage drop (V_{DIODE}) across diode component, versus junction temperature, (including chip parasitic resistance), is given below (I_{DIODE} = 1mA).

Figure 4-16. Junction Temperature Versus Diode Voltage for I = 1 mA



5. Applications Information

5.1 Bypassing, Decoupling and Grounding

5.1.1 Decoupling capacitor

Globally, the ADC is decoupled following a four row decoupling capacitors strategy, providing adequate decoupling over frequency taking into account the external decoupling: at Evaluation Board and Package surrounding level, and the internal ADC decoupling (transparent for the end-user): at internal Package decoupling and on chip decoupling level.

ADC **external** decoupling: typical values

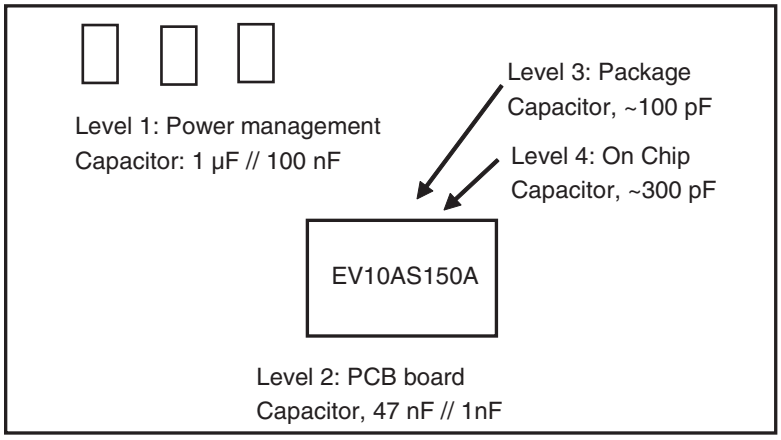
1. At Evaluation Board incoming level: (1st level): ~ 1 µF (tantalum) in parallel with ~ 100 nF chip capacitor.
2. Close to Package surrounding: 2nd level: 144 nF per analog supply (V_{CCA5} & V_{CCA3}), 192 nF for V_{CCD} and 288 nF for V_{PLUSD}.

It is recommended to decouple all power supplies to ground as close as possible to the device balls.

ADC **internal** decoupling: typical values

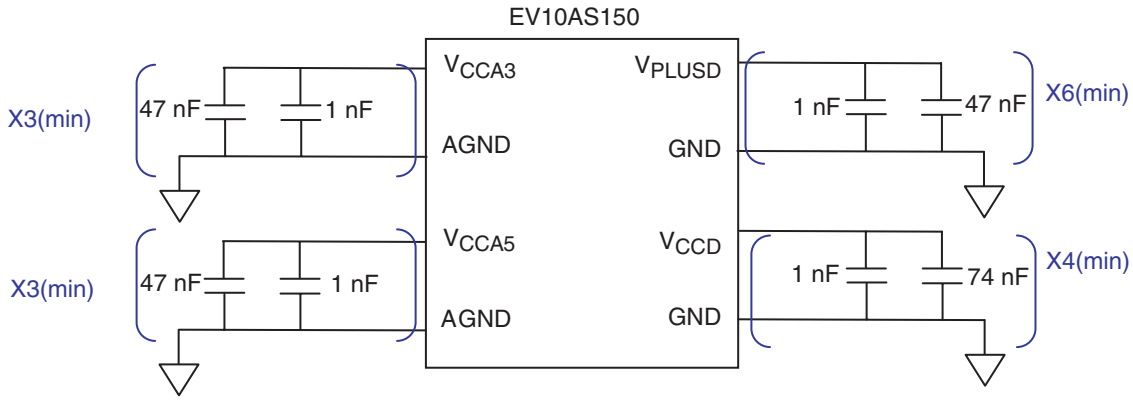
3. Inside Package: (3rd level): 100 pF per power supply plane to ground plane.
4. On chip decoupling level: (4th level): nearly 300 pF per power supplies.

Figure 5-1. EV10AS150A Decoupling Schema



5.1.2 Power Supplies Decoupling Schema

Figure 5-2. Power Supplies Decoupling Schema



5.1.3 Decoupling Capacitors Package Implementation

The table below indicates the pins to pins connected together with a pair of decoupling capacitance (47 nF // 1 nF).

Table 5-1. Decoupling Capacitors Implementation

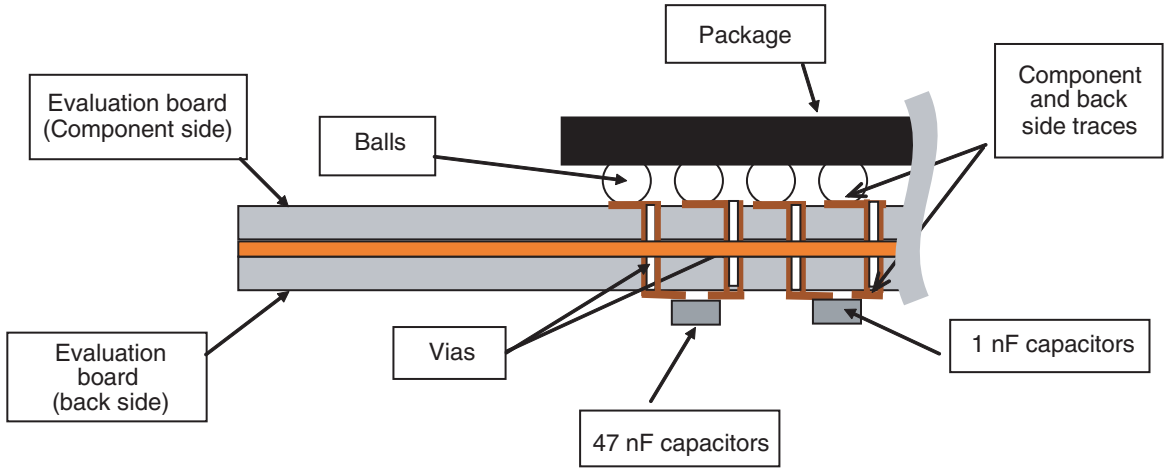
Supply	Total decoupling per supply	List of pins to be connected together with 47 nf // 1 nF
V_{CCA5}	144 nF	A27, A26, A24, B27, B26, B24, C27, C26, C24, D27, D26, D24, E26, E24, F25
V_{CCA5}		L26, L25, M27
V_{CCA5}		R21, T21, U21
V_{CCA3}	144 nF	A25, B25, B22, C25, C22, C20, D25, D22, D20, E25, E22, E20, F24, F22, F20
V_{CCA3}		R20, T20
V_{CCA3}		K26, K25,L27, M26, M25, N26, N27

Table 5-1. Decoupling Capacitors Implementation (Continued)

Supply	Total decoupling per supply	List of pins to be connected together with 47 nf // 1 nF
V_{PLUSD}	288 nF	C19, C16, C15, C14, C13, D19, D13, E19, F19
V_{PLUSD}		T15, T14, T13, U15, U14, U13
V_{PLUSD}		C11, C9, C7, C6, C5, D11, D9, D7, D6, D5
V_{PLUSD}		T11, T9, T7, T6, U11, U9, U7, U6, U5
V_{PLUSD}		C4, E3, J4, J3
V_{PLUSD}		L4, L3, N4, N3, R4, R3, U4
V_{CCD}	192 nF	C12, C10, C8, D16, D12, D10, D8, E17
V_{CCD}		D4, D3, E4, G4, G3
V_{CCD}		K4, K3, T4, T3, U3
V_{CCD}		R16, T17, T16, T12, T10, T8, T5, U12, U10, U8

5.1.4 Decoupling Capacitors PCB Implementation

Figure 5-3. Decoupling Capacitors PCB Implementation



5.1.5 Power Plane (Analog and Digital)

For performance reasons it is always recommend to use separate supplies for digital and analog circuitry.

The digital supply should only be used for parts placed over the digital ground plane, i.e. all pure digital parts. The analog supply is used for all analog and mixed-signal parts.

Analog supplies ➔ V_{CCA3} and V_{CCA5}

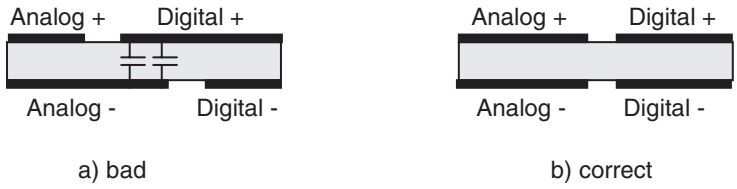
Digital supplies ➔ V_{PLUSD} and V_{CCD}

V_{PLUSD} supply must be isolated from analog supplies

Note: V_{PLUSD} supply is dedicated to digital output buffer only

It is important that a digital power plane does not overlap an analog power plane as can be seen on Figure 5-4 a). If this constraint is not respected, this will induce capacitance between the overlapping areas, which is likely to cause RF emissions to pass from one plane to another.

Figure 5-4. Overlapping of Analog and Digital Planes



Power planes are designed using the same rules as ground planes. Keep the analog supply plane entirely under the analog ground plane, see on Figure 5-4 on page 50. This gives an analog supply plane over the analog ground plane and a digital supply plane over the digital ground plane. In this case, it could not cause unwanted capacitance between the two planes.

Moreover, power supply pins should be decoupled directly to the ground plane. The ceramic capacitor should be located as close as possible to the IC power pins.

The sampling clock generation circuitry should be treated like analog circuitry and also be grounded and heavily-decoupled to the analog ground plane. It also should be isolated from noisy digital circuits.

So, the ground plane not only acts a low impedance return path for decoupling high frequency currents but also minimizes RF emissions. Because of the shielding action of the ground plane, the circuit's susceptibility to external RF is also reduced.

The optimum partitioning for Analog and Digital Power and Ground planes is illustrated in Figure 5-5 on page 51.

The isolation between FPGA Ground plane and DGND of ADC is recommended but not mandatory, depending on switching noise level which may be injected by FPGA.

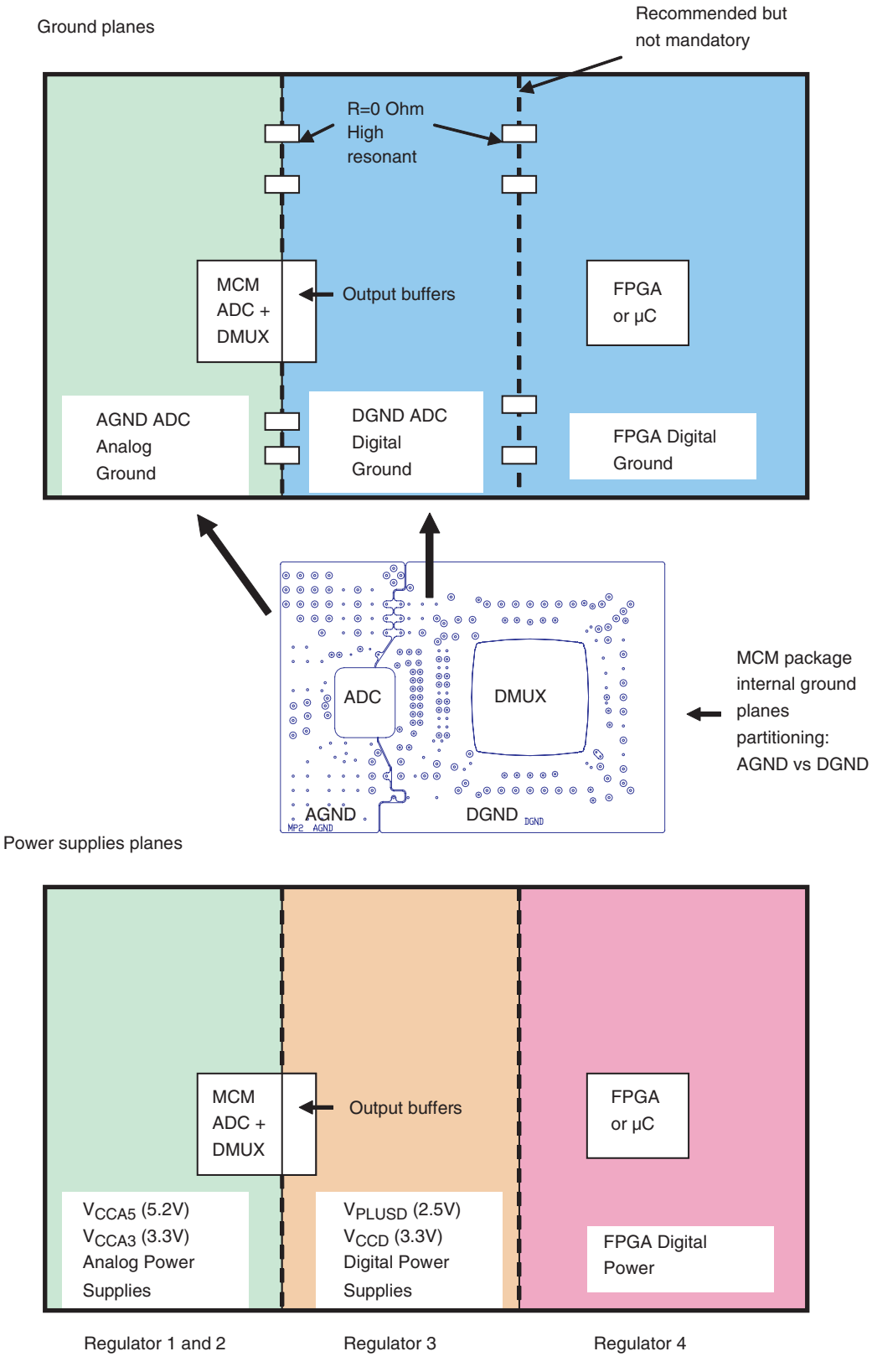
The AGND and DGND shall be DC connected together by a 0 ohm resistor, and making use of the parasitic (high resonant) inductance of the resistor element to reject the HF spikes. Same DC connection shall be between DGND of ADC and DGND of FPGA if used.

This recommendation for optimum isolation must be followed carefully for optimum rejection of Fclk/4 clock spur in 1:4 DMUX mode.

DGND is only allocated to Output Buffers of ADC and digital section + Digital output buffers of 1:4 DMUX. AGND ground plane is allocated to ADC only, and needs to be isolated from 1:4 DMUX output buffers switching into 40 differential 100Ω terminations. Switching Noise is mainly generated by back reflection effects due to L,C parasitics of 100Ω terminations. This leads to switching noise into V_{PLUSD} and DGND which gives energy to Fclk/4 clock related spur if fed back to the ADC Ground.

As digital output buffers are of main concern, we essentially have to concentrate on V_{PLUSD} and DGND layout. V_{PLUSD} power plane shall not overlap with AGND ground plane and other analog power supplies planes (V_{CCA5}, V_{CCA3}). Coupling with VCCD is less critical since allocated to the Digital DMUX only, not to the ADC analog section.

Figure 5-5. Analog and Digital Partitioning of Power and Ground Planes for Optimum Isolation



5.2 Analog Input Implementation

5.2.1 ADC Analog Input Terminations

The front-end input preamplifier in on chip terminated (100Ω differential, 50Ω single-ended with accurate thin film TaN resistors with temperature coefficient close to 0°C), driven by 50Ω controlled impedance lines (100 Ω differential) with the multilayer EBGA317 Package.

This allows flat input Voltage Standing Wave Ratio (VSWR) over frequency, (< 1.25:1 measured for packaged ADC, from DC up to 3 GHz (less than 1.3% of incoming power reflected from the ADC input, < 0.05 dB transmission loss), and < 1.5:1 from 3 GHz to 5 GHz Full power input bandwidth of the ADC (less than 4% of power reflected from ADC input, < 0.17 dB transmission loss).

The low input VSWR together with the 5 GHz (–3 dB) full power input Bandwidth of the ADC, allows operation up to the 3rd Nyquist region (including L_Band and S_Band) with negligible carrier level fluctuations related to packaged ADC input impedance deviation from ideal Z = 50Ω (including package parasitics).

The on-chip terminations (in-phase V_{IN} and inverted phase V_{INN}) are actually based on a resistive voltage splitter of 55Ω + 550Ω biased under +3.3V to ground, providing proper 50Ω termination (550 // 55 = 50), together with 3V internal DC common mode biasing. Since the internal analog input DC common mode is +3V, the differential Analog inputs shall be driven through high resonant (> 5 GHz) DC blocking capacitors.

Driving the EV10AS150A in single-ended for ADC Full Scale voltage span:
If single-ended driven, the applied in-phase (V_{IN}) input voltage amplitude for ADC full-scale voltage span is 0.5V peak-to-peak, (i.e. –2 dBm Full Scale input power into 50Ω on-chip termination.)

For proper symmetric input impedance matching, the inverted phase input (V_{INN}) must be externally terminated by 50Ω to Ground through a DC blocking chip capacitor. The inverted phase (V_{INN}) is internally on-chip 50Ω terminated and biased the same way as the in-phase analogue input.

Driving the EV10AS150A in differential for ADC Full Scale voltage span:
If entered in differential, each analog input (in-phase V_{IN} and inverted phase V_{INN}) shall be entered with ±0.125V peak = 0.25V peak-to-peak amplitude, to comply with 0.5V ADC Full Scale voltage span.

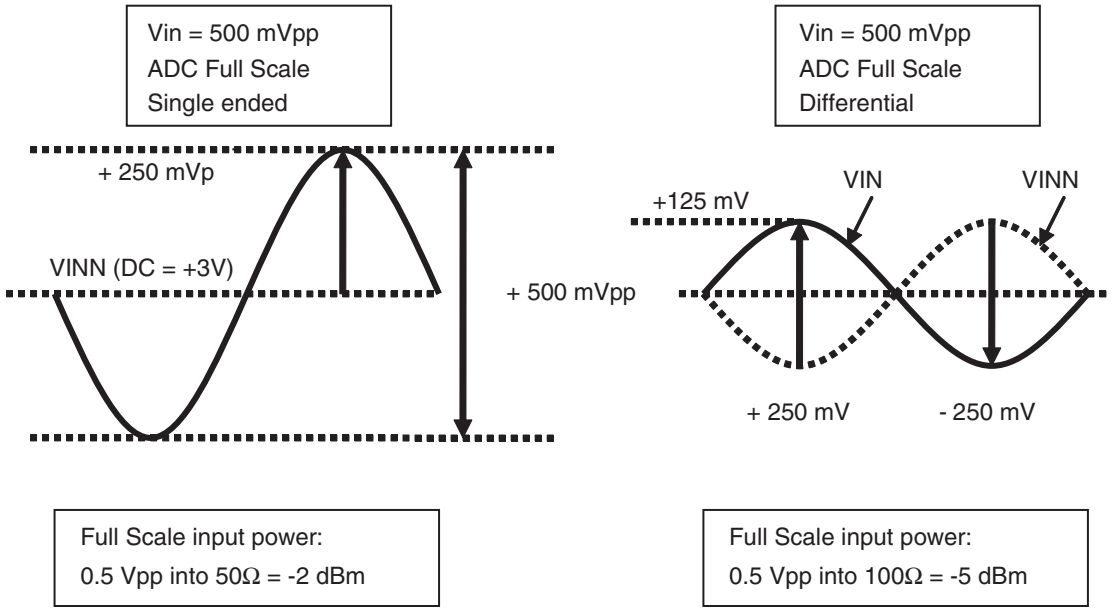
Since the 0.5Vpp Full Scale input voltage span is applied onto 100Ω termination instead of 50Ω, the ADC Full Scale differential input power into 100Ω loading is –5 dBm instead of –2 dBm into 50Ω if single-ended driven.

Low cost low profile sub-miniature unbalanced to balanced transformers (baluns) are commercially available, designed specifically for driving differential inputs and/or output locations for fast sampling ADCs in the GHz range. These baluns are providing 50Ω impedance on unbalanced input, and 100Ω impedance on the balanced differential output port, making it easy to use on surface mount application boards to drive AC coupled differential Analog inputs and clock inputs.

For optimum SFDR performance, the maximum phase balance shall not exceed 12 degree and less than 1.5 dB for amplitude balance, over the entire band of operation. For example, for operation over the 2nd Nyquist region at 2.5 Gsps, baluns featuring less than 6 degree Phase Balance and 1 dB amplitude Balance within a band of operation of 1.6 GHz to 3 GHz are available (for roughly 1 dB insertion loss). Baluns covering a larger band of operation (e.g. 400 MHz to 3000 MHz) with 12 degrees max Phase unbalance and 1.5 dB Amplitude Balance are also convenient.

Since the ADC tolerates up to 12 degrees of phase unbalance without impacting the dynamic performance (SFDR), it is not mandatory to use cascaded (double) transformer to improve phase balance characteristics. Double transformer implementations may degrade the inherent band flatness of the device with additional insertion loss.

Figure 5-6. ADC Full Scale Single Ended vs. Differential Analog Input



5.2.2 Differential Versus Single-ended Input Dynamic Performance (SNR, SFDR, THD)

The EV10AS150A implements a front-end Track and Hold preamplifier which has been designed in order to be entered either in differential or single-ended, up to maximum operating sampling rate without significant loss in dynamic performance in either 1st and 2nd Nyquist for large signals close to ADC Full Scale:

Same SNR values are measured in single-ended and differential, 1st and 2nd Nyquist (delta SNR < 0.2 dB).

Regarding linearity performance (Total Harmonic Distortion (THD) and Spurious Free Dynamic Range (SFDR)):

- If differential driven, it is the odd Harmonics (mainly H3) which mainly dictates the ADC large signal linearity performance (SFDR and THD), whereas the even harmonics (H2, H4, …) only little contributes to THD.
- In single-ended driven, the even harmonics (H2, H4, …) will become significant with the same weighting as the odd Harmonics (H3,H5,…). The 2nd Harmonic will rise to the same level as 3rd Harmonic, mainly in the 2nd Nyquist.
  The EV10AS150A front-end preamplifier has been boosted to maintain the 2nd Harmonic (H2) level below –60 dBFS in single-ended over 1st and 2nd Nyquist, even for large signals close to ADC Full Scale. Since the 2nd harmonic weighting is not higher than the 3rd Harmonic level (H3), the SFDR performance will not be impacted.

However, the THD will be somewhat impacted, since the harmonics are RSS summed since even and odd harmonics have now similar weightings in single-ended:
The THD is slightly impacted by –1 dB in the 1st Nyquist, and –2 dB in the 2nd Nyquist (Fin < 3000 MHz).
In the 3rd Nyquist for large signals close to ADC Full Scale, (e.g. Fin = 4000 MHz, –1 dBFS), the 2nd Harmonic impact on THD in single-ended will become much more important (H2 = + 6 dB versus differential mode):
Therefore in the 3rd Nyquist, it is highly recommended to drive the inputs in differential for optimum Spurious Free Dynamic Range (SFDR) and optimum total harmonic distortion performance (THD).
Note: For THD computation, the 10 1st low rank harmonics are taken into account.

5.2.3 Differential versus Single-ended Input: Rejection for Fclk/4 Spurs

If the 1:4 DMUX Ratio is selected, the rejection of the Fclk/4 clock related spur becomes an issue since the clock spur is located at the middle of the Nyquist zone.

With 1:2 DMUX Ratio, the clock related spur is located at Fclk/2, and does not affect the center of the band of operation.

The rejection of Fclk/4 becomes 6 dB more efficient if the ADC is differentially driven. (A delta of –6 dB is measured in differential vs. single-ended for the Fclk/4 level).

On EV10AS150A evaluation board, the measured Fclk/4 level is:

- –72 dBFS in single-ended, corresponding to –74 dBm with –2 dBm Full Scale input power (0.5Vpp in 50Ω).
- –78 dBFS in differential, corresponding to –82 dBm with –5 dBm Full Scale input power (0.5Vpp in 100Ω).

The ADC has been carefully implemented at chip layout level and packaging level to ensure maximum electric isolation between the noisy Digital output buffers Section and Analog sections of the ADC. (Analog sections include the logic section and the timing circuitry of the ADC).

At application board level:

The absolute value for Fclk/4 in either single-ended or differential mode can be even further improved by improving the electric isolation of the +2.5V power supply: The +2.5V Power plane dedicated to the 40 Digital Output Buffers drives most of the Fclk/4 switching noise energy, and has to be isolated from the other remaining power supplies.

Refer to Figure 5-5 on page 51 for board layout recommendation for optimum isolation.

5.3 Clock Input Implementation

The EV10AS150A differential clock input buffer is based on fast regeneration amplifiers, in order to feature a square wave like sampling clock for the Track and Hold, featuring very fast internal slew-rates to ensure low internal sampling jitter.

The EV10AS150A differential clock input buffer is on-chip 100Ω terminated (50Ω on each single-ended clock input).

The clock input buffer is biased in the same way as the differential analog input preamplifier:

The differential on-chip clock inputs terminations are based on resistive 55Ω + 550Ω voltage splitter biased under +3.3V to Ground, providing 5Ω impedance (550Ω // 55Ω = 50Ω) together with 3V internal DC common mode biasing for both inputs.

5.3.1 Driving the EV10AS150A with a Sinewave Clock Input

The SNR rolloff in the high input frequency region (2nd and 3rd Nyquist) is dictated by sampling jitter:

The ADC sampling jitter is 120 fs rms, to be RSS summed with external sampling clock jitter:

To achieve optimum SNR in the 2nd Nyquist (e.g; SNR > 48 dB at Fin = 3000 MHz, the external clock sinewave requirements are mainly two-fold:

The external sinewave clock signal phase noise and clock signal slew-rate.

The Single Side Band (SSB) phase noise floor of the reference sinewave clock signal shall not exceed 155 dBc/Hz (at 1 MHz from carrier).

The slew-rate of the 2.5 GHz clock input shall not be lower than 5 GV/s at 2.5 GHz frequency.

Accordingly, at 2.5 GHz sampling clock frequency, a sinewave clock input can be directly entered provided the sinewave amplitude is 0.632 Vpp minimum into the 100Ω differential output to ensure 5 GV/s minimum slew-rate, and 155 dBc/Hz phase noise floor.

Sinewave Clock slew-rate effect on SNR:

Due to very fast internal slew-rates of regeneration stages, a sinewave clock can be entered without impacting the SNR so far the sinewave slew-rate is higher than 5 GV/s minimum (8 GV/s recommended).

These fast slewing front-end clock buffer regeneration stages provides lowest internal rms time domain jitter, as illustrated by the following relationship:

Rms(time jitter) = Rms(voltage noise) / Rms(slew-rate)

Assuming the ADC clock input is driven by a transformer (single-ended unbalanced 50Ω to balanced 100Ω differential), the minimum clock input power shall not be lower than –3 dBm into 50Ω input impedance = 0.45 Vpp at transformer input yielding 0.45 Vpp.SQRT(2) = 0.632 Vpp across 100Ω differential outputs applied to the ADC.

A minimum swing of 0.632 Vpp at 2.5 GHz corresponds to a minimum slew-rate of nearly 5 GV/s at 2.5 GHz.

Therefore, the 2.5 GHz external sinewave clock signal voltage amplitude applied across the 100Ω termination shall not be lower than 0.632 Vpeak to peak for optimum SNR performance in the 1st and 2nd Nyquist.

For sinewave clock frequencies lower than 2.5 GHz, the sinewave amplitude shall be increased accordingly, to preserve the minimum slew-rate of 5 GV/s, without exceeding 2 Vpp maximum operating amplitude applied to the differential clock input. For example, with a 1.25 GHz sinewave clock, to keep the same slew-rate of 5 GV/s, the minimum voltage amplitude to be applied to the ADC clock input shall not be lower than 2 × 0.632 Vpp = 1.264 Vpp across the 100Ω differential clock inputs, corresponding to + 3 dBm into 50Ω transformer input (which is twice the clock input power of a 2.5 GHz sinewave input).

Typical recommended clock input power for a 2.5 GHz sinewave clock for optimum SNR over full temperature range shall be +1 dBm into 50Ω transformer input impedance, which corresponds to 0.710 Vpp.SQRT(2) = 1 Vpp across 100Ω across differential outputs applied to the ADC clock inputs. This corresponds to a slew-rate of 7.85 GV/s at 2.5 GHz.

Therefore, typical recommended slew-rates to ensure flat SNR over operating temperature range shall be in the range of 8 GV/s.

Maximum operating clock input power shall not exceed + 7 dBm, which corresponds to 2 Vpp on differential 100Ω clock input. This corresponds to slew-rates of 15.7 GV/s

Maximum ratings for differential clock input is 3 Vpp which corresponds nearly to +11 dBm maximum clock input power.

Sinewave Clock Phase noise vs. time domain jitter effect on SNR rolloff at high input frequencies:

The SNR due to ADC intrinsic clock jitter contribution only (i.e. 120 fs rms), excluding external clock source jitter (jitter free external clock source), is 50 dB at Fin = 2500 MHz, –1 dBFS.

Taking into account the external clock source time domain jitter contribution on SNR performance, the ADC intrinsic clock jitter of 120 fs rms has to be RSS summed to the external rms clock jitter, yielding to total sampling clock Jitter:

For example with a 100 fs rms external clock source jitter, the total sampling clock jitter will be $SQRT(120^2 + 100^2) = 156$ fs rms.

With a 120 fs rms clock source jitter, the total jitter will be 170 fs rms:

For the EV10AS150A, the measured SNR at Fin = 2500 MHz for –1 dBFS analog input amplitude is 50 dB with a jitter free external clock source, (taking only into account the ADC intrinsic jitter of 120 fs rms). With 120 fs rms external clock source time domain jitter RSS summed with the 120 fs rms intrinsic ADC clock jitter, (leading to 170 fs rms total jitter), the measured SNR becomes 48.5 dB.

Relationship between sinewave clock source phase noise and time domain jitter:

The 100 fs rms external time domain jitter corresponds approximately to an external sinewave clock source with (white) phase noise floor spectral density of 155 dBc / Hz, integrated from 1 MHz up to 5.5 GHz:

The 5.5 GHz upper limit of integration corresponds to the ADC clock input bandwidth. The 1 MHz lower limit of integration corresponds to the flat section of white phase noise, excluding 1/f and close in phase noise contribution for 1st order calculations.

The integration bandwidth for the phase noise floor is taken from 1 MHz up to 5.5 GHz ADC clock input bandwidth, leading to:
Integrated SSB phase noise floor spectral density: 155 dBc/Hz, 1 MHz to 5.5 GHz:
$–155 \text{ dB} + 10.\log(5.5.10^9 – 1.10^6) = –155 + 97.4 \text{ dB} = –57.6 \text{ dB}$.

This corresponds to the Single Side Band (SSB) phase noise power spectral density $10.\log(\text{Rad}^2/\text{Hz})$ expressed in dBc/Hz, integrated over nearly 5.5 GHz. The total integrated Double Side Band phase noise power expressed in radian (rms) is:

$SQRT\ (2.10^{-57.6\ /\ 10}) = 1{,}86.10^{-03}$ radians (rms).

In time domain, the rms jitter is obtained by dividing the total phase noise power (radians rms) by the carrier frequency.

For example, with a 2.5 GHz sinewave clock carrier, the time domain jitter will be $1{,}86.10^{-03}$ radians (rms) / $2.\pi.2{,}5$ GHz = ~ 118 fs rms

Therefore for a given constant phase noise floor, the external clock source time domain jitter will be slightly better when increasing clock frequency (due to faster signal slew-rate).

The 1/f phase noise contribution from 10 KHz to 1 MHz can be neglected so far the mean noise level in this region is below 130 dBc / Hz:

Integrated SSB mean phase noise spectral density: 130 dBc/Hz, 10 KHz to 1 MHz:

-130 dB + 10.log(10^6–10^4) = –130 + 60 dB = –70 dB

Integrated double SSB phase noise power in radians (rms):

SQRT($2.10^{-70\ /\ 10}$) = $0{,}447.10^{-03}$ radians (rms)

To be compared with $1{,}86.10^{-03}$ radians (rms) 155 dBc/Hz phase noise integrated over 5.5 GHz. The total RSS summed phase noise from 10KHz to 5.5 GHz is:

SQRT (($1{,}86.10^{-03}$ radians)2 + ($0{,}447.10^{-03}$ radians)^2) = $1{,}91.10^{-03}$ radians

Therefore the close-in phase contribution remains negligible. The close-in phase noise (1/f2 and 1/f3) contributions can also be neglected since this type of phase noise is related only to long term jitter drift effects which are not of concern here regarding the registration length of the Digital Data.

For example, considering the registration length time window for a 32K FFT at 2.5 Gsps:

32768x400 ps = 13.107 µs, corresponding to 76.3 KHz.

As a result, the close-in phase noise below 70 KHz has not to be taken into account for the integration. As a conclusion, considering a phase noise floor between 1 MHz and 5.5 GHz, any clock source phase noise floor better than 155 dBc/Hz will improve somewhat the SNR:

For example, a 160 dBc/Hz phase noise clock source will feature only 67 fs rms time domain jitter for a 2.5 GHz carrier, and a 165 dBc/Hz clock source will feature only 38 fs rms.

In these cases, the external clock source contribution to total jitter will be negligible, compared to the 120 fs rms intrinsic jitter of the ADC, and SNR performance in the 2nd and 3rd Nyquist will be improved.

Better SNR performance over frequency will then necessarily go through the improvement of intrinsic ADC jitter (< 50 fs rms for instance).

On the other hand, using a lower performance phase noise floor sinewave source will cause extra rolloff of the SNR in 2nd Nyquist region.

Example: 150 dBc/Hz phase noise will feature a time domain jitter of 188 fs rms time domain jitter for a 2.5 GHz carrier, and a 145 dBc/Hz phase noise will feature 375 fs rms time domain jitter at 2.5 GHz.

Therefore the impact on SNR (and therefore ENOB performance) for very high analog input frequencies is no more negligible against ADC intrinsic jitter, and the SNR performance will be impacted in these cases.

As a conclusion, the recommended phase noise floor shall be at least 155 dBc / Hz for optimum SNR performance over multiple Nyquist zones. Any improvement in phase noise floor will help to save a few dBs especially in the 2nd and 3rd Nyquist zones.

Note: If a fixed clock source can be used, (i.e.: non swept clock), the sinewave clock source can be band-pass filtered to further improve the phase noise floor.

5.3.2 Driving the EV10AS150A with a Square Wave Differential Cock Input

If the clock input signal is a square wave, the incoming signal slew-rate becomes independent to signal amplitude and frequency:
So far the slew-rate of the square clock signals is constant and controlled (> 5 GV/s), the SNR performance of the ADC will be independent to clock signal frequency and amplitude.
Consequently with square wave clock signals, much lower signal amplitudes and frequencies can be entered to the ADC as with sinewaves. With square waves, the SNR performance will be mainly dependant on time domain jitter, which shall remain below 100 fs rms, to ensure optimum SNR performance especially in the 2^{nd} and 3^{rd} Nyquist as detailed in the previous sections.

With a square wave clock input, a minimum amplitude of ±125 mV peak = 250 mVpp can be entered without impact on linearity (SFDR and THD) and SNR. LVDS logic compatible and LVPECL logic compatible clock inputs can therefore be used to drive the EV10AS150A ADC clock input, so far the time domain jitter of the square wave is < 100 fs rms, and slew-rate is < 5GV/s. So it is not actually the rise/fall time of the square wave clock signals which are of interest, but the actual Slew-rate of the clock edges.

For LVPECL square wave clock input featuring a typical rise time (20% to 80%) of 75 ps for 800 mV voltage swing, the corresponding signal slew-rate is roughly 500 mV/75 ps = 6.6 GV/s, which is convenient.

In addition to that, the time domain jitter shall be < 100 fs rms. (e.g.: 70 fs rms).

LVDS and/or LVPECL compatible low jitter regeneration signals Buffers are commercially available, featuring less than 100 fs rms time domain jitter.
Of course, the sinewave to square wave regeneration buffers shall be driven by a low phase noise sinewave reference clock source (> 155 dBc/Hz), as stated in the previous sections:
The additional jitter due to the square wave regeneration circuitry has then to be RSS summed to the driving sinewave signal time domain jitter (e.g.: 100 fs rms time domain jitter which are achieved by a 155 dBc/Hz sinewave clock source will have to be RSS summed with a 70 fs rms square wave jitter, yielding to $SQRT(100^2 + 70^2)$ = 122 fs rms total external jitter (sinewave & square wave).
In these conditions, the SNR performance of the ADC will be nearly 49 dB at Fin = 3000 MHz, (–1 dBFS at 2.5 Gsps). It is reminded that an SNR of 50 dB at (3000 MHz, –1 dBFS) is achieved if the external clock source jitter contribution can be neglected, only taking into account the 120 fs rms intrinsic sampling clock jitter of the ADC, assuming ideal (jitter-free) external clock sources with ultra fast slew-rates (> 10 GV/s).

Note 1: ADC Minimum sampling clock frequency:

The square wave clock input frequency shall not be lower than 500 MHz minimum, to avoid SNR and THD rolloff due to front-end Track and Hold droop rate. Recommended minimum value for clock frequency over temperature is 1 GHz to avoid any roll-off in dynamic performance.

Note 2: ADC SNR performance at low analog input frequencies:

The sampling clock jitter effect on SNR is negligible at low input frequencies (oversampling conditions).

The SNR performance for low input frequencies is mainly dictated by the ADC front-end Track and Hold input referred thermal noise integrated over the 5 GHz Analog input Bandwidth (times $\pi/2$ assuming 1^{st} order rolloff).

The measured SNR in oversampling conditions is 54 dB.

The ADC deviation from ideal quantification noise (Differential Non Linearity: DNL) on SNR performance is negligible compared to input referred thermal noise:
The measured Differential Non Linearity (DNL) is < 0.5 LSB peak (= 0.2 lsb rms) at 2.5 Gsps 1^{st} and 2^{nd} Nyquist, which is the same order of magnitude as quantification noise Q/SQRT(12).

Note 3: Effect of 3WSI SDA (Sampling Delay Adjust) tunable delay line on ADC intrinsic jitter

The previous assumptions are made with ADC intrinsic clock jitter = 120 fs rms, which is assuming the sampling clock adjust is de-activated (SDA OFF), which is the case by default setting at ADC Reset.
If multiple ADCs need to be interleaved, the respective Aperture delays of the ADCs need to be carefully aligned, and fine tuned with the “SDA” function monitored by the 3 Wire Serial Interface (3WSI), by activating the SDA function (SDA ON).

Turning “ON” the SDA will activate an internal tunable delay line in serial with the sampling clock path, (which is bypassed if SDA is turned OFF). By turning ON the SDA, the ADC intrinsic jitter becomes 150 fs rms (with minimum delay), since some additional extra delay cells will contribute to jitter, which will slightly impact the SNR performance by 1 dB at Fin = 2500 MHz. (50 dB with SDA turned OFF, and 49 dB if SDA is turned ON). If SDA is turned ON and fully tuned (maximum delay), the ADC intrinsic jitter becomes 170 fs rms.

Refer to chapter 4.6.6. for more information about Sampling Delay Adjust function.

5.4 LVDS Output Implementation

Output Data, Output Clock (Data Ready) and out-of-range bit are LVDS signals that needs to be 100Ω differentially terminated.

Output data:

- In-phase (Ai) and inverted phase (AiN) digital outputs on DEMUX Port A (with i = 0…9)
- In-phase (Bi) and inverted phase (BiN) digital outputs on DEMUX Port B (with i = 0…9)
- In-phase (Ci) and inverted phase (CiN) digital outputs on DEMUX Port C (with i = 0…9)
- In-phase (Di) and inverted phase (DiN) digital outputs on DEMUX Port D (with i = 0…9)

A0, B0, C0, D0 are the LSB, A9, B9, C9, D9 are the MSB

Output Clock (Data Ready)

- In-phase DR and inverted phase DRN.
- In-phase DRA and inverted phase DRAN on DEMUX Port A used in staggered mode.
- In-phase DRB and inverted phase DRBN on DEMUX Port B used in staggered mode.
- In-phase DRC and inverted phase DRCN on DEMUX Port C used in staggered mode.
- In-phase DRD and inverted phase DRDN on DEMUX Port D used in staggered mode.

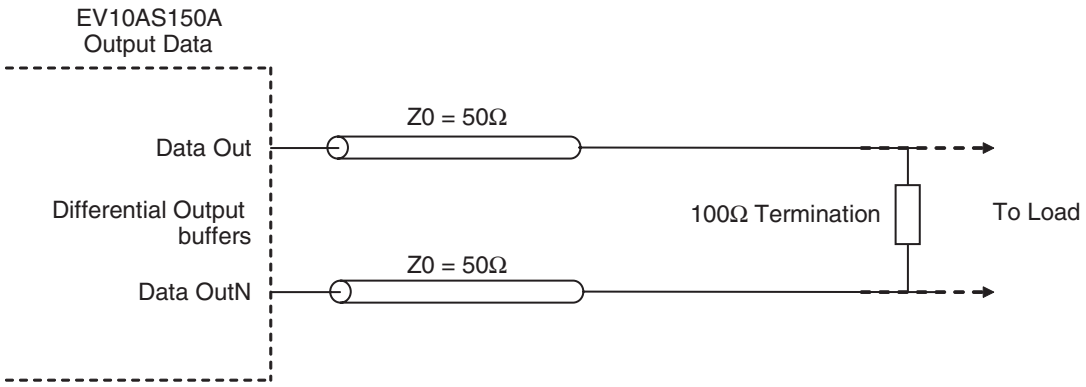
Out of Range

- In-phase AOR and inverted phase AORN on DEMUX Port A used in simultaneous mode.
- In-phase BOR and inverted phase BORN on DEMUX Port B used in simultaneous mode.
- In-phase COR and inverted phase CORN on DEMUX Port C used in simultaneous mode.
- In-phase DOR and inverted phase DORN on DEMUX Port D used in simultaneous mode.

Each of these outputs should be terminated by 100Ω differential resistor placed as close as possible to the differential receiver (inside receiver is even better).

In 1:2 DMUX Ratio the unused Output Data and out-of-range bit (Port C and D) could be leave floating without 100Ω differential resistor.

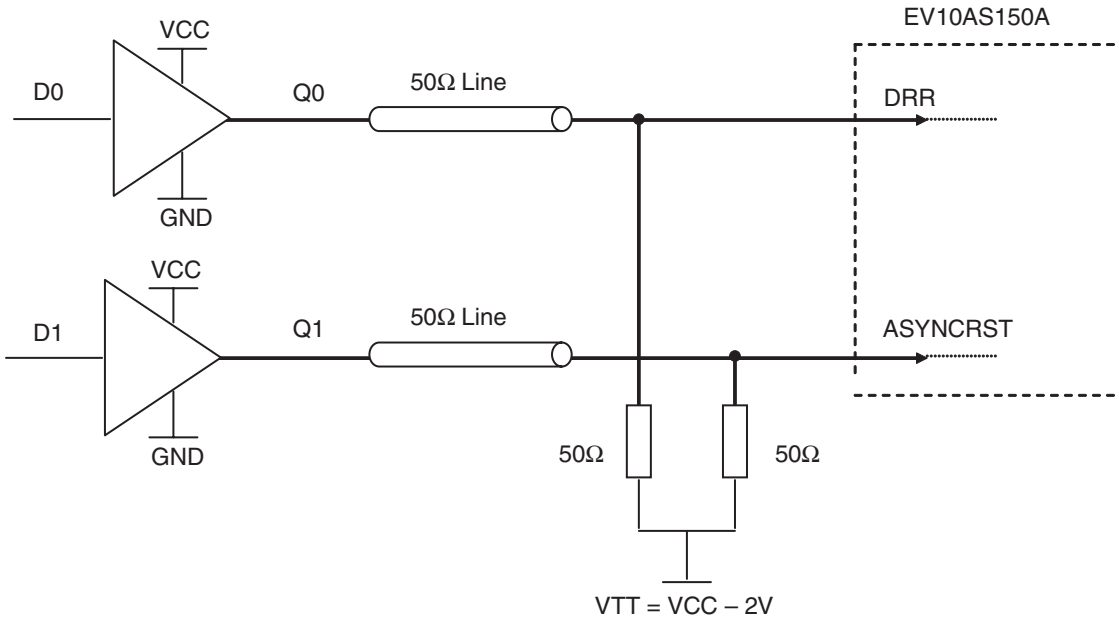
Figure 5-7. Differential Digital Outputs Terminations (100Ω LVDS)



5.5 DRR and ASYNCRST Implementation

50Ω termination of reset drivers need to be placed as close as possible of EV10AS150A ADC.

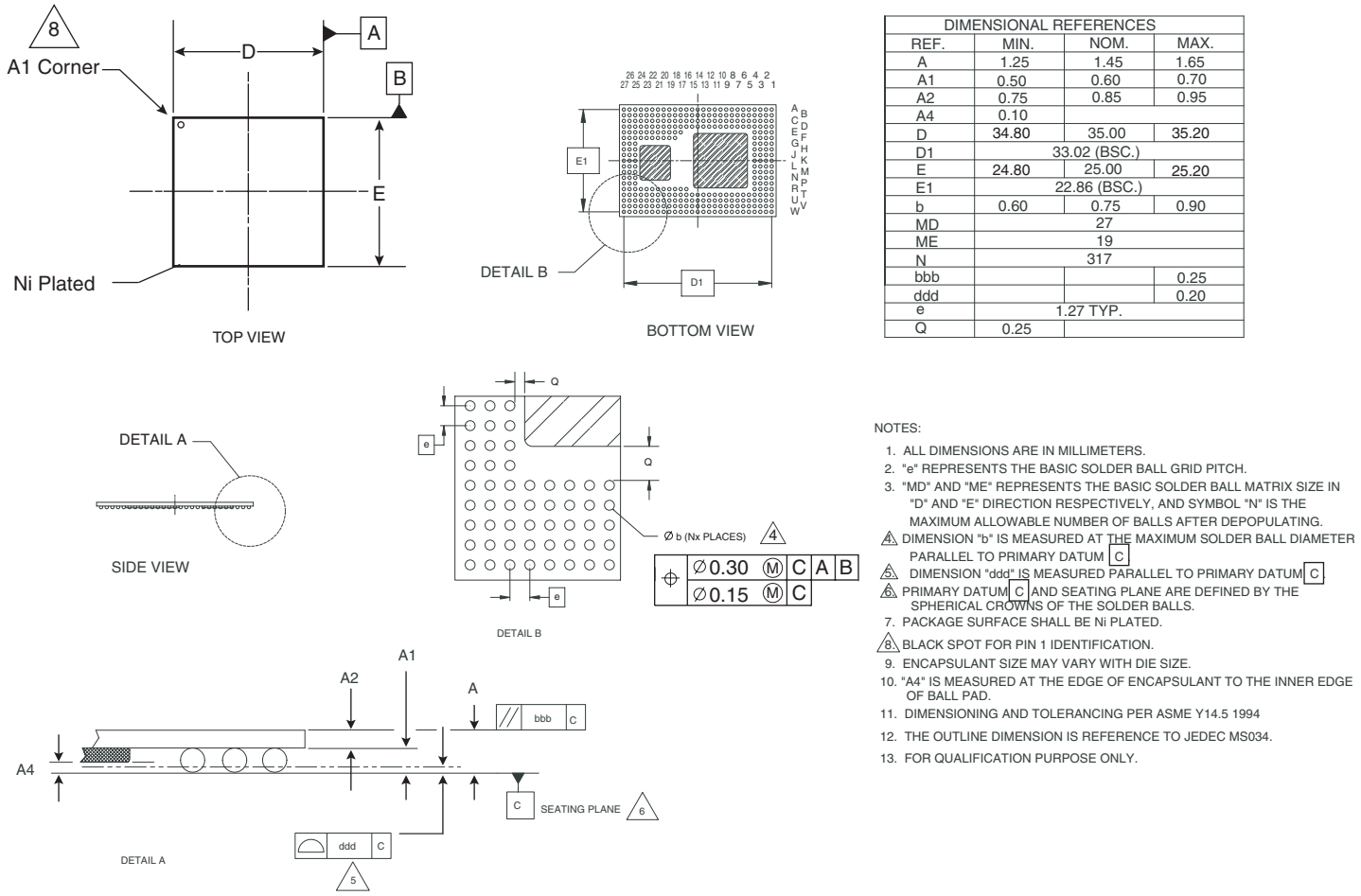
Figure 5-8. DRR and ASYNCRST Signals Implementation



6. Package Description

6.1 Package Outline

Figure 6-1. EBGA 317 Package Outline



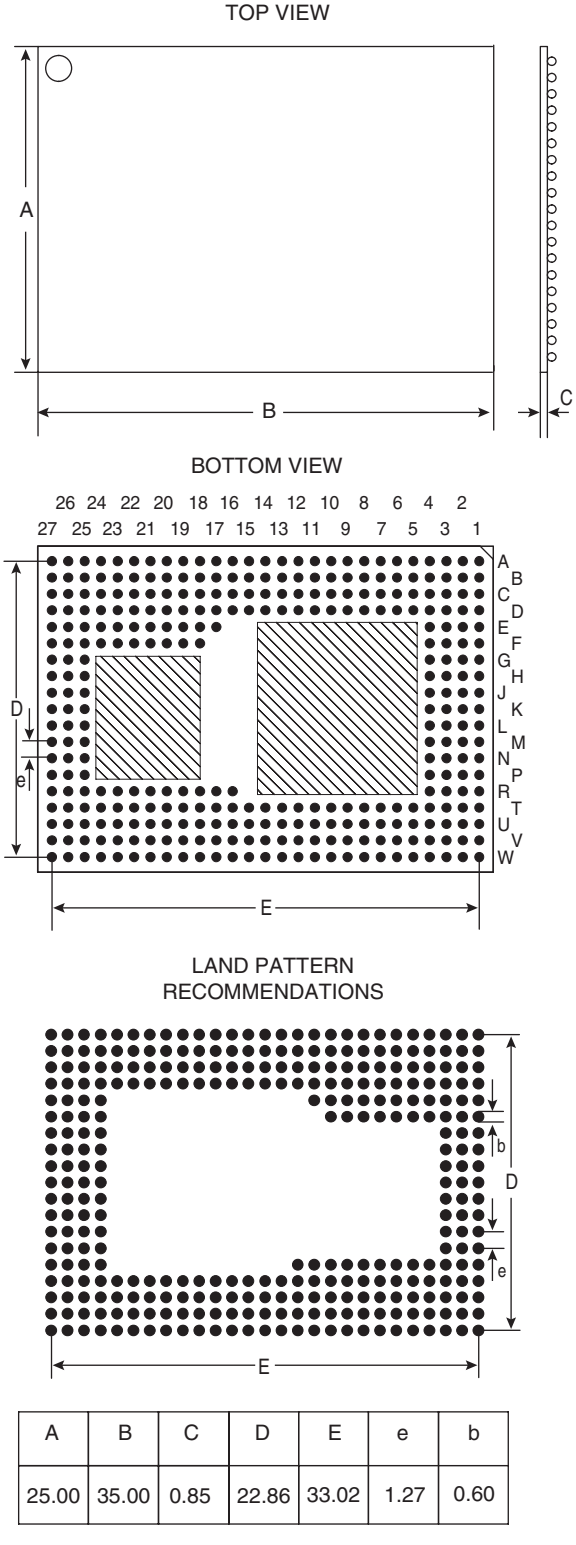
DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	1.25	1.45	1.65
A1	0.50	0.60	0.70
A2	0.75	0.85	0.95
A4	0.10		
D	34.80	35.00	35.20
D1	33.02 (BSC.)		
E	24.80	25.00	25.20
E1	22.86 (BSC.)		
b	0.60	0.75	0.90
MD	27		
ME	19		
N	317		
bbb			0.25
ddd			0.20
e	1.27 TYP.		
Q	0.25		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "MD" AND "ME" REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE IN "D" AND "E" DIRECTION RESPECTIVELY, AND SYMBOL "N" IS THE MAXIMUM ALLOWABLE NUMBER OF BALLS AFTER DEPOPULATING.
4. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C
5. DIMENSION "ddd" IS MEASURED PARALLEL TO PRIMARY DATUM C.
6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. PACKAGE SURFACE SHALL BE Ni PLATED.
8. BLACK SPOT FOR PIN 1 IDENTIFICATION.
9. ENCAPSULANT SIZE MAY VARY WITH DIE SIZE.
10. "A4" IS MEASURED AT THE EDGE OF ENCAPSULANT TO THE INNER EDGE OF BALL PAD.
11. DIMENSIONING AND TOLERANCING PER ASME Y14.5 1994
12. THE OUTLINE DIMENSION IS REFERENCE TO JEDEC MS034.
13. FOR QUALIFICATION PURPOSE ONLY.

6.2 Land Pattern Recommendation

Figure 6-2. EBGA 317 Land Pattern Recommendation



A	B	C	D	E	e	b
25.00	35.00	0.85	22.86	33.02	1.27	0.60

All dimensions are in millimeters

6.3 Thermal Characteristics

As there is no JEDEC standard definition for the thermal resistance applied to a multi-die device, only the thermal resistance for each die (ADC block powered ON only or DMUX block powered ON only) is provided.

All results were computed with ANSYS thermal simulation tool and with the following assumptions:

- Half geometry simulation
- ADC heating zone = 1.9 × 1.9 mm^2
- MUX heating 4.0 × 4.0 mm^2
- No air, pure conduction, no radiation

Table 6-1. Thermal Resistor

	Rth junction to bottom of balls	Rth junction to Top of Case	Rth junction to Board(1)	Rth junction to ambient
ADC block ON only	7°C/W	4.1°C/W	8°C/W	17.1°C/W
DMUX block ON only	3.9°C/W	1.5°C/W	4.9°C/W	13.9°C/W

Note: 1. Assumed board size = 53 × 43 mm^2.

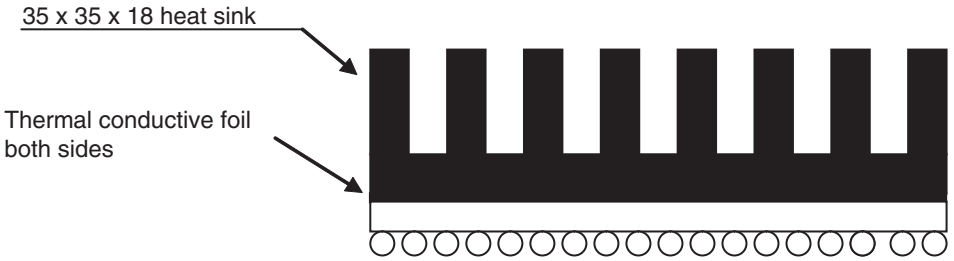
6.3.1 Thermal Management Recommendations

In still air and 25°C ambient temperature conditions, the maximum temperature of 106°C + 25°C = 131°C is reached for the ADC block. It is consequently necessary to manage heat from the EV10AS150 very carefully to avoid permanent damages of the device due to over temperature operation.

In no air cooling conditions, an external heatsink must be placed on top of package. An electrical isolation may be necessary as the TOP of the package is at ground potential.

It is advised to use an external heatsink with intrinsic thermal resistance better than 4°C/Watt when using air at room temperature 20–25°C. At 60°C, the external heatsink should have an intrinsic thermal resistance better than 3°C/Watt.

Figure 6-3. EV10AS150A-EB Evaluation Board Heat Sink Outlines



6.4 Moisture Characteristics

This device is sensitive to the moisture (MSL3 according to JEDEC standard). Its shelf life in sealed bag is 12 months at < 40°C and < 90% relative humidity (RH).

Once the bag is opened, devices that will be subjected to infrared reflow, vapor-phase reflow, or equivalent processing (peak package body temp. 260°C for ROHS versions and 220°C for non ROHS versions) must be:

- Mounted within 168 hours at factory conditions of ≤ 30°C/60% RH, or
- Stored at ≤ 20% RH

Before mounting, devices will require baking if the humidity indicator is > 20% when read at 23°C ± 5°C.

If baking is required, devices may be baked for:

- 192 hours at 40°C + 5°C/–0°C and < 5% RH for low-temperature device containers, or
- 24 hours at 125°C ± 5°C for high-temperature device containers

7. Ordering Information

Table 7-1. Ordering Information

Part Number	Package	Temperature	Screening	Comments
EVX10AS150ATP	EBGA317	Ambient	Prototype	
EV10AS150ACTP	EBGA317	Commercial grade 0°C < T_{amb}; T_J < 90°C	Standard	Production version
EV10AS150AVTP	EBGA317	Industrial grade –40°C < T_{amb}; T_J < 110°C	Standard	Production version
EV10AS150ACTPY	EBGA317 RoHS	Commercial grade 0°C < T_{amb}; T_J < 90°C	Standard	Production version
EV10AS150AVTPY	EBGA317 RoHS	Industrial grade –40°C < T_{amb}; T_J < 110°C	Standard	Production version
EV10AS150ATP-EB	EBGA317	Ambient	Prototype	Evaluation Board with soldered EVX10AS150ATP prototype in EBGA317 package

Table of Contents

How to reach us

Home page: www.e2v.com

Sales offices:

Europe Regional sales office

e2v ltd

106 Waterhouse Lane

Chelmsford Essex CM1 2QU

England

Tel: +44 (0)1245 493493

Fax: +44 (0)1245 492492

mailto: enquiries@e2v.com

e2v sas

16 Burospace

F-91572 Bièvres Cedex

France

Tel: +33 (0) 16019 5500

Fax: +33 (0) 16019 5529

mailto: enquiries-fr@e2v.com

e2v gmbh

Industriestraße 29

82194 Gröbenzell

Germany

Tel: +49 (0) 8142 41057-0

Fax: +49 (0) 8142 284547

mailto: enquiries-de@e2v.com

Americas

e2v inc

520 White Plains Road

Suite 450 Tarrytown, NY 10591

USA

Tel: +1 (914) 592 6050 or 1-800-342-5338,

Fax: +1 (914) 592-5148

mailto: enquiries-na@e2v.com

Asia Pacific

e2v ltd

11/F.,

Onfem Tower,

29 Wyndham Street,

Central, Hong Kong

Tel: +852 3679 364 8/9

Fax: +852 3583 1084

mailto: enquiries-ap@e2v.com

Product Contact:

e2v

Avenue de Rochepleine

BP 123 - 38521 Saint-Egrève Cedex

France

Tel: +33 (0)4 76 58 30 00

Hotline:

mailto: hotline bdc@e2v.com