Features

- 10-bit Resolution ADC
- 2.2 Gsps Sampling Rate
- Seamless Ascending Compatibility with TS83102G0B 10-bit 2 Gsps ADC
- 500 mVpp Full-scale Analog Input Range
- 100Ω Differential or 50Ω Single-ended Analog input and Clock Input
- 100Ω Differential Outputs
- ECL/LVDS Output Compatibility
- Functions:
  - ADC Gain Adjust and Sampling Delay Adjust
  - Data Ready Output with Asynchronous Reset
  - Out-of-range Output Bit
- Power Consumption: 4.2W
- Power supplies:
  - Analog: -5V, 5V
  - Digital: -5V to -2.2V and 1.5V
- Radiation Tolerant
- Package: CBGA152 Cavity Down Hermetic Package
- Evaluation Board AT84AS008GL-EB
- Companion Device:
  - DMUX 10-bit 1:2/1:4 LVDS 2.2 Gsps AT84CS001

Performances

- 3.3 GHz Full Power Input Bandwidth (-3 dB)
- Gain Flatness: ±0.2 dB (from DC up to 1.5 GHz)
- Low Input VSWR: 1.2 Maximum from DC to 2.5 GHz
- Single Tone Performances (-1 dBFs):
  SFDR = -58 dBc; 8.0 ENOB; SNR = 52 dBc at F_S = 1.7 Gsps, F_{IN} = 850 MHz
  SFDR = -54 dBc; 7.6 ENOB; SNR = 50 dBc at F_S = 2.2 Gsps, F_{IN} = 1.1 GHz
  SFDR = -54 dBc, 7.4 ENOB; SNR = 48 dBc at F_S = 2.2 Gsps, F_{IN} = 2 GHz
- Dual Tone Performances (IMD3), Fs = 1.7 Gps, (-7dBF_S tone):
  (Fin1 = 995 MHz, Fin2 = 1005 MHz): IMD3 = 64 dBF_S
  (Fin1 = 1545 MHz, Fin2 = 1555 MHz): IMD3 = 62 dBF_S
  (Fin1 = 1945 MHz, Fin2 = 1955 MHz): IMD3 = 59 dBF_S
- Low Bit Error Rate (10^{-11}) at 2.2 Gsps

Screening

- Temperature Range for Packaged Device:
  0°C < T_c; T_j < 90°C (Commercial *C* Grade)
  -20°C < T_c; T_j < 110°C (Industrial *V* Grade)

Applications

- Broadband Direct RF Down Conversion
- Wide Band Satellite Receivers
- Phased Array Antennas, Radars and ECM
- High-speed Instrumentation and High-speed Acquisition Systems
- High Energy Physics
- Automatic Test Equipment

e2v

10-bit 2.2 Gsps ADC

AT84AS008

5404A–BDC–11/06

1. Description

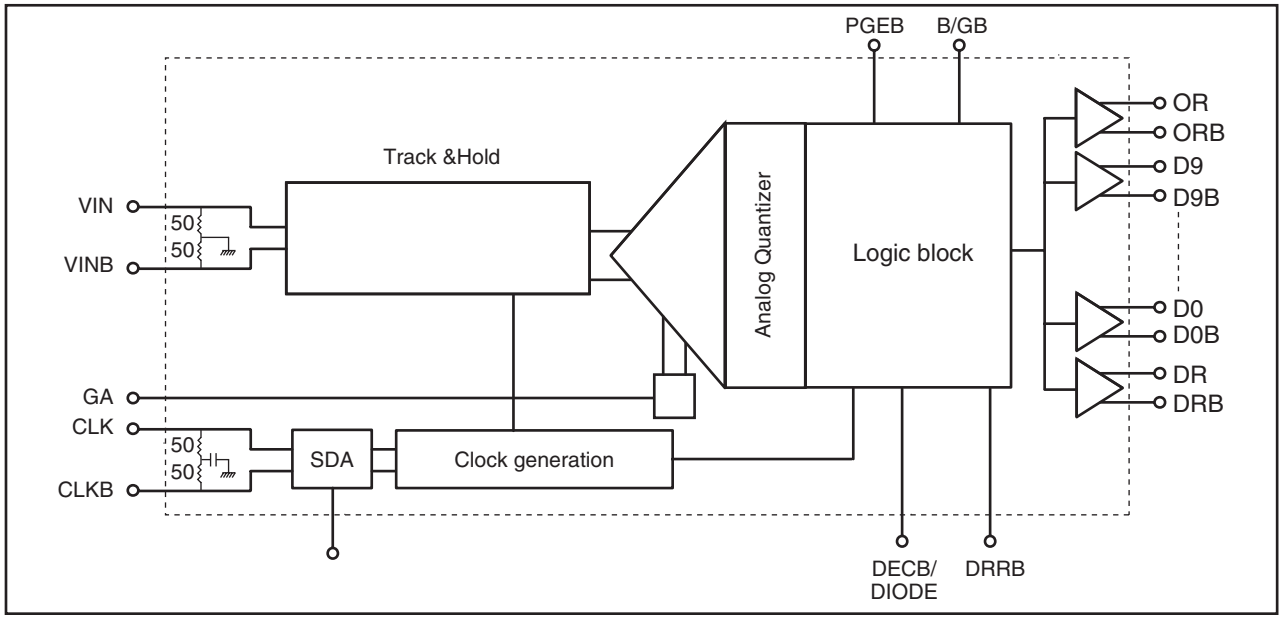
The AT84AS008 10-bit 2.2 Gsps ADC allows accurate digitization of high frequency signals thanks to the 3.3 GHz analog input bandwidth.

The innovative design of the on-chip Track and Hold (T/H) and digitizing core lead to unprecedented dynamic performance at a sampling rate of 2.2 GHz (over the full first Nyquist zone). A 7.6 ENOB is achieved at 2.2 Gsps in Nyquist conditions, using gray encoded digital outputs for optimum SNR performance.

The AT84AS008 features an enhanced spectral purity and very low noise floor, independent on frequency and temperature. It is particularly well suited for performance enhancement (i.e. dithering).

The AT84AS008 is fully compatible with TS83102G0B 10-bit 2 Gsps ADC, allowing zero-effort system improvement by plug-and-play replacement with the new part.

Figure 1-1. Block Diagram



2. Functional Description

The AT84AS008 is a 10-bit 2.2 Gsps ADC. The device includes a front-end Track and Hold stage (T/H), followed by an analog encoding stage (Analog Quantizer) which outputs analog residues resulting from analog quantization. Successive banks of latches regenerate the analog residues into logical levels before entering an error correction circuitry and a resynchronization stage followed by 100Ω differential output buffers.

The AT84AS008 works in fully differential mode from analog inputs up to digital outputs. A differential Data Ready output (DR/DRB) is available to indicate when the outputs are valid and an Asynchronous Data Ready Reset ensures that the first digitized data corresponds to the first acquisition.

For sampling rates exceeding 2 Gsps, the gray output encoding is recommended for optimum SNR performance.

The Control pin B/GB (A11 of CBGA package) is provided to select either a binary or gray data output format. The gain control pin GA (R9 of CBGA package) is provided to adjust the ADC gain transfer function. A Sampling Delay Adjust function (SDA) is provided to fine tune the ADC aperture delay, for applications requesting the interleaving of multiple ADCs for example. A Pattern Generator is integrated on chip for debug or acquisition set-up. This function is enabled through the PGEB pin (A9 of CBGA package). An out of range bit (OR,ORB) indicates when the input overrides the ADC full-scale range. A selectable decimation by 32 function is also available for enhanced testability coverage (A10 of CBGA package) along with a die junction temperature monitoring function.

The AT84AS008 uses only vertical isolated NPN transistors together with oxide isolated polysilicon resistors, which allows enhanced radiation tolerance (over 100 kRad (Si) expected total dose). The AT84AS008 provides full ascending compatibility with the TS83102G0B with enhanced performances.

3. Specifications

3.1 Absolute Maximum Ratings

Table 3-1. Absolute Maximum Ratings

Parameter	Symbol	Comments	Value	Unit
Positive supply voltage	V_{CC}		GND to 6.0	V
Digital negative supply voltage	D_{VEE}		GND to -5.7	V
Digital positive supply voltage	V_{PLUSD}		GND -1.1 to 2.5	V
Negative supply voltage	V_{EE}		GND to -5.5	V
Max difference between digital voltages	V_{PLUSD} - D_{VEE}		7	V
Maximum difference between negative supply voltages	D_{VEE} to V_{EE}		0.3	V
Analog input voltages	V_{IN} or V_{INB}		-1.5 to 1.5	V
Maximum difference between V_{IN} and V_{INB}	V_{IN} - V_{INB}		-1.5 to 1.5	V
Clock input common mode voltage	$(V_{CLK} + V_{CLKB})/2$		-1.5 to 0.6	V
Maximum difference between V_{CLK} and V_{CLKB}	V_{CLK} - V_{CLKB}		-1 to 1	Vpp
Static input voltage	V_D	GA, SDA	-1 to 0.8	V
Digital input voltage	V_D	SDAEN, DRRB, B/GB, PGEB, DECB	-5 to 0.8	V
Digital output voltage	V_O		V_{PLUSD} min operating -2.2 to V_{PLUSD} max operating + 0.8	V
Junction temperature	T_J		130	°C

Note: Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability.
All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

3.2 Recommended Conditions of Use

Table 3-2. Recommended Conditions of Use

Parameter	Symbol	Comments	Min	Typ	Max	Unit
Positive supply voltage	V_{CC}		4.75	5	5.25	V
Positive digital supply voltage[1]	V_{PLUSD}	Differential ECL output compatibility	-0.9	-0.8	-0.7	V
	V_{PLUSD}	LVDS output compatibility	1.375	1.45	1.525	V
	V_{PLUSD}	Grounded				
	V_{PLUSD}	Maximum operating V_{PLUSD}			1.7	V
Negative supply voltages	V_{EE}		-5.25	-5.0	-4.75	V
Negative supply voltages	D_{VEE}		-5.25	-5.0	-4.75	V
Negative supply voltages	D_{VEE}	Recommended to save power when VPLUS is above 1.4V[2]	-2.3	-2.2	-2.1	V
Differential analog input voltage (full-scale)	V_{IN} - V_{INB}	100Ω differential or 50Ω single-ended (Vinb grounded)		500	750	mV mVpp
Clock input power level (ground common mode)	P_{CLK}, P_{CLKB}	50 Ω single-ended clock input impedance or 100 Ω differential input (recommended)	-4	0	4	dBm
Operating temperature Range		Commercial *C* grade Industrial *V* grade	0°C < T_C; T_J < 90°C -20°C < T_C; T_J < 110°C			°C
Storage temperature	Tstg		-65 to 150			°C

Notes:
1. ADC performances are independent on V_{PLUSD} common mode voltage and performances are guaranteed in the limits of the specified V_{PLUSD} range (from -0.9V to 1.7V).
2. To save power D_{VEE} can be raised up to -2.2V as long as difference between V_{PLUSD} and D_{VEE} remains greater than 3.5V.

3.3 Electrical Characteristics

- V_{CC} = 5V; V_{EE} = D_{VEE} = -5V (unless otherwise specified): ADC performances are independent of V_{PLUSD} and D_{VEE} common mode voltage and performances are guaranteed in the limit of the specified V_{PLUSD} range (from -0.9V to 1.7V) and D_{VEE} range (from V_{EE} to -2.1V, as long as V_{PLUSD}-V_{EE} > 3.5V)
- V_{IN} - V_{INB} = 500 mVpp (full-scale single-ended or differential Input). Clock inputs differential driven; analog-input single-ended driven

Table 3-3. Electrical Operating Characteristics at Ambient Temperatures and Hot Temperatures

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Resolution				10		Bits
Power Requirements						
Power supply voltage						
- analog	1	V_{CC}	4.75	5	5.25	V
- digital (ECL)	1	V_{PLUSD}		-0.8		V
- digital (LVDS)	4	V_{PLUSD}		1.45		V
Power supply current						
- analog	1	I_{VCC}		80	100	mA
- digital ECL	1	I_{VPLUSD}		180	220	mA
LVDS (D_{VEE} = -2.2)	1	I_{VPLUSD}		160	200	mA
LVDS (D_{VEE} = -5)	1	I_{VPLUSD}		250	300	mA
Negative supply voltage						
- analog	1	V_{EE}	-5.25	-5	-4.75	V
- digital	1	D_{VEE}	-5.25	-5	-4.75	V
Negative supply current						
- analog	1	I_{VEE}		620	660	mA
- digital ECL	1	I_{DVEE}		180	220	mA
LVDS (D_{VEE} = -2.2)	1	I_{DVEE}		160	200	mA
LVDS (D_{VEE} = -5)	1	I_{DVEE}		250	300	mA
Power dissipation						
ECL	1			4.2	4.9	W
LVDS (D_{VEE} = -2.2)	1	P_D		4.0	4.8	W
LVDS (D_{VEE} = -5)	1			5.0	5.9	W
Analog Inputs						
Full-scale input voltage range (differential mode)	4	$V_{IN,}$	-125		125	mV
(0V common mode voltage)	4	V_{INB}	-125		125	mV
Full-scale input voltage range (single-ended input option other input grounded)	4 4	$V_{IN,}$ V_{INB}	-250	0	250	mV mV
Analog input power level (50Ω single-ended)	4	P_{IN}		-2		dBm
Analog input capacitance (die)	4	C_{IN}		0.3		pF
Input leakage current	4	I_{IN}		10		µA
Input resistance						
- single-ended	4	R_{IN}	49	50	51	Ω
- differential	4	R_{IN}	98	100	102	Ω

Table 3-3. Electrical Operating Characteristics at Ambient Temperatures and Hot Temperatures (Continued)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Clock Inputs						
Logic common mode compatibility for clock inputs			Differential ECL to LVDS			
Clock inputs common voltage range (V_{CLK} or V_{CLKB}) (DC coupled clock input) AC coupled for LVDS compatibility (common mode 1.2V)	4	V_{CM}	-1.2	0	0.3	V
Clock input power level (low-phase noise sinewave input) 50Ω single-ended or 100Ω differential	4	P_{CLK}	-4	0	4	dBm
Clock input swing (single ended; with CLKB = 50Ω to GND)	4	V_{CLK}	±200	±320	±500	mV
Clock input swing (differential voltage) - on each clock input	4	V_{CLK} V_{CLKB}	±141	±226	±354	mV
Clock input capacitance (die)	4	C_{CLK}		0.3		pF
Clock input resistance - single-ended - differential ended	 4 4	 R_{CLK} R_{CLK}	 45 90	 50 100	 55 110	 Ω Ω
Digital Inputs (SDAEN, PGEB, DECB/Diode, B/GB)						
- logic low - logic high	4	V_{IL} V_{IH}	-5 -2		-3 0	V V
Digital Inputs (DRRB Only)						
Logic Compatibility			Negative ECL			
- logic low - logic high	4	V_{IL} V_{IH}	-1.810 -1.165		-1.625 -0.880	V V
Digital Outputs[1]						
Logic compatibility (depending on V_{PLUSD} value)			Differential ECL (V_{PLUSD} = -0.8V typical)			
Output levels 50Ω transmission lines, 100Ω (2 × 50Ω) differentially terminated						
- logic low	1	V_{OL}		-1.24	-1.15	V
- logic high	1	V_{OH}	-0.99	-0.96		V
- swing (each single-ended output)	1	V_{OH} - V_{OL}	200	260	300	mV
- common mode	1		-1	-1.1	-1.15	V
Logic compatibility (depending on V_{PLUSD} value)			LVDS (V_{PLUSD} = 1.45V typical) D_{VEE} = -2.2V			
Output levels 50Ω transmission lines, 100Ω (2 × 50Ω) differentially terminated						
- logic low	4	V_{OL}		1050	1100	mV
- logic high	4	V_{OH}	1250	1280		mV
- swing (each single-ended output)	4	V_{OH} - V_{OL}	200	240	280	mV
- common mode[4]..... max V_{PLUSD} = 1.525V	4				1310	mV
..... typ V_{PLUSD} = 1.45V	4			1160		mV
..... min V_{PLUSD} = 1.375V	4		1010			mV

Table 3-3. Electrical Operating Characteristics at Ambient Temperatures and Hot Temperatures (Continued)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Logic compatibility (depending on V_{PLUSD} value)	LVDS (V_{PLUSD} = 1.45V typical) D_{VEE} = - 5V					
Output levels 50Ω transmission lines, 100Ω (2 × 50Ω) differentially terminated						mV
- logic low	1	V_{OL}		840	900	mV
- logic high	1	V_{OH}	1160	1220		mV
- swing (each single-ended output)	1	V_{OH} - V_{OL}	325	375	450	mV
- common mode[4] ..... max V_{PLUSD} = 1.525V	4				1180	mV
..... typ V_{PLUSD} = 1.45V	1			1030		mV
..... min V_{PLUSD} = 1.375V	4		880			
DC Accuracy						
DNLrms	1	DNLrms		0.2	0.3	LSB
Differential non-linearity[2]	1	DNL+		0.8	1.5	LSB
Integral non-linearity[2]	1	INL-	-4	-2.5		LSB
Integral non-linearity[2]	1	INL+		2.5	4	LSB
Gain central value[3]	1		0.9	1	1.1	
Gain error drift	4			23	35	ppm/°C
Input offset voltage	1		-10		10	mV

Notes:
1. Differential output buffers impedance = 100Ω differential (50Ω single-ended).
2. Histogram testing at Fs = 390 Msps Fin = 100 MHz.
3. The ADC Gain can be fine tuned to *1* thanks to the gain adjust function.
4. The output common mode only depends on V_{PLUSD} value and can thus be adjusted accordingly.

Table 3-4. AC Electrical Characteristics at Ambient Temperatures and Hot Temperatures (T_J Max)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
AC Analog Inputs						
Full power input bandwidth[1]	4	FPBW		3.3		GHz
Small signal input bandwidth (10% full-scale)	4	SSBW		3.5		GHz
Gain flatness[2]	4	BF		±0.2	±0.3	dB
Input voltage standing wave ratio[3]	4	VSWR		1.1:1	1.2:1	
AC Performance: Nominal Condition at Ambient and Hot Temperature Tj Max -1 dBF_S Single ended input mode (unless otherwise specified), 50% clock duty cycle, 0dBm differential clock (CLK, CLKB), Binary output data format.						
Signal-to-noise and Distortion Ratio						
Fs = 1.4 Gsps ..... Fin = 700 MHz	1	SINAD	46	49		dBc
Fs = 1.7 Gsps ..... Fin = 1.7 GHz	4		44	47		
Fs = 2.2 Gsps ..... Fin = 1.1 GHz	4		43	47		
Fs = 2.2 Gsps ..... Fin = 2.0 GHz	4		43	46		

Table 3-4. AC Electrical Characteristics at Ambient Temperatures and Hot Temperatures (T_J Max) (Continued)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Effective Number of Bits						
Fs = 1.4 Gsps ..... Fin = 700 MHz	1	ENOB	7.4	8.0		Bit
Fs = 1.7 Gsps ..... Fin = 1.7 GHz	4		7.2	7.7		
Fs = 2.2 Gsps ..... Fin = 1.1 GHz	4		7.1	7.6		
Fs = 2.2 Gsps ..... Fin = 2.0 GHz	4		7.0	7.4		
Signal to Noise Ratio						
Fs = 1.4 Gsps ..... Fin = 700 MHz	1	SNR	49	52		dBc
Fs = 1.7 Gsps ..... Fin = 1.7 GHz	4		46	49		
Fs = 2.2 Gsps ..... Fin = 1.1 GHz	4		46	50		
Fs = 2.2 Gsps ..... Fin = 2.0 GHz	4		45	48		
Total Harmonic Distortion (25 harmonics)						
Fs = 1.4 Gsps ..... Fin = 700 MHz	1	|THD|	46	52		dBc
Fs = 1.7 Gsps ..... Fin = 1.7 GHz	4		47	52		
Fs = 2.2 Gsps ..... Fin = 1.1 GHz	4		45	49		
Fs = 2.2 Gsps ..... Fin = 2.0 GHz	4		45	50		
Spurious Free Dynamic Range						
Fs = 1.4 Gsps ..... Fin = 700 MHz	1	|SFDR|	50	58		dBc
Fs = 1.7 Gsps ..... Fin = 1.7 GHz	4		52	58		
Fs = 2.2 Gsps ..... Fin = 1.1 GHz	4		48	54		
Fs = 2.2 Gsps ..... Fin = 2.0 GHz	4		48	54		
Two-tone Third Order Inter-modulation Distortion						
Fs = 1.7 Gsps (-7 dBF_S each tone)		|IMD3|				dBFs
- Fin1 = 995 MHz; Fin2 = 1005 MHz	4			64		
- Fin1 = 1545 MHz; Fin2 = 1555 MHz	4			62		
- Fin1 = 1945 MHz; Fin2 = 1955 MHz	4			59		

Notes:
1. See “Definition of Terms” on page 31.
2. From DC to 1.5GHz
3. Specified from DC up to 2.5 GHz input signal. Input VSWR is measured on a soldered device. It assumes an external 50Ω ± 2Ω controlled impedance line, and a 50Ω driving source impedance (S_{11} < -30 dB).

Table 3-5. Transient and Switching Performances

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Transient Performance						
Bit error rate(1)	4	BER			10^{-11}	Error/ Sample
ADC settling time (VIN-VINB = 400 mVpp)	4	TS		400		ps
Overvoltage recovery time	4	ORT			500	ps
ADC step response rise/fall time (10/90%)	4			80	100	ps
Overshoot	5			4		%
Ringback	5			2		%

Table 3-5. Transient and Switching Performances (Continued)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Switching Performance and Characteristics						
Maximum clock frequency(2)		Fs Max	2.2			Gsps
Minimum clock frequency(2)	4	Fs Min			200	Msps
Minimum clock pulse width (high)	4	TC1	0.22		2.5	ns
Minimum clock pulse width (low)	4	TC2	0.22		2.5	ns
Aperture delay(2))	4	TA		160		ps
Aperture uncertainty(2)	4	Jitter		150	200	fs rms
Output rise/fall time for DATA (20%-80%)(3)	4	TR/TF		80	110	ps
Output rise/fall time for DATA READY (20%-80%)(3)	4	TR/TF		80	110	ps
Data Output Delay(4)	4	TOD		360		ps
Data Ready Output Delay(4)	4	TDR		360		ps
	4	|TOD-TDR|	-50	0	+50	ps
Output Data to Data Ready propagation delay(5)	4	TD1	200	250	250	ps
Data Ready to Output Data propagation delay(5)	4	TD2	150	200	250	ps
Output data pipeline delay	4	TPD		4.0		Clock Cycles
Data ready reset delay	4	TRDR	300			ps

Notes:
1. Output error amplitude < ± 6 lsb. Fs = 2.2Gsps TJ = 110 °C
2. See “Definition of Terms” on page 31.
3. 50Ω // C_{LOAD} = 2 pF termination (for each single-ended output). Termination load parasitic capacitance derating value: 50 ps/pF (ECL). See “Timing Information” on page 33.
4. TOD and TDR propagation times are defined at package input/outputs. They are given for reference only
5. Values for TD1 and TD2 are given for a 2.2 Gsps external clock frequency (50% duty cycle). For different sampling rates, apply the following formula: TD1 = T/2 +(|TOD-TDR|) and TD2 = T/2 +(|TOD-TDR|), where T = clock period.
This places the rising edge (True-False) of the differential Data Ready signal in the middle of the Output Data valid window. This gives maximum setup and hold times for external data acquisition.

3.4 Explanation of Test Levels

Table 3-6. Explanation of Test Levels

1	100% production tested at +25°C(1) (for *C* temperature range(2))
2	100% production tested at +25°C(1), and sample tested at specified temperatures (for *V* temperature ranges(2))
3	Sample tested only at specified temperatures
4	Parameter is guaranteed by design and characterization testing (thermal steady-state conditions at specified temperature)
5	Parameter is a typical value only guaranteed by design only

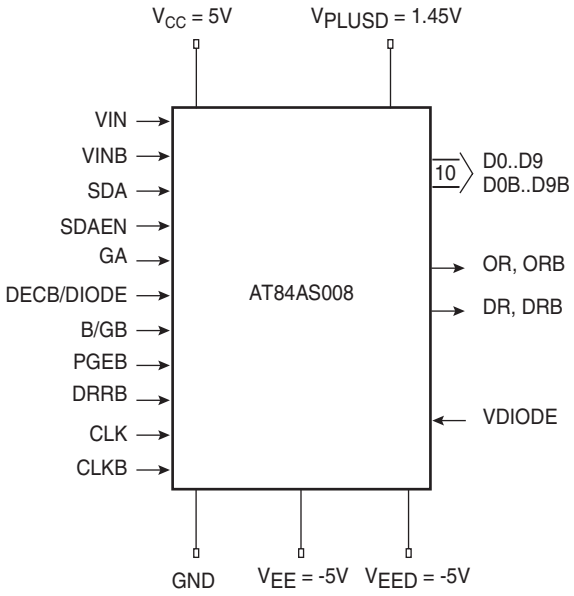
Only minimum and maximum values are guaranteed (typical values are issuing from characterization results).

Notes:
1. Unless otherwise specified.
2. Refer to ”Ordering Information” on page 45.

3.5 Functions Description

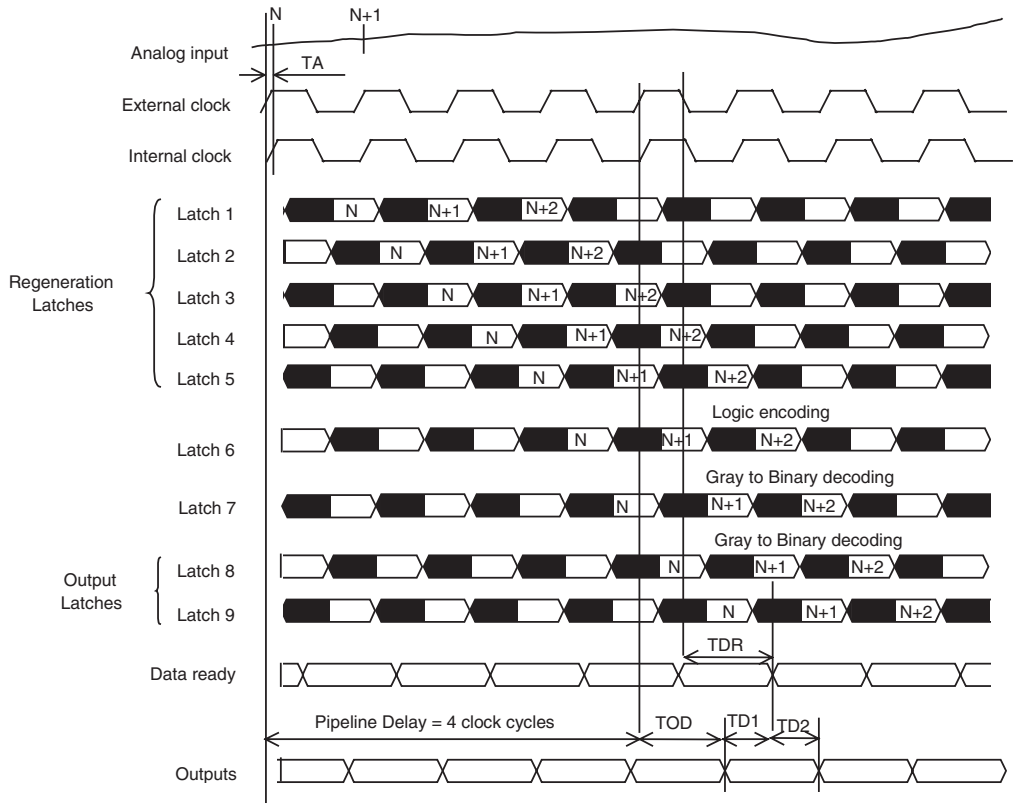
Table 3-7. Functions Description

Name	Function
V_{CC}	Positive power supply: 5V
V_{PLUSD}	Positive power supply for buffers:-0.8V => ECL; 1.45V => LVDS
V_{EE}	Negative power supply: -5V
D_{VEE}	Negative power supply for buffers:-5V or -2.2V (if LVDS output logic)
VIN,VINB	Differential analog input
CLK,CLKB	Differential clock input
[D0:D9][D0B:D9B]	Differential output data.
OR, ORB	Differential out of range
DR,DRB	Differential data ready
DRRB	Active low data ready reset
PGEB	Active low pattern generator enable
SDA	Sampling delay adjust input
SDAEN	Active low sampling delay adjust enable
GA	Gain adjust input
DECB/DIODE	Active low decimator enable and diode for die junction temperature monitoring



3.6 Timing Diagram

Figure 3-1. Timing Diagram



Detailed timing diagram is provided in Section 3.6 on page 11.

3.7 Coding

Table 3-8. ADC Coding Table

Differential Analog Input	Voltage Level	Digital Output			
		Binary (B/GB = GND or floating) MSB……..LSB	Out-of-Range	GRAY (B/GB = V_{EE}) MSB……..LSB	Out-of-Range
> + 250.25 mV	>Top end of full-scale + ½ LSB	1 1 1 1 1 1 1 1 1 1 1	1	1 0 0 0 0 0 0 0 0 0 0	1
+ 250.25 mV	Top end of full-scale + ½ LSB	1 1 1 1 1 1 1 1 1 1 1	0	1 0 0 0 0 0 0 0 0 0 0	0
+ 249.75 mV	Top end of full-scale - ½ LSB	1 1 1 1 1 1 1 1 1 1 0	0	1 0 0 0 0 0 0 0 0 0 1	0
+ 125.25 mV	3/4 full-scale + ½ LSB	1 1 0 0 0 0 0 0 0 0 0	0	1 0 1 0 0 0 0 0 0 0 0	0
+ 124.75 mV	3/4 full-scale - ½ LSB	1 0 1 1 1 1 1 1 1 1 1	0	1 1 1 0 0 0 0 0 0 0 0	0
+ 0.25 mV	Midscale + ½ LSB	1 0 0 0 0 0 0 0 0 0 0	0	1 1 0 0 0 0 0 0 0 0 0	0
-0.25 mV	Midscale - ½ LSB	0 1 1 1 1 1 1 1 1 1 1	0	0 1 0 0 0 0 0 0 0 0 0	0
-124.75 mV	1/4 full-scale + ½ LSB	0 1 0 0 0 0 0 0 0 0 0	0	0 1 1 0 0 0 0 0 0 0 0	0
-124.25 mV	1/4 full-scale - ½ LSB	0 0 1 1 1 1 1 1 1 1 1	0	0 0 1 0 0 0 0 0 0 0 0	0
-249.75 mV	Bottom end of full-scale + ½ LSB	0 0 0 0 0 0 0 0 0 0 1	0	0 0 0 0 0 0 0 0 0 0 1	0
-250.25 mV	Bottom end of full-scale - ½ LSB	0 0 0 0 0 0 0 0 0 0 0	0	0 0 0 0 0 0 0 0 0 0 0	0
< -250.25 mV	< Bottom end of full-scale - ½ LSB	0 0 0 0 0 0 0 0 0 0 0	1	0 0 0 0 0 0 0 0 0 0 0	1

4. Characterization Results

4.1 Nominal Conditions

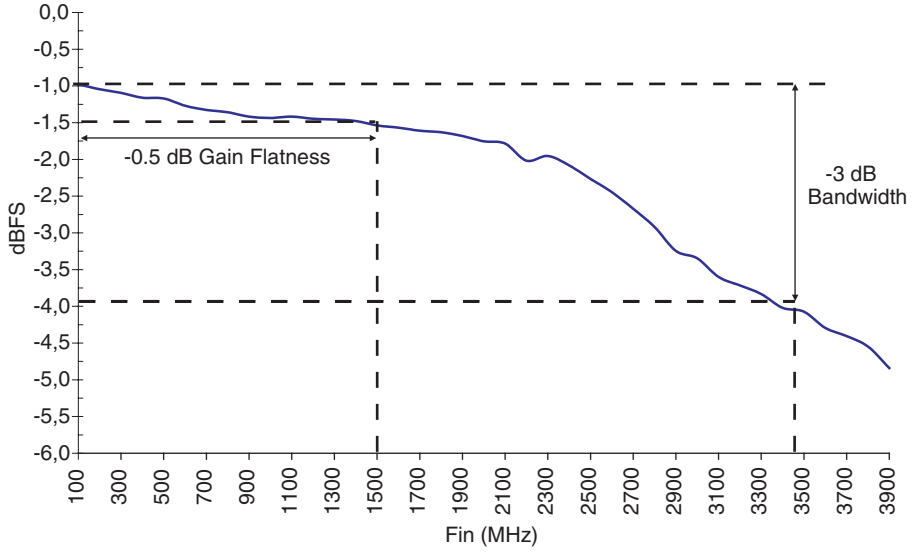
Unless Otherwise specified:

V_{CC} = 5V, V_{EE} = -5V, V_{PLUSD} = 1.45V
TJ = 80°C
50% clock duty cycle, binary output data format
-1 dBFS analog Input

4.2 Full Power Input Bandwidth

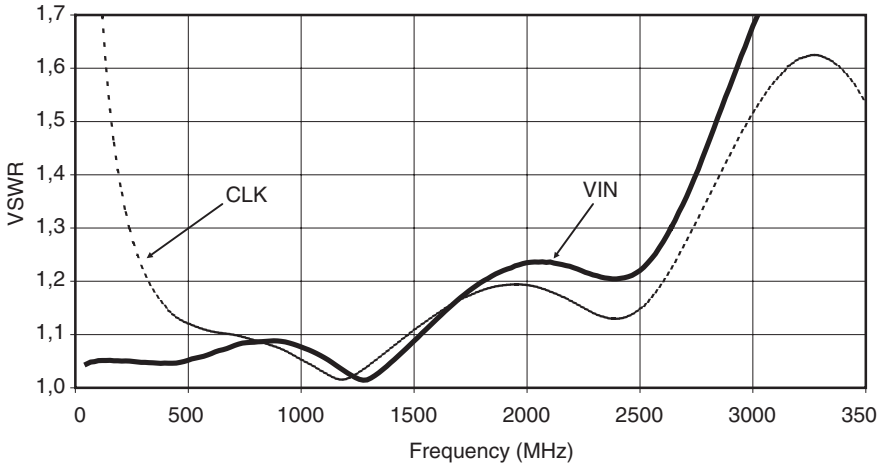
Analog input level = -1 dBFS
Gain flatness at -0.5 dB from DC to 1.5 GHz

Figure 4-1. Full Power Input Bandwidth at -3 dB



4.3 VSWR Versus Input Frequency

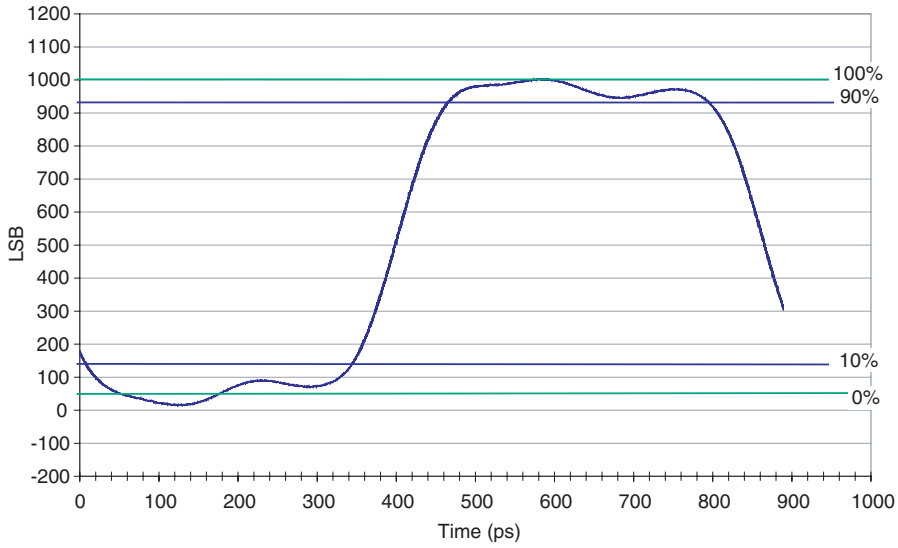
Figure 4-2. VSWR Curve for the Analog Input (VIN) and Clock (CLK)



4.4 Step Response

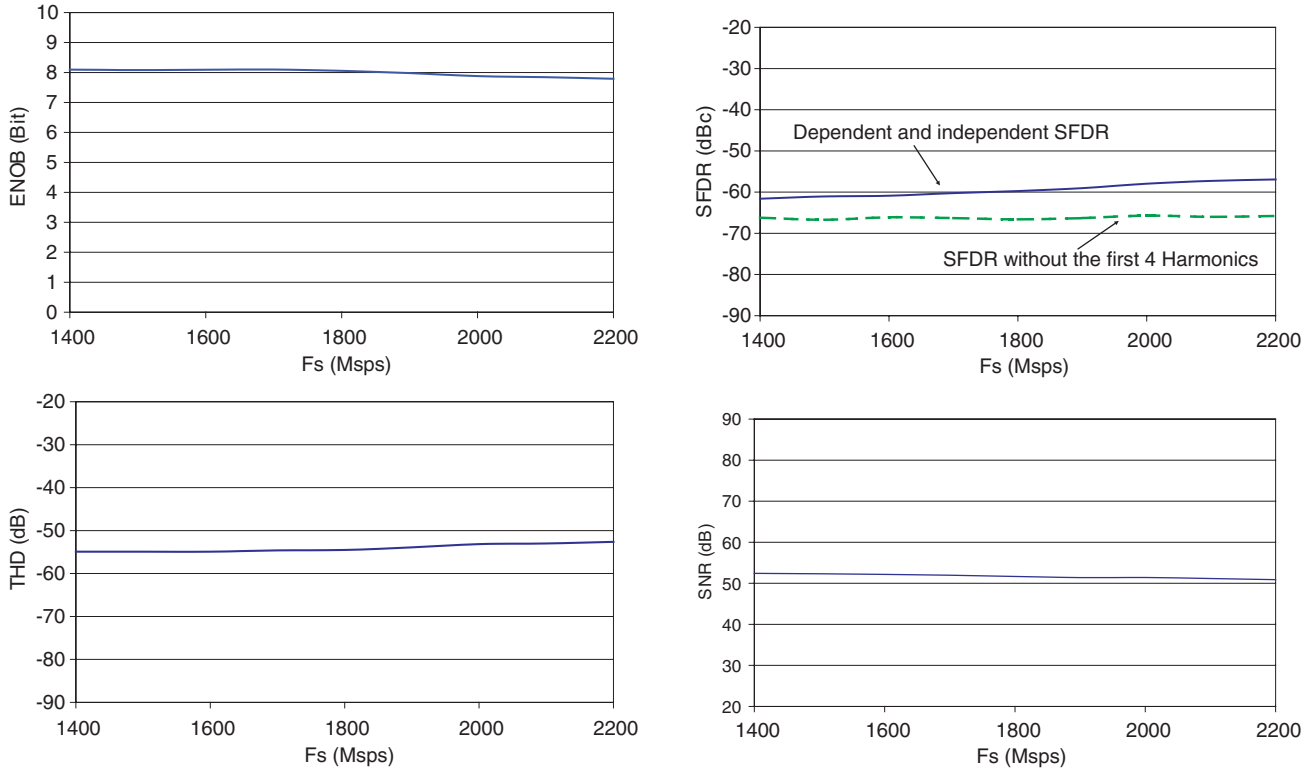
Tr measured = 115 ps = sqrt($Tr_{PulseGenerator}^2$ + Tr_{ADC}^2)
$Tr_{PulseGenerator}$ (estimated) = 41 ps
Actual Tr_{ADC} = 107 ps

Figure 4-3. Step Response Rise Time (Fs = 2.2 Gsps, fin = 1.1 GHz)



4.5 Dynamic Performance Versus Sampling Frequency

Figure 4-4. Dynamic Parameters Versus Sampling Frequency in Nyquist Conditions (Fin = Fs/2)



4.6 Dynamic Performance Versus Input Frequency

Figure 4-5. Dynamic Parameters Versus Input Frequency at Fs = 1.7 Gsps and 2.2 Gsps

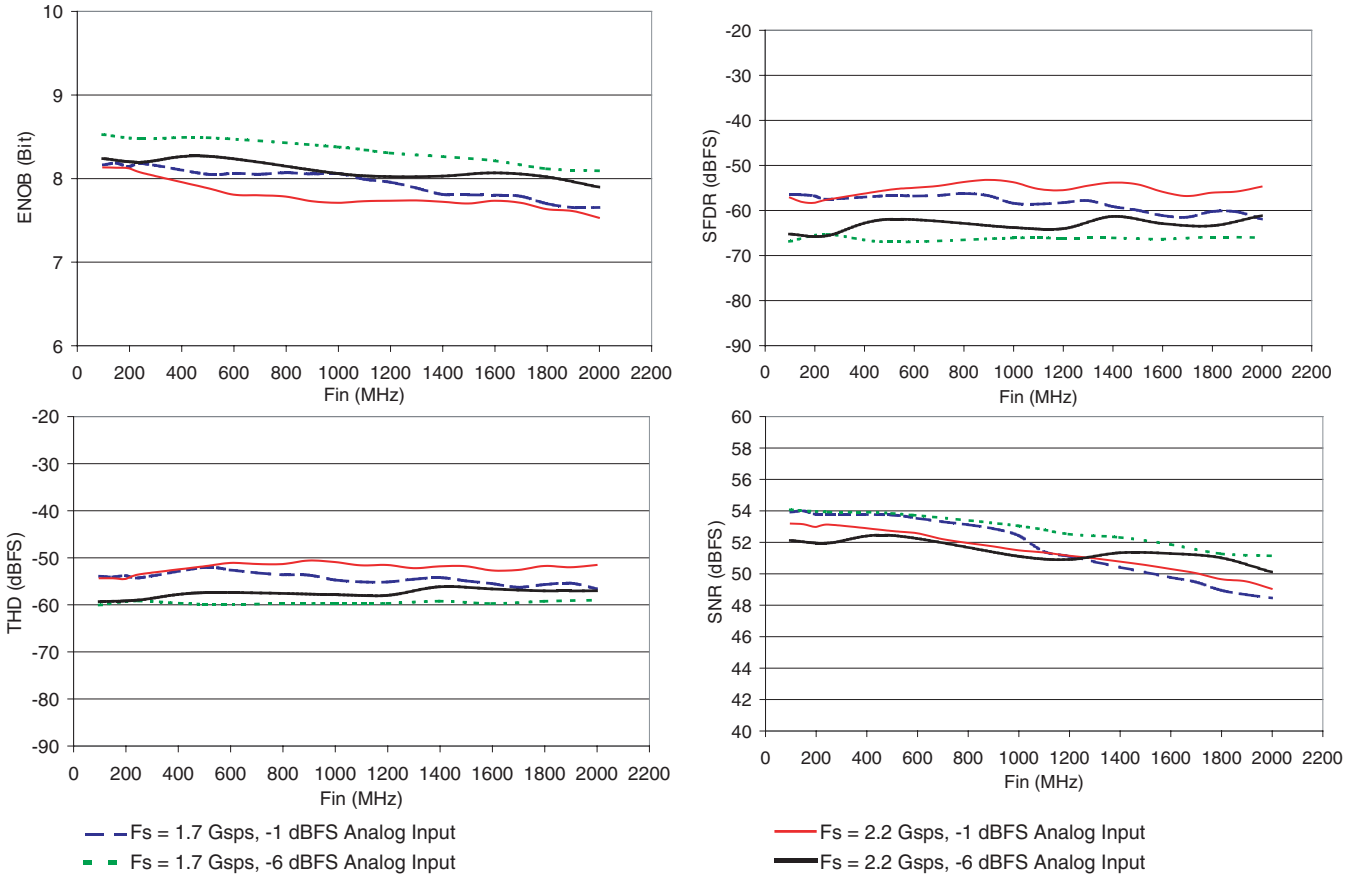
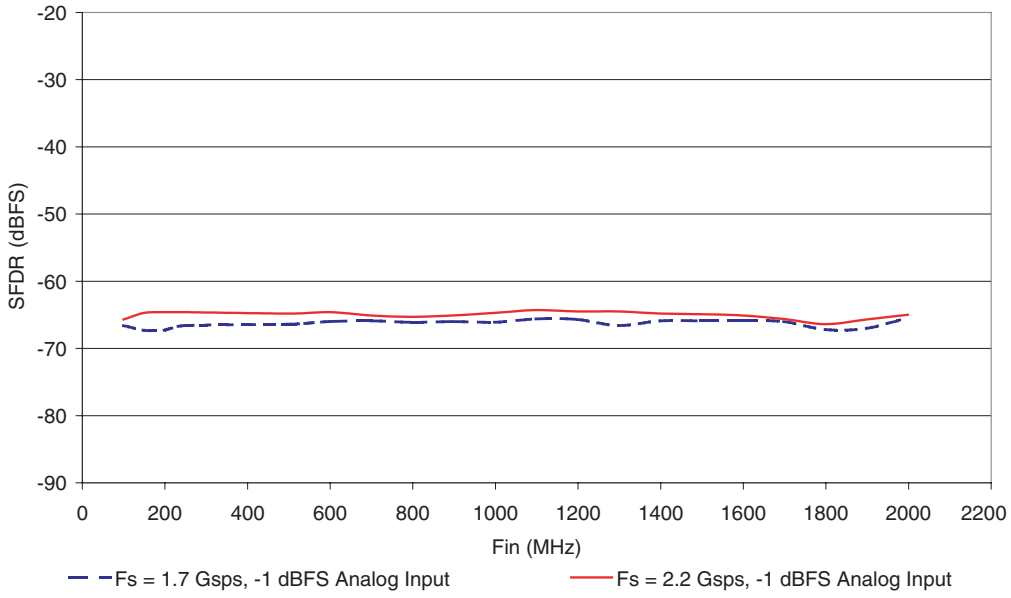


Figure 4-6. SFDR (Minus the First 4 Harmonics) Versus Input Frequency at Fs = 1.7 Gsps and 2.2 Gsps



4.7 Signal Spectrum

Figure 4-7. Fs = 1.7 Gsps, Fin = 848 MHz, and 1698 MHz, -1 dBFS analog input, 32 kpoint FFT

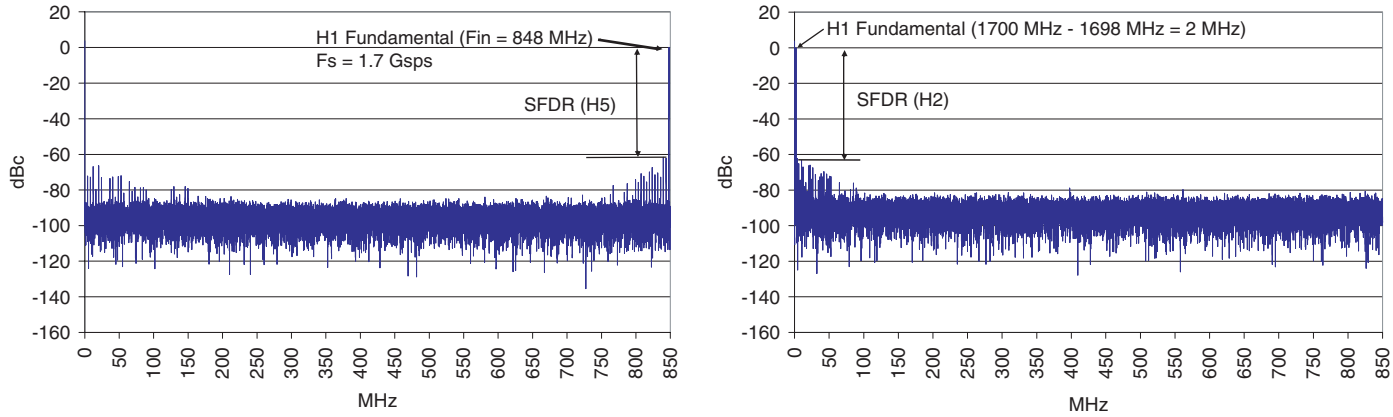


Figure 4-8. Fs = 1.9 Gsps, Fin = 948 MHz and 1899 MHz, -1 dBFS Analog Input, 32 kpoint FFT

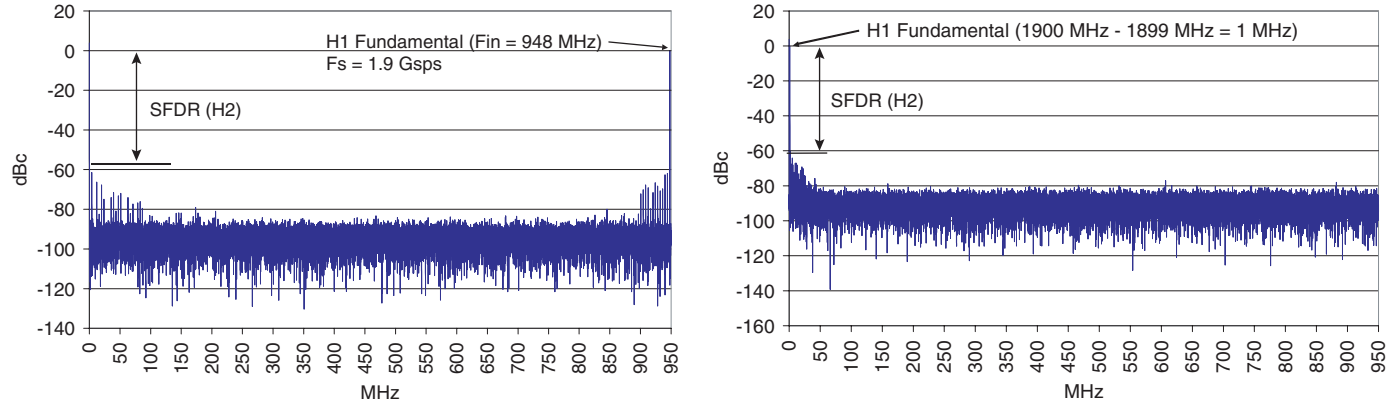
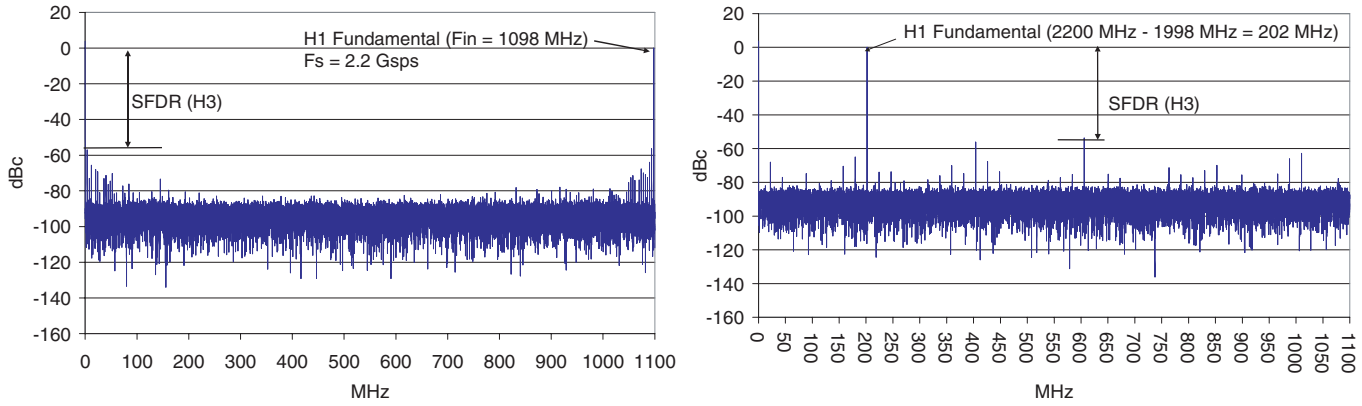


Figure 4-9. Fs = 2.2 Gsps, Fin = 1098 MHz and 1998 MHz, -1 dBFS Analog Input, 32 kpoint FFT



4.8 Dynamic Performance Sensitivity Versus Temperature and Power Supply

Figure 4-10. Dynamic Parameters Versus Junction Temperature at Fs = 1.7 Gsps, Fin = 848 MHz, -1 dBFS Analog Input

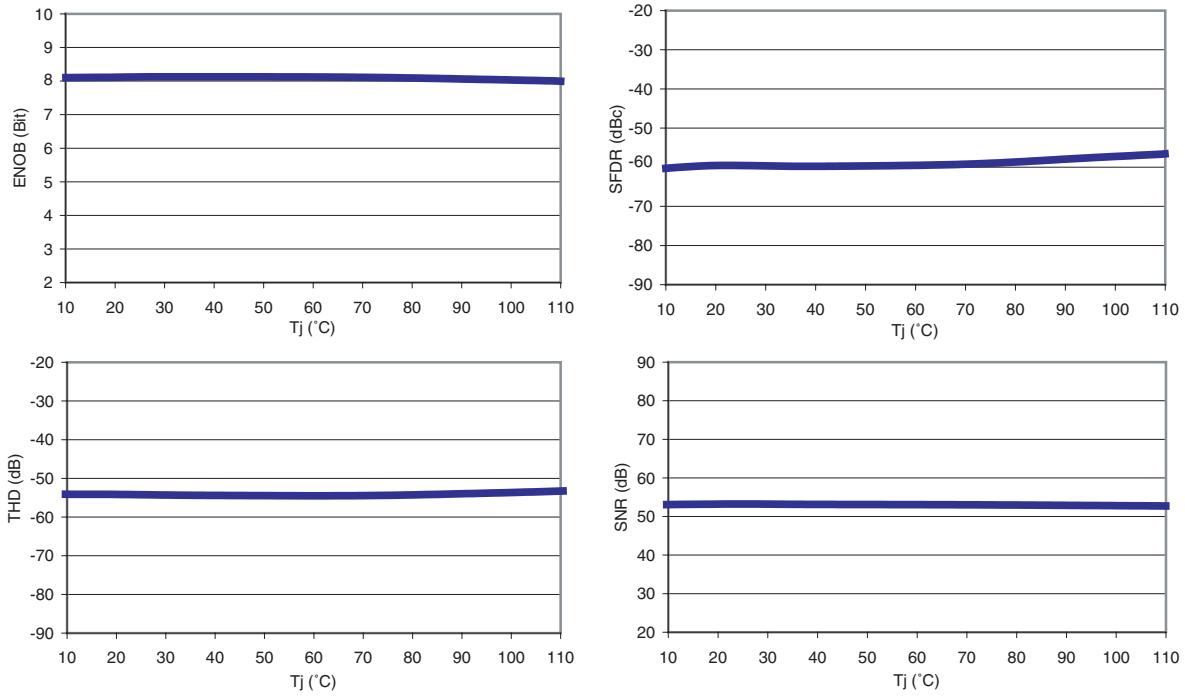
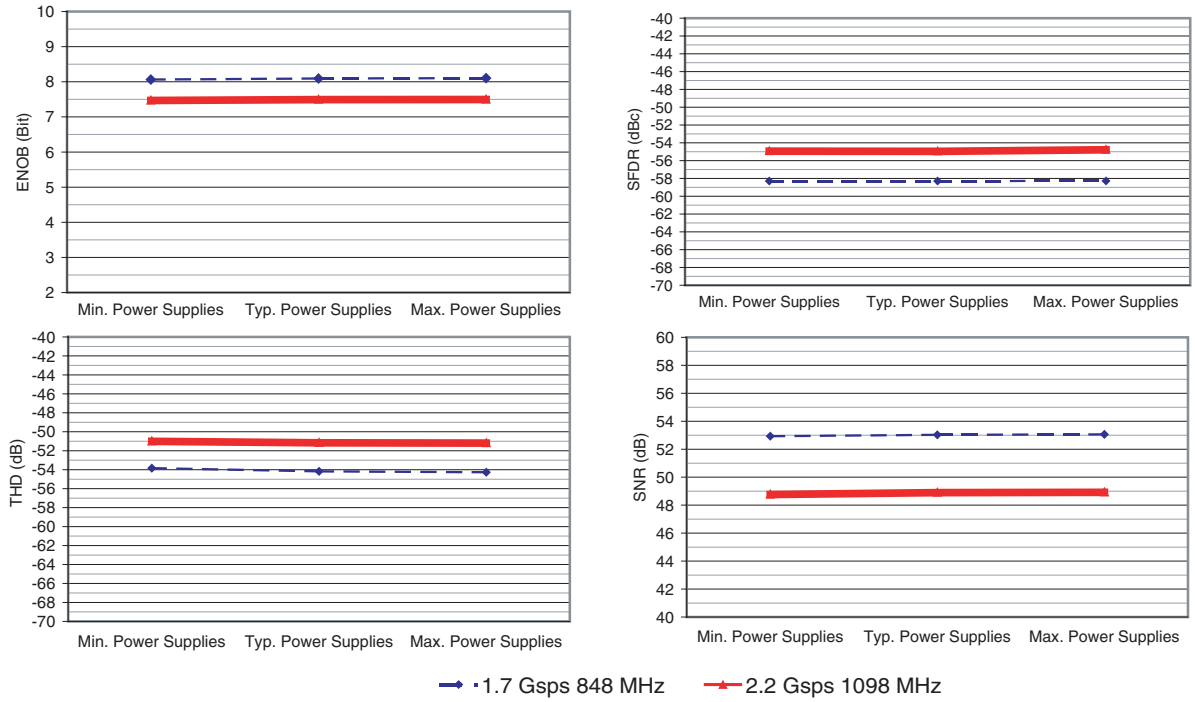


Figure 4-11. Dynamic Parameters at Min., Typ. And Max. Power Supplies, -1 dBFS Analog Input



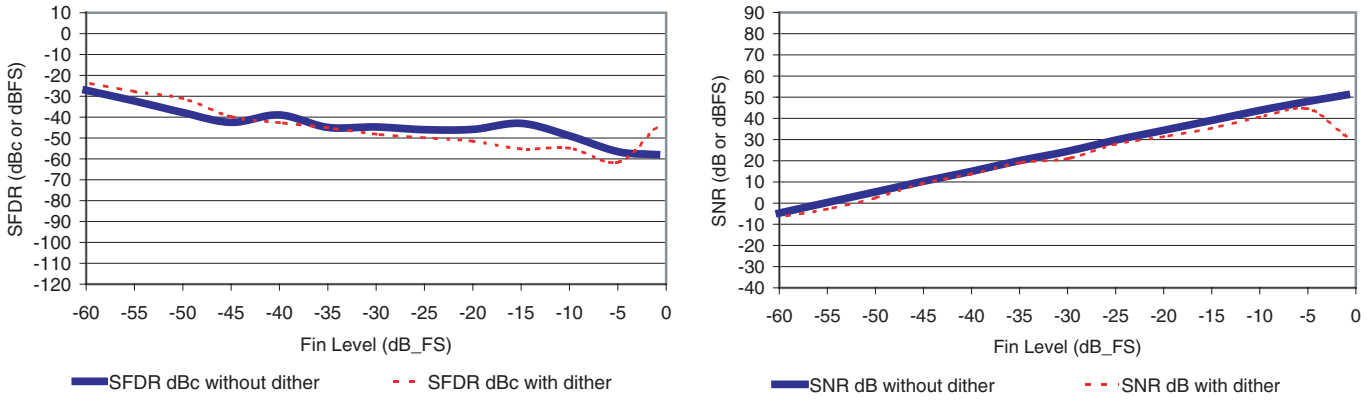
Note: Min. power supplies: V_{CC} = 4.75,V V_{EE} = -4.75V, V_{PLUSD} = 1.375V
Typ. power supplies: V_{CC} = 5V, V_{EE} = -5V, V_{PLUSD} = 1.45V
Max. power supplies: V_{CC} = 5.25V, V_{EE} = -5.25V, V_{PLUSD} = 1.525V

4.9 SFDR Performance with and without Added Dither

The dither profile has to be defined according to the ADC's INL pattern as well as the trade-off to be reached between the increase in SFDR and the loss in SNR, as described in Figure 4-12

Please refer to the application note on Dither for more information.

Figure 4-12. SFDR and SNR (dBc and dBFS) with and without Added Dither (-17 dBm DC to 5 MHz out of Band Dither) Versus Analog Input Power at Fs = 1.7 Gsps, Fin = 710 MHz



4.10 Dual Tone Performance

Figure 4-13. Dual Tone Signal Spectrum at Fs = 1.7 Gsps, Fin1 = 995 MHz, Fin2 = 1005 MHz (-7 dBFS), IMD3 = 68 dBFS.

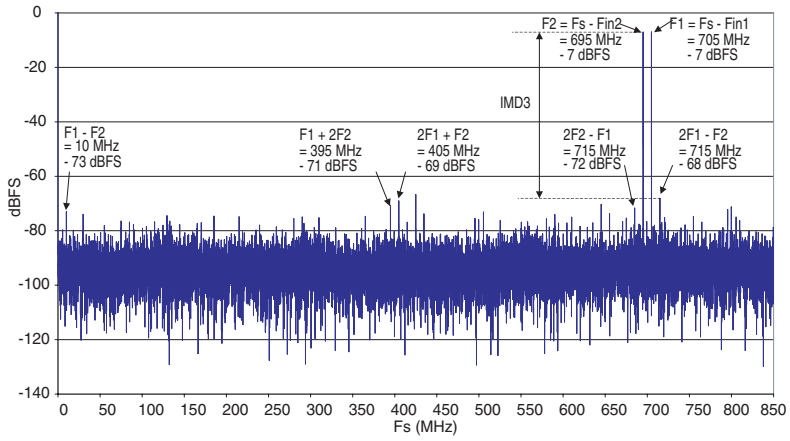


Figure 4-14. Dual Tone Signal Spectrum at Fs = 1.7 Gsps, Fin1=1545 MHz, Fin2 = 1555 MHz (-7 dBFS), IMD3 = 64 dBFS.

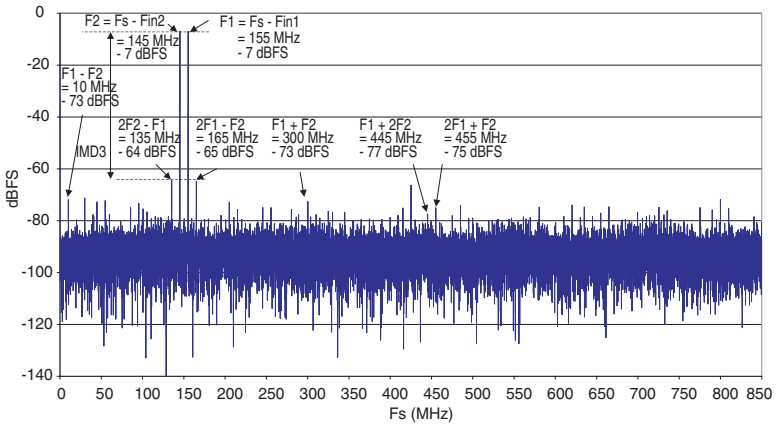


Figure 4-15. Dual Tone Signal Spectrum at Fs = 1.7 Gsps, Fin1 = 1945 MHz, Fin2 = 1955 MHz (-7 dBFS), IMD3 = 59 dBFS

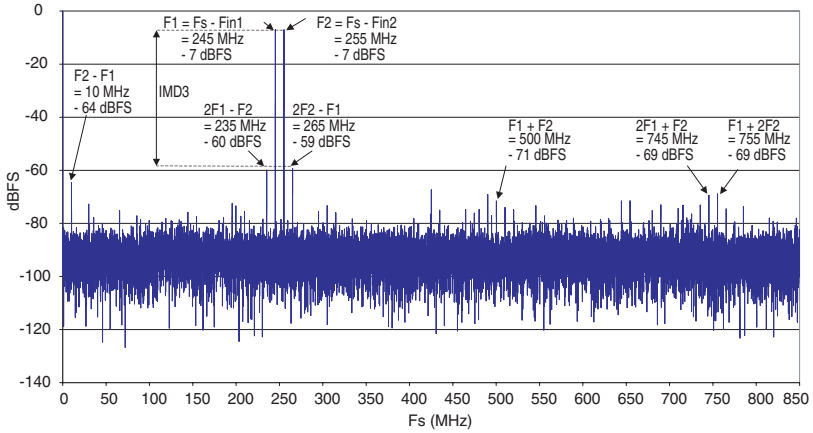


Figure 4-16. Dual Tone Signal Spectrum at Fs = 2.2 Gsps, Fin1 = 1015 MHz, Fin2 = 1025 MHz (-7 dBFS), IMD3 = 62 dBFS.

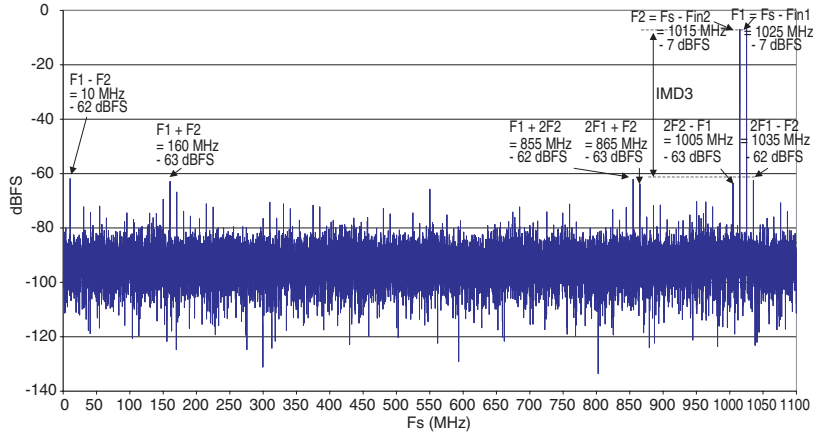


Figure 4-17. Dual Tone Signal Spectrum at Fs = 2.2 Gsps, Fin1= 1545 MHz, Fin2 = 1555 MHz (-7 dBFS), IMD3 = 64 dBFS.

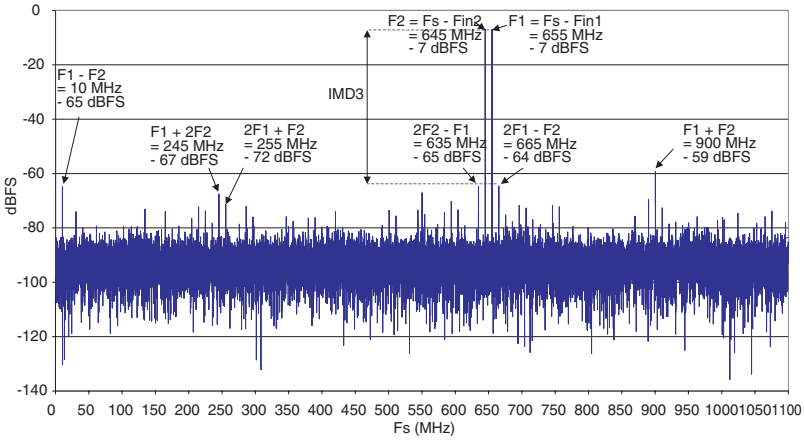
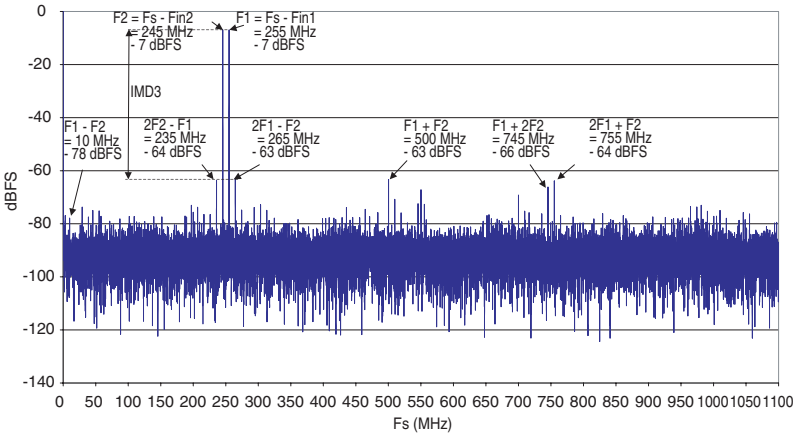
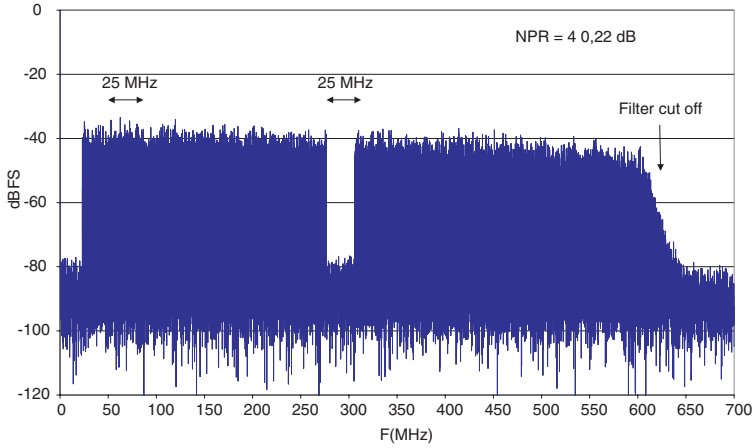


Figure 4-18. Dual Tone Signal Spectrum at Fs= 2.2 Gsps, Fin1=1945 MHz, Fin2 = 1955 MHz (-7 dBFS), IMD3 = 63 dBFS.



4.11 NPR performance

Figure 4-19. Digitizing of 575 MHz Broadband Pattern @ 1.4 Gsps, 25 MHz Notch Centered Around 290 MHz, -12 dBFS Loading Factor.



5. Pin Description

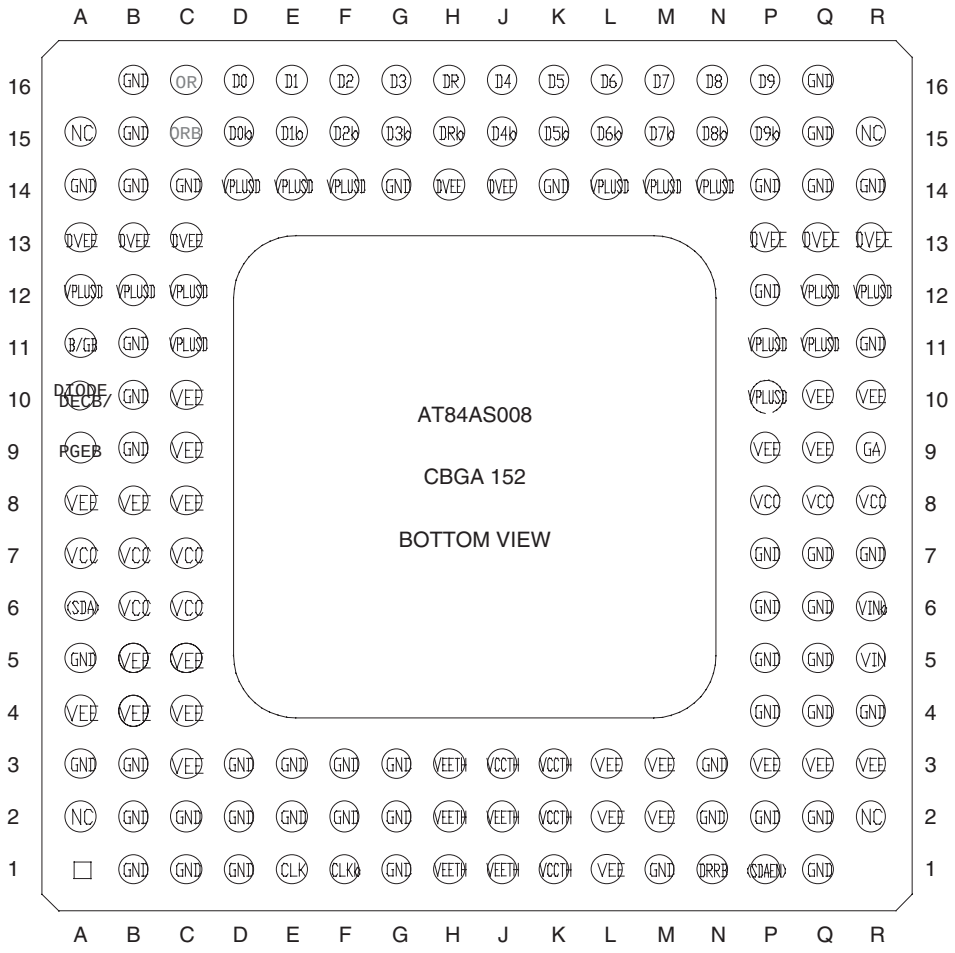
Table 5-1. Pin Description (CBGA 152)

Symbol	Pin Number	Function
Power Supplies		
V_{CC}	K1, K2, J3, K3, B6, C6, A7, B7, C7, P8, Q8, R8	5V analog supply (connected to same power supply plane)
GND	B1, C1, D1, G1, M1, Q1, B2, C2, D2, E2, F2, G2, N2, P2, Q2, A3, B3, D3, E3, F3, G3, N3, P4, Q4, R4, A5, P5, Q5, P6, Q6, P7, Q7, R7, B9, B10, B11, R11, P12, A14, B14, C14, G14, K14, P14, Q14, R14, B15, Q15, B16, Q16	Analog ground
V_{EE}	H1, J1, L1, H2, J2, L2, M2, C3, H3, L3, M3, P3, Q3, R3, A4, B4, C4, B5, C5, A8, B8, C8, C9, P9, Q9, C10, Q10, R10	-5V analog supply (connected to same power supply plane)
V_{PLUSD}	P10, C11, P11, Q11, A12, B12, C12, Q12, R12, D14, E14, F14, L14, M14, N14	Digital positive supply
D_{VEE}	A13, B13, C13, P13, Q13, R13, H14, J14	-5V or -2.2V digital power supply
Analog Inputs		
VIN	R5	In-phase (+) analog input signal of the differential sample and hold preamplifier
VINB	R6	Inverted phase (-) analog input signal of the differential sample and hold preamplifier
Clock Inputs		
CLK	E1	In-phase (+) clock input
CLKB	F1	Inverted phase (-) clock input
Digital Outputs		
D0, D1, D2, D3, D4, D5, D6, D7, D8, D9	D16, E16, F16, G16, J16, K16, L16, M16, N16, P16	In-phase (+) digital outputs D0 is the LSB, D7 is the MSB
D0B, D1B, D2B, D3B, D4B, D5B, D6B, D7B, D8B, D9B	D15, E15, F15, G15, J15, K15, L15, M15, N15, P15	Inverted phase (-) digital outputs
OR	C16	In-phase (+) out-of-range output
ORB	C15	Inverted phase (-) out-of-range output
DR	H16	In-phase (+) data ready signal output
DRB	H15	Inverted phase (-) data ready signal output
Additional Functions		
B/GB	A11	Binary or gray select output format control - binary output format if B/GB is floating or connected to GND - gray output format if B/GB is connected to V_{EE}

Table 5-1. Pin Description (CBGA 152) (Continued)

Symbol	Pin Number	Function
DECB / DIODE	A10	Decimation function enable or die junction temperature measurement: - Decimation active when low (die junction temperature monitoring is then not possible) - Normal mode when high or left floating die junction temperature monitoring when current is applied
PGEB	A9	Active low pattern generator enable - Digitized input delivered at outputs according to B/GB if PGEB is floating or connected to GND - Checker Board pattern delivered at outputs if PGEB is connected to V_{EE}
DRRB	N1	Asynchronous data ready reset function (active at ECL low level)
GA	R9	Gain adjust
SDA	A6	Sampling delay adjust
SDAEN	P1	Sampling delay adjust enable inactive if floating or connected to GND active if connected to V_{EE}

Figure 5-1. CBGA152 Pinout



Notes:
1. If required, 4 NC balls can be electrically connected to GND if simplifying PCB routing.
2. The pinout is given with a BOTTOM view. The way the columns and rows were defined is different from the JEDEC standard.

5.1 Package Description

5.1.1 Hermetic CBGA 152 Outline Dimensions

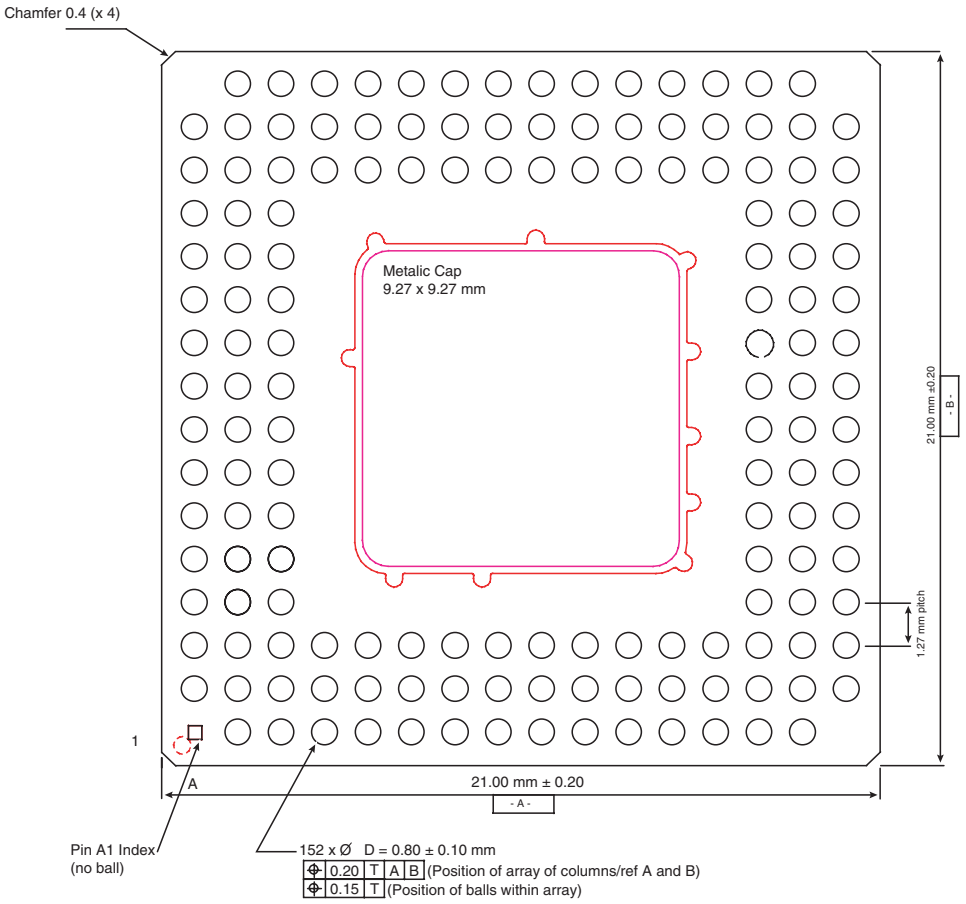
Ceramic body size: 21 × 21 mm

Ball pitch: 1.27 mm

Cofired: Al2O3

Optional: discrete capacitor mounting lands on top side of package for extra decoupling.

Figure 5-2. Mechanical Description Bottom View



5.1.2 Mechanical Up View

Figure 5-3. Isometric View

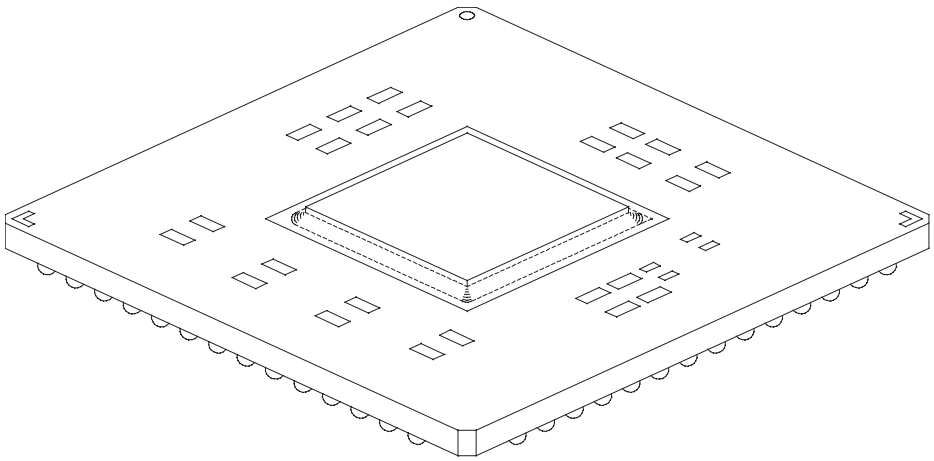


Figure 5-4. Package Top View

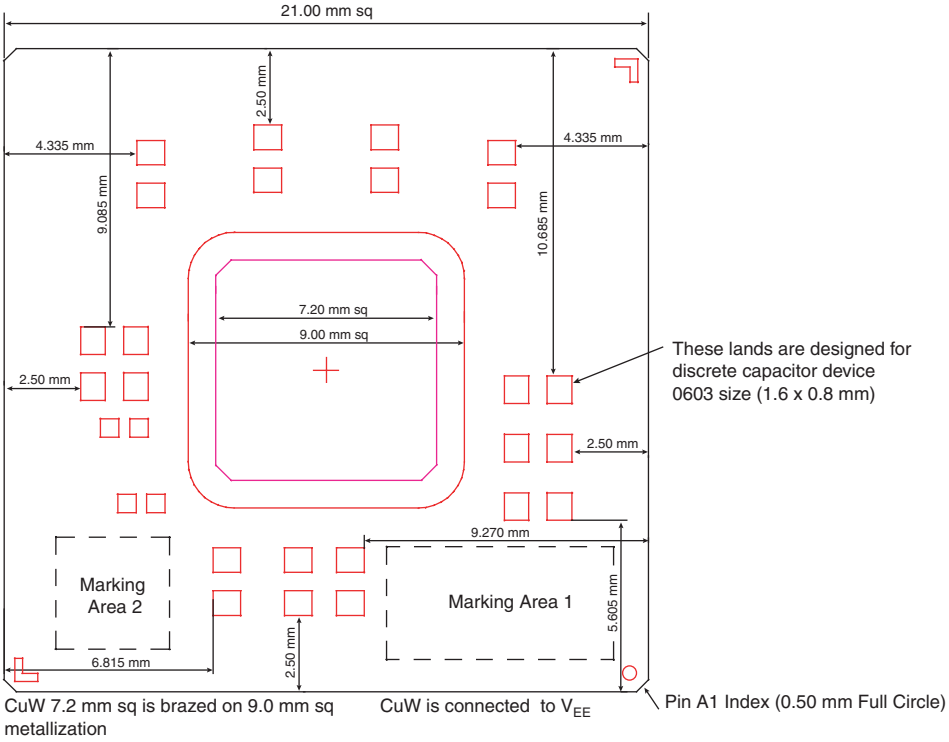
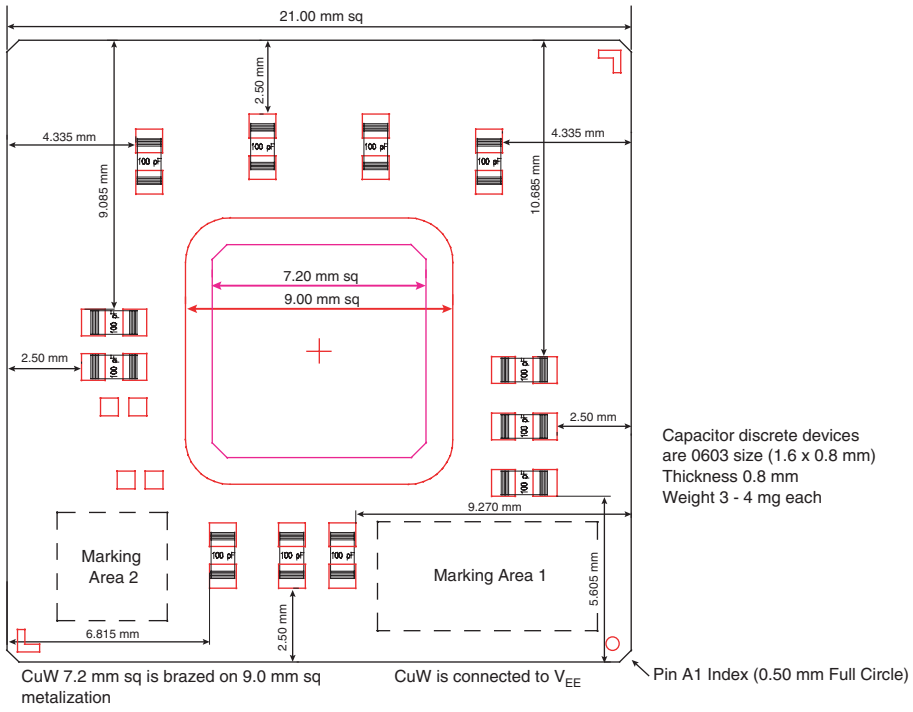


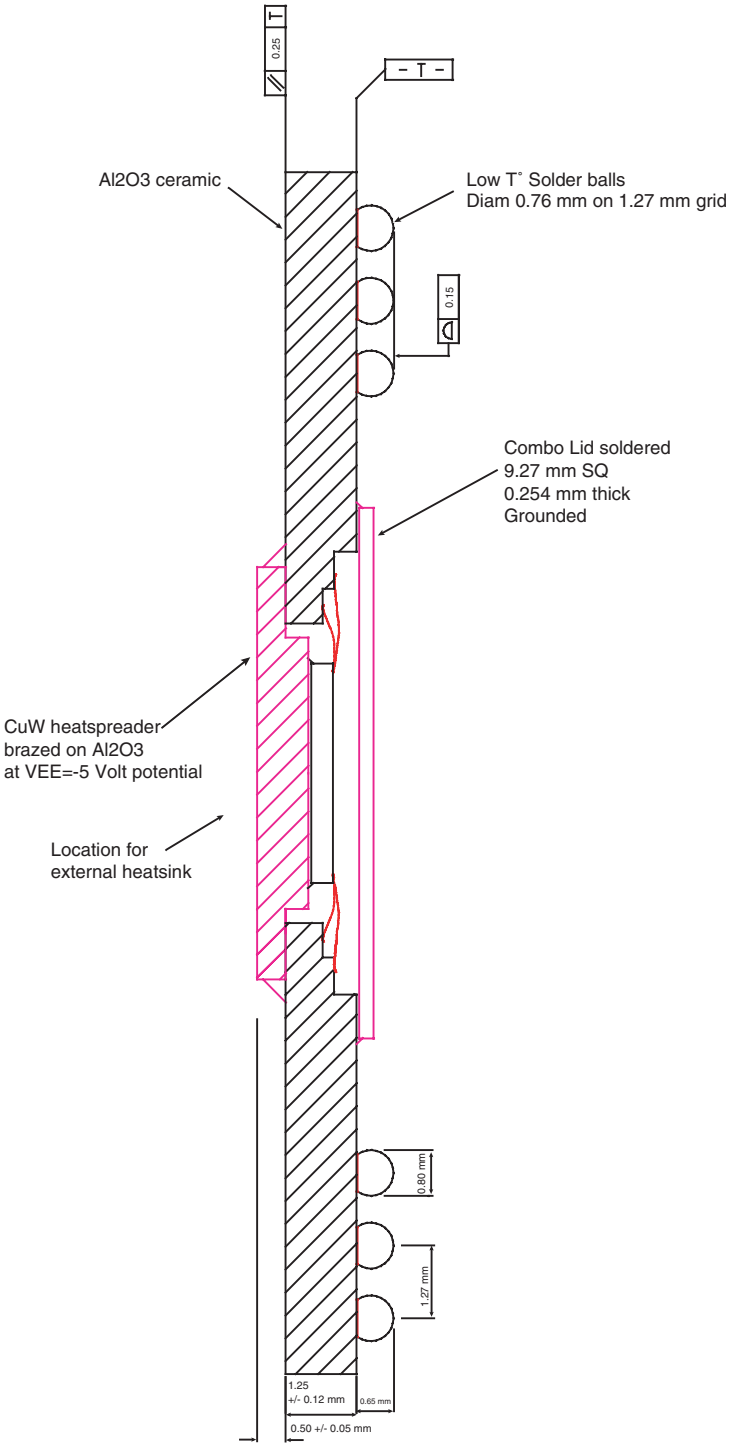
Figure 5-5. Package Top View with Optional Discrete Capacitors



Note: For additional decoupling of the power supplies, extra land capacitors have been foreseen as shown in this scheme. They are not needed if evaluation board decoupling recommendations are followed and if standard power supply are used (no switched power supply). Performance results of the device have proven to be equivalent with / without these capacitors.

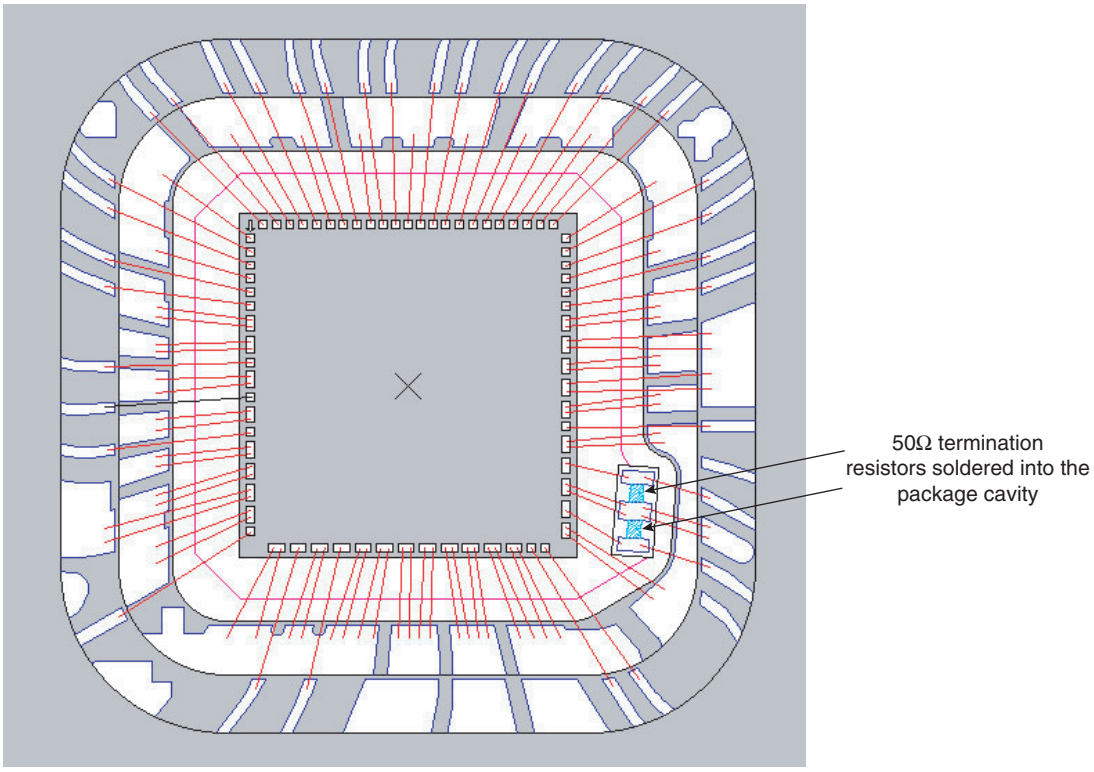
5.1.3 Cross Section

CBGA 152 21x21 mm Cross Section
10 bits/2.2 Gsps ADC. External heatsink required



5.1.4 CBGA 152 Cavity, Wirebonding and Resistor Pairs

Figure 5-6. CBGA 152 Cavity, Wirebonding and Resistor Pairs



5.2 Thermal and Moisture Characteristics

5.2.1 Dissipation by Conduction and Convection

The thermal resistance from junction to ambient RTH_{JA} is around 30°C/W. Therefore, to lower RTH_{JA} it is mandatory to use an external heatsink to improve dissipation by convection and conduction. The heatsink should be fixed in contact with the top side of the package (CuW heatspreader over Al2O3) which is at -5V. The heatsink needs to be electrically isolated; using an adequate low Rth electrical isolation.

Example:

The thermal resistance from case to ambient RTH_{CA} is typically 4.0°C/W (0 m/s air flow or still air) with the heatsink depicted in figure 1, of dimensions 50mm × 50mm × 22mm (respectively L × l × H). Global junction to ambient thermal resistance RTH_{JA} is:

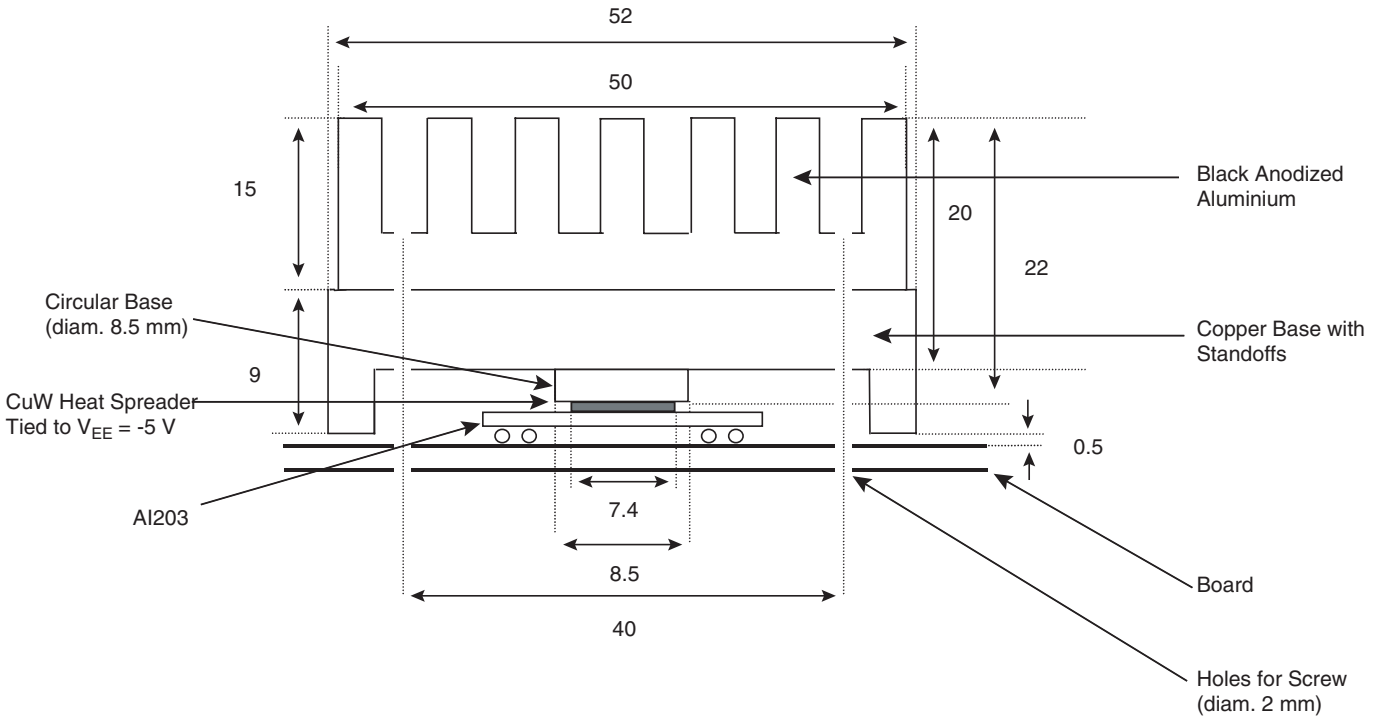
4.35°C/W RTH_{JC} +2.0°C/W thermal grease resistance +4.0°C/W RTH_{CA} (case to ambient) + = 0.35°C/W total (RTH_{JA}).

Assuming:

- Typical thermal resistance from junction to bottom of case RTH_{JC} is 4.35oC/Watt (Finite Element Method thermal simulation results).This value does not include thermal contact resistance between package and external heatsink (glue, paste, or thermal foil interface for example). As an example, use 2.0°C/W value for 50 µm thickness of thermal grease.

Note: Example of calculation of ambient temperature T_A max to ensure T_J max = 110°C:
Assuming RTH_{JA} = 10.35°C/W and Power dissipation = 4.6W, T_A max = T_J - (RTH_{JA} × 4.6W) = 110 -(10.35 × 4.6) = 62.39°C
T_A max can be increased lowering RTH_{JA} with adequate air flow (2 m/s, for example).

Figure 5-7. Black Anodized Aluminum Heatsink Glued on a Copper Base Screwed on Board (All Dimensions in mm).



Cooling system efficiency can be monitored using the temperature sensing diodes, integrated in the device.

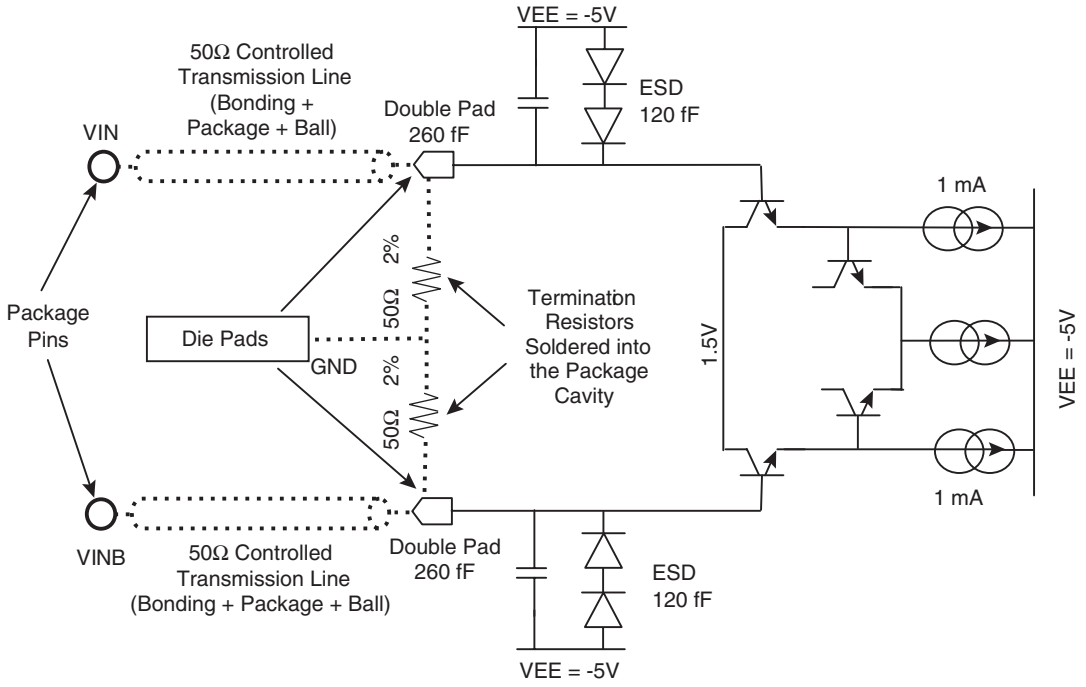
5.2.2 Thermal Dissipation by Conduction Only

When external heatsink cannot be used the relevant thermal resistance is thermal resistance from junction to bottom of balls:

$RTH_{J\text{-}Bottom\text{-}of\text{-}balls}$. Thermal path, in this case, is junction, then silicon, glue, CuW heatspreader, Al2O3 of package, and balls (Sn63Pb37). Finite Element Method (FEM) with thermal simulator lead to $RTH_{J\text{-}bottom\ of\ balls}$ = 12.3°C/Watt. This value assume pure conduction from junction to bottom of balls.(that is worst case, no radiation and no convection applied). With such assumption the $RTH_{J\text{-}\ Bottom\text{-}of\text{-}balls}$ is user independent. To complete thermal analysis, user must add the thermal resistance from top of board (on which is soldered the device) to ambient, which value is user dependent (type of board, thermal via, area covered by copper in each layer of the board, thickness, airflow or cold plate are parameters to consider).

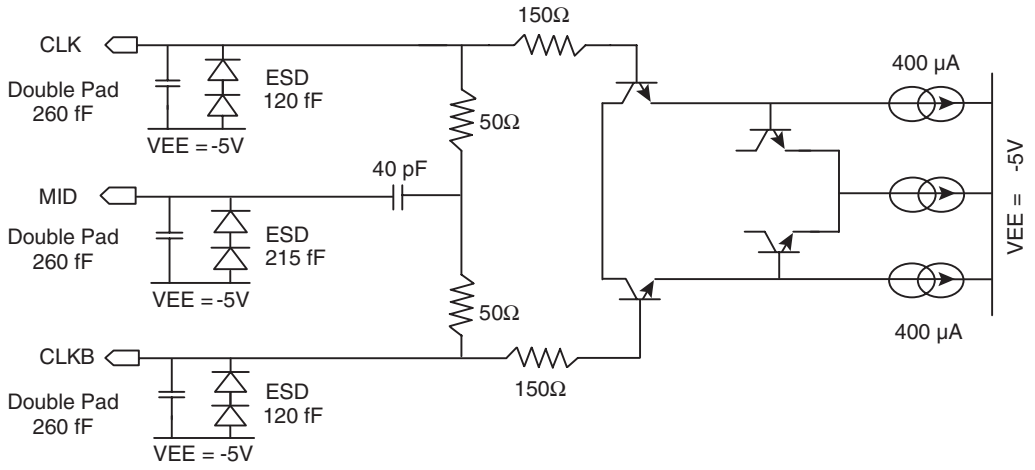
6. Equivalent Input/Output Schematics

Figure 6-1. Equivalent Analog Input Circuit and ESD Protection



Note: 100Ω termination mid point are located inside package cavity and DC coupled to ground.

Figure 6-2. Equivalent Analog Clock Input Circuit and ESD Protection



Note: 100Ω termination mid point are on chip and AC coupled to ground through a 40 pF capacitor.

Figure 6-3. Equivalent Data Output Buffer Circuit And ESD Protection

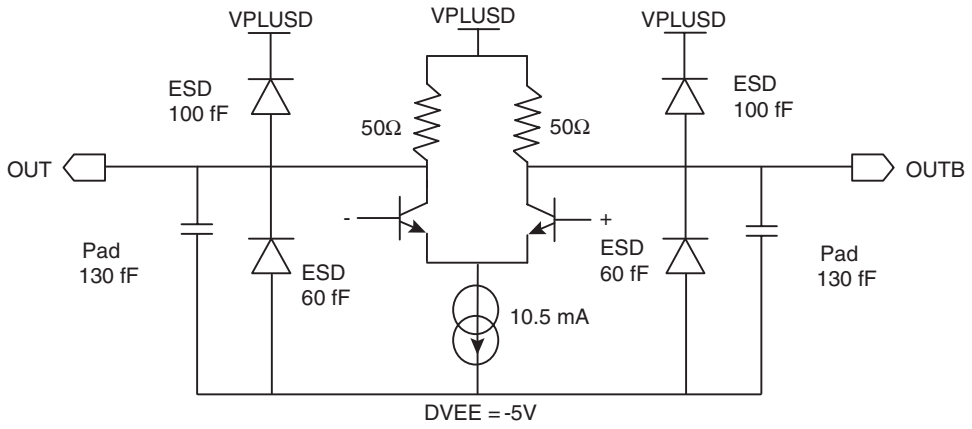


Figure 6-4. ADC Gain Adjust Equivalent Input Circuits and ESD Protection

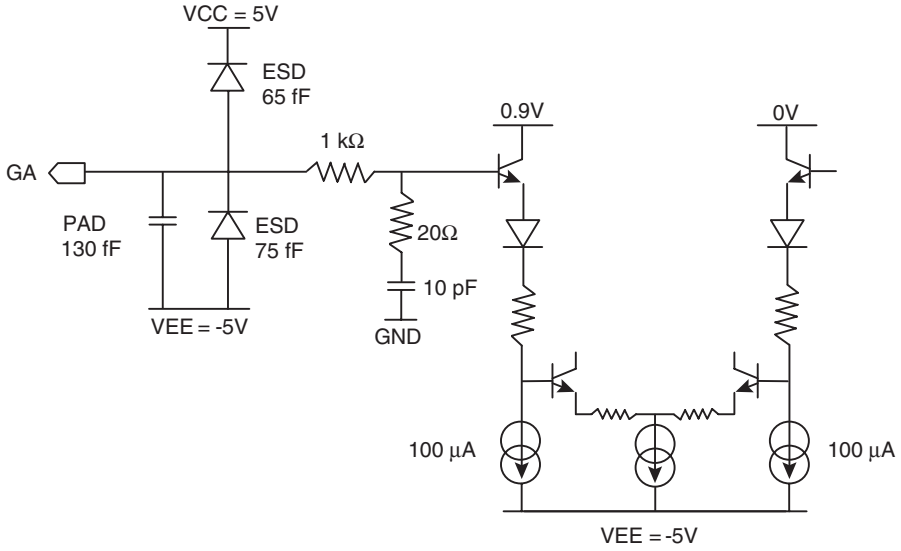


Figure 6-5. B/GB and PGEB Equivalent Input Schematics and ESD Protection

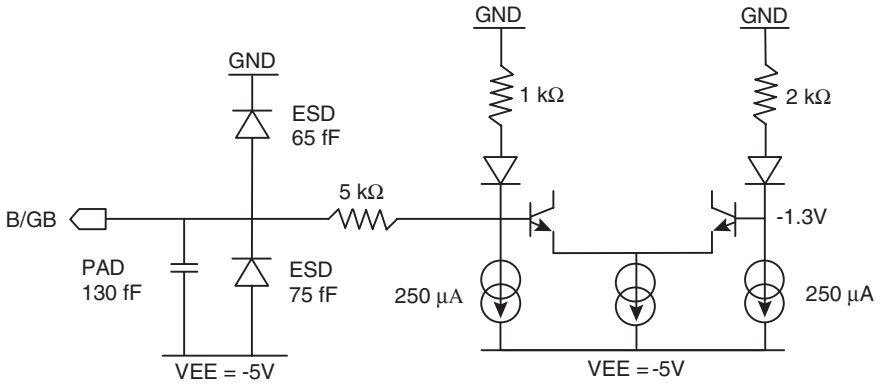


Figure 6-6. DRRB Equivalent Input Schematic and ESD Protection

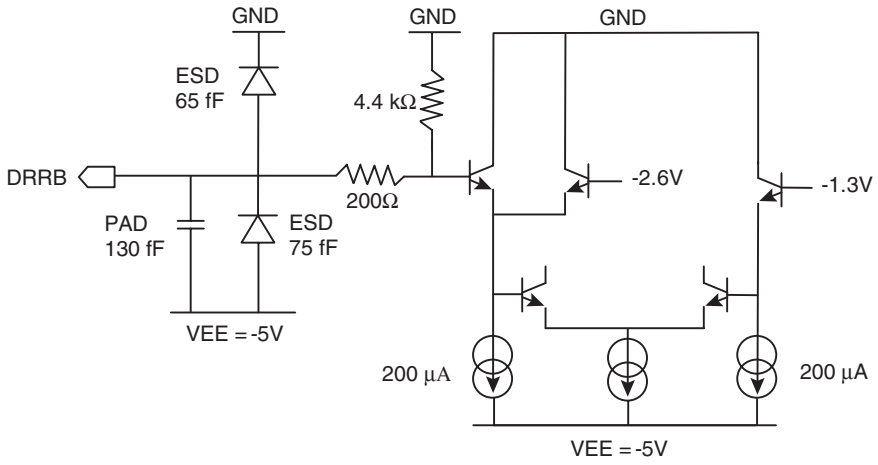
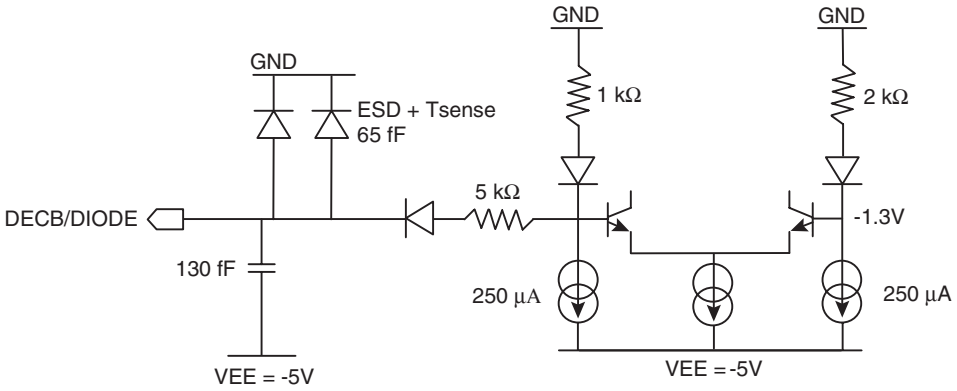


Figure 6-7. DECB/DIODE Equivalent Input Schematic and ESD Protection



7. Definition of Terms

Table 7-1. Definition of Terms

Term		Description
Fs max	Maximum Sampling Frequency	Sampling frequency for which ENOB < 6 bits
Fs min	Minimum Sampling frequency	Sampling frequency for which the ADC Gain has fallen by 0.5dB with respect to the gain reference value. Performances are not guaranteed below this frequency
BER	Bit Error Rate	Probability to exceed a specified error threshold for a sample at maximum specified sampling rate. An error code is a code that differs by more than ±4 LSB from the correct code
FPBW	Full Power Input Bandwidth	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at full-scale -1 dB (-1 dBF_S)
SSBW	Small Signal Input Bandwidth	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at full-scale -10 dB (-10 dBF_S)
SINAD	Signal-to-noise and Distortion Ratio	Ratio expressed in dB of the RMS signal amplitude, set to 1dB below full-scale (-1 dBF_S), to the RMS sum of all other spectral components, including the harmonics except DC
SNR	Signal-to-noise Ratio	Ratio expressed in dB of the RMS signal amplitude, set to 1dB below full-scale, to the RMS sum of all other spectral components excluding the twenty five first harmonics
THD	Total Harmonic Distortion	Ratio expressed in dB of the RMS sum of the first twenty five harmonic components, to the RMS input signal amplitude, set at 1 dB below full-scale. It may be reported in dB (i.e, related to converter -1 dB full-scale), or in dBc (i.e, related to input signal level
SFDR	Spurious Free Dynamic Range	Ratio expressed in dB of the RMS signal amplitude, set at 1dB below full-scale, to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic. It may be reported in dB (i.e., related to converter -1 dB full-scale), or in dBc (i.e, related to input signal level)
ENOB	Effective Number of Bits	$ENOB = \frac{SINAD - 1{\cdot}76 + 20\log\frac{A}{Fs/2}}{6{\cdot}02}$ Where A is the actual input amplitude and F_S is the full-scale range of the ADC under test
DNL	Differential Non-Linearity	The Differential non-linearity for an output code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic
INL	Integral Non-Linearity	The Integral non-linearity for an output code i is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all INL (i)
TA	Aperture Delay	Delay between the rising edge of the differential clock inputs (CLK,CLKB) (zero crossing point), and the time at which (VIN,VINB) is sampled

Table 7-1. Definition of Terms (Continued)

Term		Description
JITTER	Aperture Uncertainty	Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point
TS	Settling Time	Time delay to achieve 0.2% accuracy at the converter output when a 80% full-scale step function is applied to the differential analog input
ORT	Overvoltage Recovery Time	Time to recover 0.2% accuracy at the output, after a 150% full-scale step applied on the input is reduced to midscale
TOD	Digital Data Output Delay	Delay from the rising edge of the differential clock inputs (CLK,CLKB) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load
TDR	Data Ready Output Delay	Delay from the falling edge of the differential clock inputs (CLK,CLKB) (zero crossing point) to the next point of change in the differential data ready output (zero crossing) with specified load
TD1	Time Delay from Data Transition to Data Ready	General expression is TD1 = TC1 + TDR - TOD with TC = TC1 + TC2 = 1 encoding clock period
TD2	Time Delay from Data Ready to Data	General expression is TD2 = TC2 + TDR - TOD with TC = TC1 + TC2 = 1 encoding clock period
TC	Encoding Clock period	TC1 = Minimum clock pulse width (high) TC = TC1 + TC2TC2 = Minimum clock pulse width (low)
TPD	Pipeline Delay	Number of clock cycles between the sampling edge of an input data and the associated output data being made available, (not taking in account the TOD)
TRDR	Data Ready Reset Delay	Delay between the falling edge of the Data Ready output asynchronous Reset signal (DDRB) and the reset to digital zero transition of the Data Ready output signal (DR)
TR	Rise Time	Time delay for the output DATA signals to rise from 20% to 80% of delta between low level and high level
TF	Fall Time	Time delay for the output DATA signals to fall from 20% to 80% of delta between low level and high level
PSRR	Power Supply Rejection Ratio	Ratio of input offset variation to a change in power supply voltage
NRZ	Non Return to Zero	When the input signal is larger than the upper bound of the ADC input range, the output code is identical to the maximum code and the Out of Range bit is set to logic one. When the input signal is smaller than the lower bound of the ADC input range, the output code is identical to the minimum code, and the Out of range bit is set to logic one. (It is assumed that the input signal amplitude remains within the absolute maximum ratings)
IMD	Inter-Modulation Distortion	The two tones Inter-modulation distortion (IMD) rejection is the ratio of either input tone to the worst third order Inter-modulation products
NPR	Noise Power Ratio	The NPR is measured to characterize the ADC performance in response to broad bandwidth signals. When applying a notch-filtered broadband white-noise signal as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test
VSWR	Voltage Standing Wave Ratio	The VSWR corresponds to the ADC input insertion loss due to input power reflection. For example a VSWR of 1.2 corresponds to a 20 dB return loss (i.e. 99% power transmitted and 1% reflected)

8. AT84AS008 Application Information

8.1 Timing Information

8.1.1 Timing Value for AT84AS008

Timing values are defined in Section 3.3. Timing values are given at package inputs/outputs, taking into account package transmission line, bond wire, pad and ESD protections capacitance, and specified termination loads.

Evaluation board propagation delays in 50Ω controlled impedance traces are not taken into account. Apply proper derating values corresponding to termination topology.

8.1.2 Propagation Time Considerations

TOD and TDR Timing values are given from package pin to pin and do not include the additional propagation times between device pins and input/output termination loads. For the evaluation board, the propagation time delay is 6.1 ps/mm (155 ps/inch) corresponding to 3.4 dielectric constant (at 10GHz) of the RO4003 used for the board.

If a different dielectric layer is used (for instance Teflon), please use appropriate propagation time values. TD1 and TD2 do not depend on propagation times because they are differential data (See “Definition of Terms” on page 31.).

TD1 and TD2 are also the most straightforward data to measure, because it is differential: TD can be measured directly onto termination loads, with matched oscilloscope probes.

8.1.3 TOD-TDR Variation over Temperature

Values for TOD and TDR track each other over temperature (1 percent variation for TOD - TDR per 100 degrees Celsius temperature variation). Therefore TOD - TDR variation over temperature is negligible. Moreover, the internal (on chip) skews between each data TODs and TDR effect can be considered as negligible. Consequently, minimum values for TOD and TDR are never more than 100 ps apart. The same is true for the TOD and TDR maximum values.

However, external TOD - TDR values may be dictated by total digital data skews between every TODs (each digital data) and TDR: MCM board, bonding wires and output line length differences, and output termination impedance mismatches.

The external (on board) skew effect has not been taken into account for the specification of the minimum and maximum values for TOD - TDR.

8.1.4 Principle of Operation

The analog input is sampled on the rising edge of external clock input (CLK,CLKB) after TA (aperture delay). The digitized data is available after 4 clock periods latency (pipeline delay (TPD)), on clock rising edge, after typical propagation delay TOD. The Data Ready differential output signal frequency (DR, DRB) is half the external clock frequency, it switches at the same rate as the digital outputs. The Data Ready output signal (DR, DRB) switches on external clock falling edge after a propagation delay TDR.

If TOD = TDR, the rising edge (True-False) of the differential Data Ready signal is placed in the middle of the output data valid window. This gives maximum setup and hold times for external data acquisition.

A Master asynchronous reset input command DRRB (ECL compatible single-ended input) is available for initializing the differential Data Ready output signal (DR,DRB). This feature is man-

datory in certain applications using interleaved ADCs or using a single ADC with demultiplexed outputs. Without Data Ready signal initialization, it is impossible to store the output digital data in a defined order.

When used with AT84CS001 1:2/1:4 10 bit DMUX, it is not required to initialize the Data Ready, as this device can start on either clock edge.

8.2 Principle of Data Ready Signal Control by DRRB Input Command

8.2.1 Data Ready Output Signal Reset

The Data Ready signal is reset on falling edge of DRRB input command, on ECL logical low level (-1.8V). DRRB may also be tied to V_{EE} = -5V for Data Ready output signal Master Reset. So long DRRB remains at logical low level, (or tied to V_{EE} = -5V), the Data Ready output remains at logical zero and is independent on the external free running encoding clock.

The Data Ready output signal (DR,DRB) is reset to logical zero after TRDR.

TRDR is measured between the -1.3V point of the falling edge of DRRB input command and the zero crossing point of the differential Data Ready output signal (DR,DRB).The Data Ready Reset command may be a pulse of 1 ns minimum time width.

8.2.2 Data Ready Output Signal Restart

The Data Ready output signal restarts on DRRB command rising edge, ECL logical high levels (-0.8V).

DRRB may also be Grounded, or is allowed to float, for normal free running of the Data Ready output signal. The Data Ready signal restart sequence depends on the logical level of the external encoding clock, at DRRB rising edge instant:

1. The DRRB rising edge occurs when the external encoding clock input (CLK,CLKB) is low: the Data Ready output first rising edge occurs after half a clock period on the clock falling edge, after a delay time TDR = 360 ps already defined here above.
2. The DRRB rising edge occurs when the external encoding clock input (CLK,CLKB) is high: the Data Ready output first rising edge occurs after one clock period on the clock falling edge, and a delay TDR = 360 ps.

Consequently, as the analog input is sampled on the clock rising edge, the first digitized data corresponding to the first acquisition (N) after Data Ready signal restart (rising edge) is always strobed by the third rising edge of the data ready signal.

The time delay (TD1) is specified between the last point of a change in the differential output data (zero crossing point) to the rising or falling edge of the differential Data Ready signal (DR,DRB) (zero crossing point).

Note: For normal initialization of Data Ready output signal, the external encoding clock signal frequency and level must be controlled.
It is reminded that the minimum encoding clock sampling rate for the ADC is 150 MSPS, due to internal T/H droop rate. Consequently the clock cannot be stopped without corrupting the current held data.

8.2.3 Timing Diagram with Data Ready Reset

Figure 8-1. AT84AS008 Timing Diagram (2 Gsps Clock Rate) – Data Ready Reset, Clock Held at Low Level

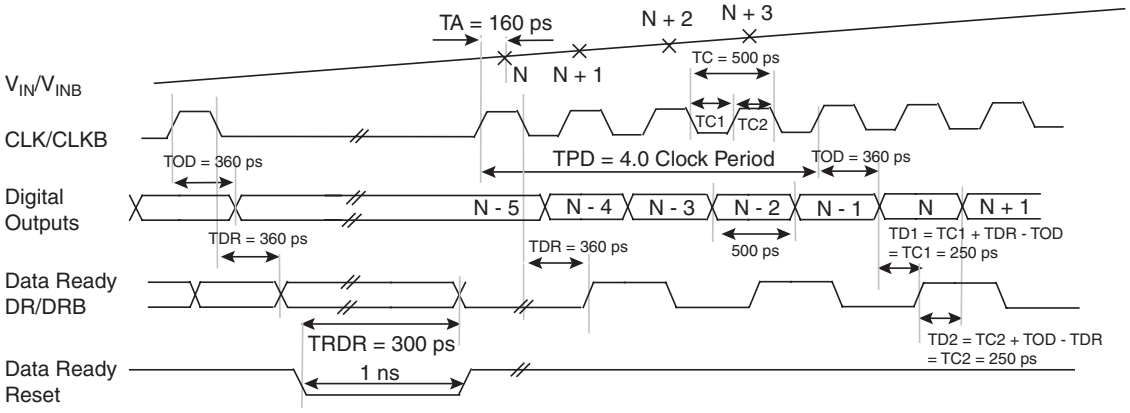
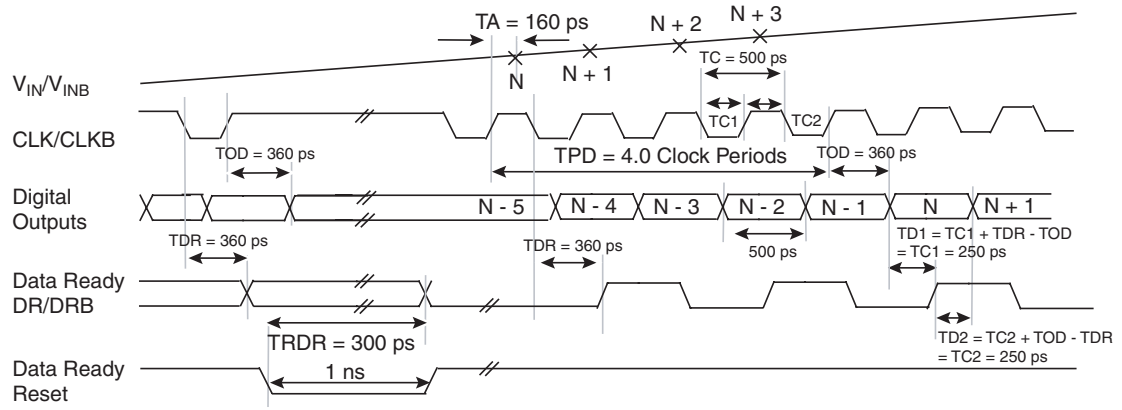


Figure 8-2. AT84AS008 Timing Diagram (2 Gsps Clock Rate) - Data Ready Reset, Clock Held at High Level



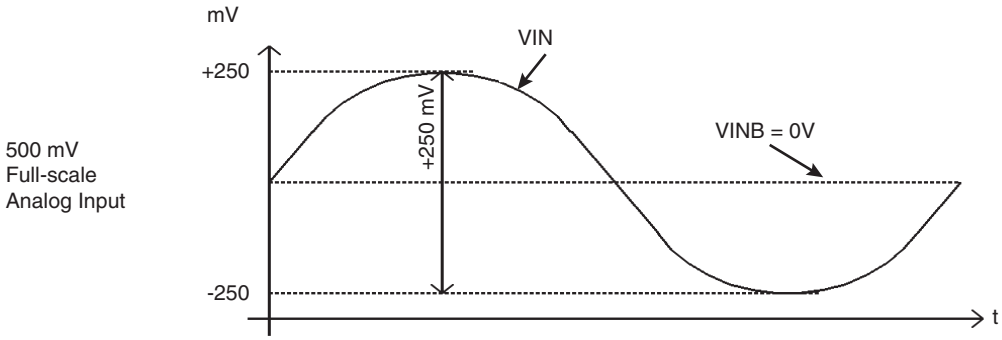
8.3 Analog Inputs (VIN/VINB)

8.3.1 Static Issues: Differential Versus Single-ended (Full-scale Inputs)

The ADC front-end Track and Hold differential preamplifier has been designed in order to be entered either in differential mode or single-ended mode, up to maximum operating speed (2.2 Gsps), without affecting dynamic performances (does not request a single to differential balun).

In single-ended input configuration, the in-phase full-scale input amplitude is 0.5V peak-to-peak, centered on 0V. (or -2 dBm into 50Ω).

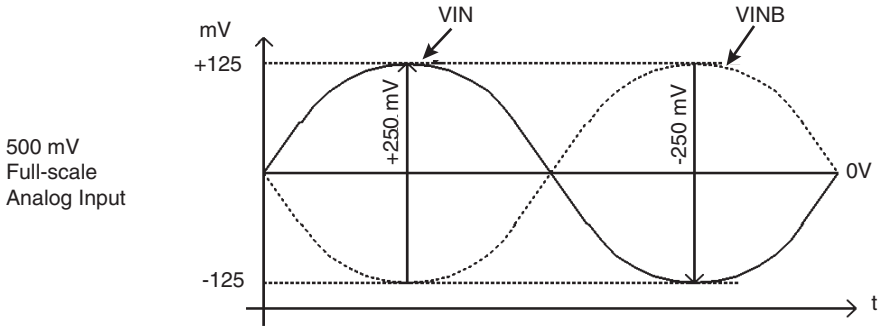
Figure 8-3. Typical Single-ended Analog Input Configuration (Full-scale)



The analog input full-scale range is 0.5V peak to peak (Vpp), or -2 dBm into the 50Ω (100Ω differential) termination resistor.

In differential mode input configuration, that means 0.25V on each input, or ±125 mV around zero volt. The input common mode is ground.

Figure 8-4. Differential Inputs Voltage Span (Full-scale)



8.3.2 Dynamic Issues: Input Impedance and VSWR

The AT84AS008 analog input features a 100Ω (±2%) differential input impedance (2 × 50Ω // 0.3 pF): Each analog input (VIN,VINB) is terminated by 50Ω single-ended (100Ω differential) resistors (±2% matching) soldered into the package cavity. The ADC package Analog Inputs transmission lines feature a 50Ω controlled impedance. Each single-ended die input pad capacitance (taking into account ESD protection) is 0.3 pF. This leads to a global input VSWR (including ball, package and bounding) of less than 1.2 from DC up to 2.5 GHz.

8.4 Clock Inputs (CLK/CLKB)

The AT84AS008 clock inputs are designed for either single-ended or differential operation. The AT84AS008 clock inputs are on- chip 100Ω (2 × 50Ω) differentially terminated. Termination mid point is AC coupled to ground through 40 pF on chip capacitor. Therefore either ground or different common modes could be used (ECL, LVDS).

However logic ECL or LVDS square wave clock generators are not recommended because of poor jitter performances.

Furthermore, the propagation times of the biasing tees used to offset the common mode voltage to ECL or LVDS levels may not match. A very low phase noise (low jitter) sinewave input signal should be used for enhanced SNR performance, when digitizing high frequency analog inputs.

Typically, using a sinewave oscillator featuring -135 dBc/Hz phase noise, at 20 KHz from carrier, a global jitter value (including ADC + generator) of less than 200 fs RMS has been measured. If clock signal frequency is at fixed rates, it is recommended to narrow band filter the signal to improve jitter performance.

Note: The clock input buffer 100Ω termination load is on chip, mid point AC coupled (40pF) to chip ground plane, whereas the analog input buffer 100Ω termination is soldered inside package cavity, mid point DC coupled to package ground plane. Therefore, driving the analog input in single ended does not perturb the chip ground plane, (since termination mid point is connected to package ground plane).

But driving the clock input in single ended will perturb the chip ground plane, (since termination mid point is AC coupled to chip ground plane). Therefore, it is required to drive the clock input in differential, for minimum chip ground plane perturbation (4 dBm max operating recommended). Typical clock input power is 0 dBm. The minimum operating clock input power is -4 dBm (equivalent to 250 mV minimum swing amplitude), to avoid SNR performances degradations linked to clock signal slew rate. A single to differential balun with sqrt (2) ratio may be used (featuring 50Ω input impedance with 100Ω differential termination).

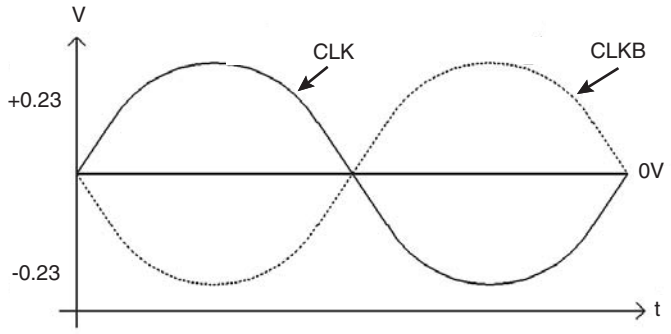
For instance:

- 4 dBm is equivalent to 1 Vpp into 50Ω and 1.4 Vpp into 100Ω termination (secondary)
- 0 dBm is equivalent to 0.632 Vpp into 50Ω and 0.632 × sqrt (2) = 0.894 Vpp into 100Ω termination (secondary), ±0.226V each clock input

Recommended clock inputs common mode is ground.

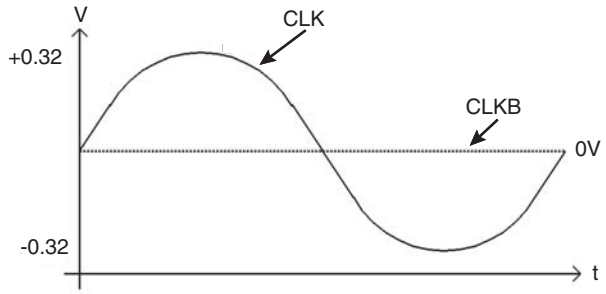
8.4.1 Differential Clock Inputs Voltage Levels (0 dBm Typical)

Figure 8-5. Differential Clock Inputs (Ground Common Mode): Recommended



8.4.2 Equivalent Single-ended Clock Inputs Voltage Levels (0 dBm Typical)

Figure 8-6. Single-ended Clock Input (Ground Common Mode)



8.5 Noise Immunity Information

Circuit noise immunity performance begins at design level.

Efforts have been made on the design in order to make the device as insensitive as possible to chip environment perturbations resulting from the circuit itself or induced by external circuitry (cascode stages isolation, internal damping resistors, clamps, internal on chip decoupling capacitors.)

Furthermore, the fully differential operation from analog input up to the digital outputs provides enhanced noise immunity by common mode noise rejection. Common mode noise voltage induced on the differential analog and clock inputs will be cancelled out by these balanced differential amplifiers.

Moreover, proper active signals shielding has been provided on the chip to reduce the amount of coupled noise on the active inputs: The analog inputs and clock inputs of the TS83102G0B device have been surrounded by ground pins, which must be directly connected to the external ground plane.

8.6 Digital Outputs: Termination and Logic Compatibility

Each single-ended output of the AT84AS008 differential output buffers are internally 50Ω terminated, and feature a 100Ω differential output impedance. The 50Ω resistors are connected to the V_{PLUSD} digital power supply. The AT84AS008 output buffers are designed to drive 50Ω controlled impedance lines properly terminated by a 50Ω resistor. A 10.5 mA bias current flowing alternately into one of the 50Ω resistors when switching ensures a 0.25V single-ended voltage drop across the resistor (0.5V differential)

Each single-ended output transmission line length must be kept identical (keep < 3 mm). Mismatches in the differential line lengths may cause output differential common mode variation.

It is recommended to bypass the midpoint of the differential 100Ω termination with a 47 pF capacitor to avoid common mode perturbation in case of slight mismatch in the differential output line lengths.

See recommended-termination scenarios here below.

Note: Since output buffers feature 100Ω differential output impedance, it is possible to drive directly high input impedance storing registers, without terminating the 50Ω transmission lines. In time domain, this means that the incident wave will reflect at the 50Ω transmission line output and travel back to the 50Ω data output buffer. Since the buffer output impedance is 50Ω, no back reflection will occur and output swing will be doubled.

V_{PLUSD} Digital Power Supply Settings:

- For differential ECL digital output levels: V_{PLUSD} should supplied with -0.8V (or connect it to ground via a 5Ω resistor to ensure the -0.8V voltage drop).
- For LVDS digital output logic compatibility, V_{PLUSD} should be tied to 1.45V (±75mV).

8.6.1 ECL differential output termination configurations

Figure 8-7. 50Ω Terminated Differential Outputs (Recommended)

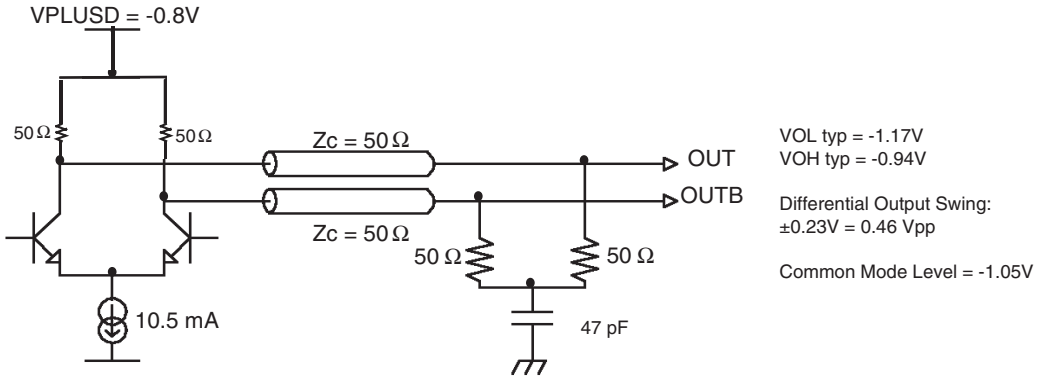
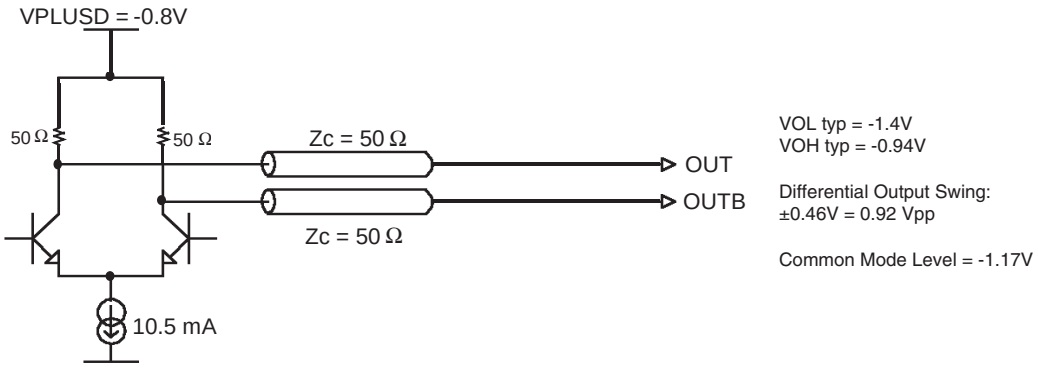


Figure 8-8. Unterminated Differential Outputs (Optional)



8.6.2 LVDS Differential Output Loading Configurations

Figure 8-9. 50Ω Terminated Differential Outputs

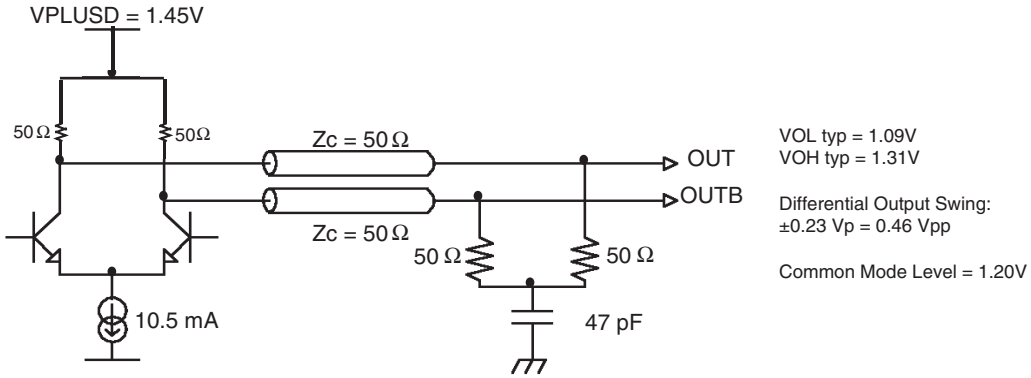
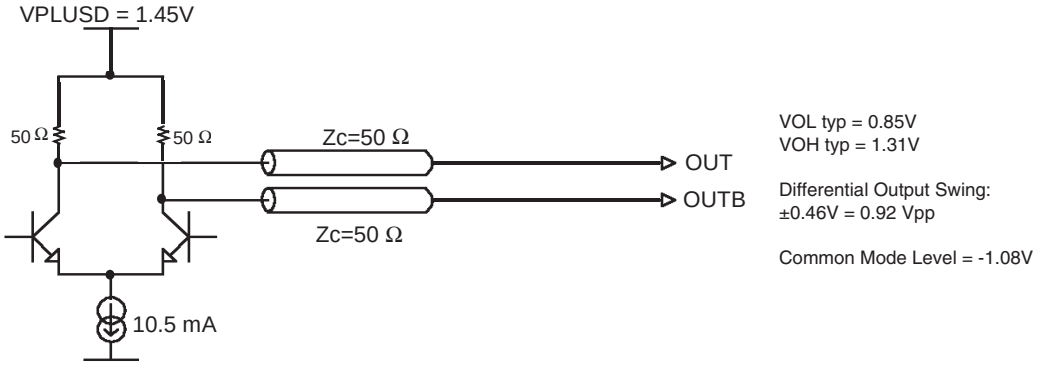
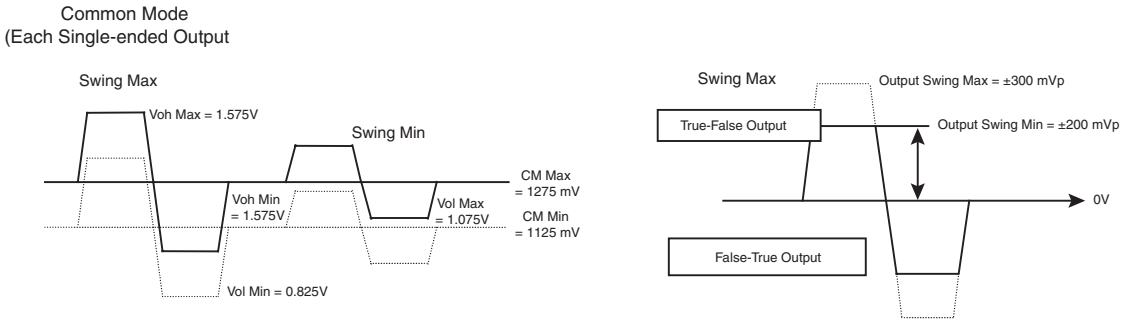


Figure 8-10. Unterminated Differential Outputs (Optional)



8.6.3 LVDS Logic Compatibility

LVDS FORMAT (cf IEEE Std 1596.3- 1994): 1125mV< Common mode<1275mV and 250mV< Output swing< 400mV.



8.7 ADC Main Functions

8.7.1 Out of Range Bit (OR/ORB)

It goes to logical high state when the input exceeds the positive full-scale or falls below the negative full-scale. When the analog input exceeds the positive full-scale, the digital outputs remain at high logical state, with (OR,ORB) at logical one. When the analog input falls below the negative full-scale, the digital outputs remain at logical low state, with (OR,ORB) at logical one again.

8.7.2 Bit Error Rate (BER)

The AT84AS008 internal regeneration latches indecision (for inputs very close to latches threshold) may produce errors in the logic encoding circuitry and leading to large amplitude output errors.

This is due to the fact that the latches are regenerating the internal analog residues into logical states with a finite voltage gain value (Av) within a given positive amount of time D(t):
$Av = \exp(D(t)/\tau)$, with τ the positive feedback regeneration time constant.

The AT84AS008 has been designed for reducing the probability of occurrence of such errors to 10^{-12}. A standard technique for reducing the amplitude of such errors down to ±1 LSB consists in setting the digital output data in gray code format. Though the AT84AS008 has been designed for featuring a Bit Error Rate of 10^{-12} with a binary output format.

8.7.3 Gray or Binary Output data format select

It is possible for the user to choose between the binary or gray output data format, in order to reduce the amplitude of such errors when occurring, by storing gray output codes.

Digital Data format selection:

BINARY output format if B/GB is floating or GND.

GRAY output format if B/GB is connected to V_{EE}.

8.7.4 Pattern Generator Function

The Pattern Generator function (enabled by connecting pin A9 PGEB to ECL low or to V_{EE} = -5V) allows to check rapidly the ADC operation thanks to a checker board pattern delivered internally to the ADC. Each output bit of the ADC should toggle from 0 to 1 successively, giving sequences such as 0101010101 (strobed by falling edge of DR) and 1010101010 (strobed by rising edge of DR) every 2 clock cycles.

8.7.5 DECB/DIODE: Junction Temperature Monitoring and Output Decimation Enable

The DECB/DIODE pin is provided for both decimation function enable and die junction temperature monitoring.

When set to ECL low or V_{EE} = -5V, the ADC runs in decimation by 32 mode (1 data out of 32 is output from the ADC, thus reducing the data rate by 32).

When the DECB/DIODE pin is left floating or ECL high, then the ADC is said to be in *normal* mode of operation (output data are not decimated) and can be used for die junction temperature monitoring only.

If the user does not intend to use the die junction temperature monitoring function, the DECB/DIODE pin (A10) has to be left either floating or connected to ground.

The decimation function can be used for debug of the ADC at initial stages. This function indeed allows to reduce the ADC output rate by 32, thus allowing for a quick debug phase of the ADC at max speed rate and is compatible with industrial testing environment.

When active, this function makes the ADC output only 1 out of 32 data, thus resulting in a data rate which is 32 times slower than the clock rate.

Note: the ADC decimation test mode is different from the pattern generator function, which can be used to check the ADC outputs.

8.7.6 External Configurations Description

Because of the use of 1 internal diode-mounted transistor (used for junction temperature monitoring), the user has to implement external head-to-tail protection diodes to avoid potential reverse currents flows which may damage the internal diode component.

Two external configurations are possible:

Configuration 1: allowing both junction temperature monitoring and output data decimation.

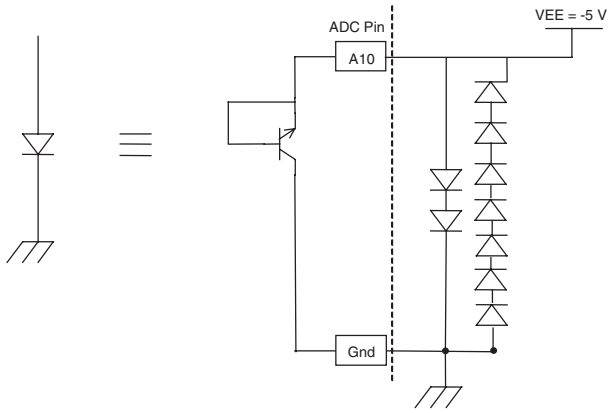
Configuration 2: allowing junction temperature monitoring only.

Configuration 1: allowing both Junction temperature monitoring and output data decimation.

This external configuration allows to apply the requested levels to activate output data decimation (ECL low or V_{EE} = -5V) and at the same time monitor the junction temperature diode (this explains why seven protection diodes are needed in the other direction, as described in the following figure).

Figure 8-11. Recommended Diode pin Implementation allowing for both die junction temperature monitoring function and Decimation mode.

Figure 8-12. Diode Pin Implementation for Decimation Activation



Configuration 2: junction temperature monitoring only (in this mode ADC decimation cannot be activated).

Note: In preliminary specification e2v recommended the use of 2 × 3 head-to-tail protection diodes. Final updated configuration is described in figure 19 here below.

Figure 8-13. Diode Pin implementation of Die Junction Temperature Monitoring Function Only

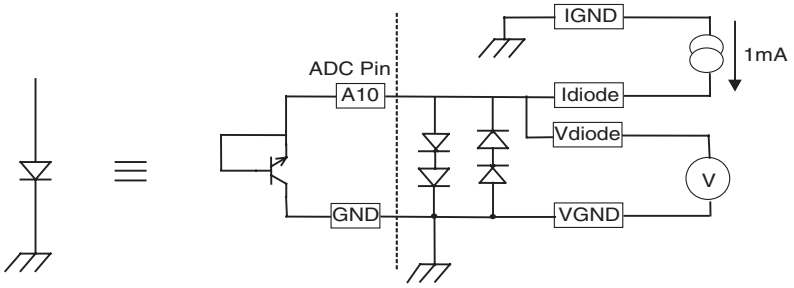
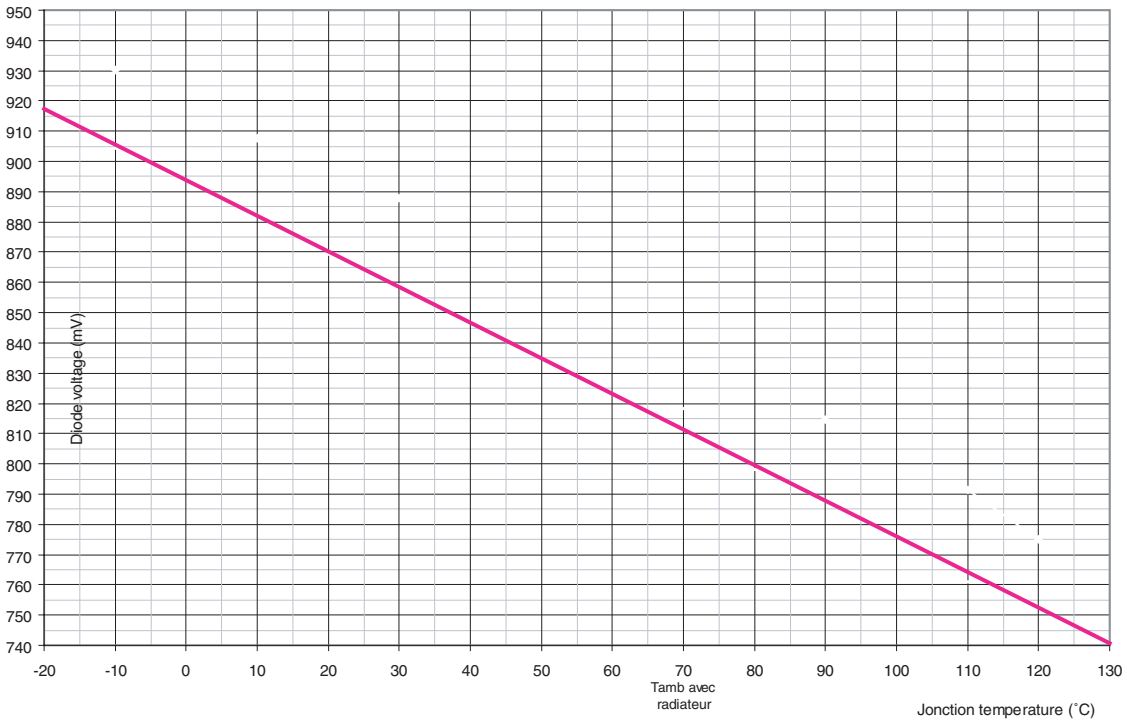


Figure 8-14. Junction Temperature Diode Transfer Function

The forward voltage drop, (VDIODE) across diode component, versus junction temperature, (including chip parasitic resistance), is given below (IDIODE = 1 mA):

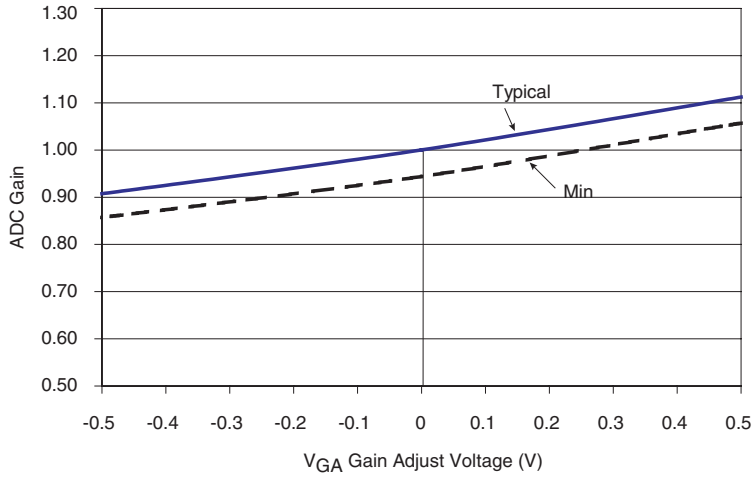


Note: The operating die junction temperature must be kept below 125°C, to ensure long term device reliability.

8.7.7 ADC Gain Control

The ADC gain is adjustable by the means of the pin R9 of CBGA package.

The gain adjust transfer function is given below:



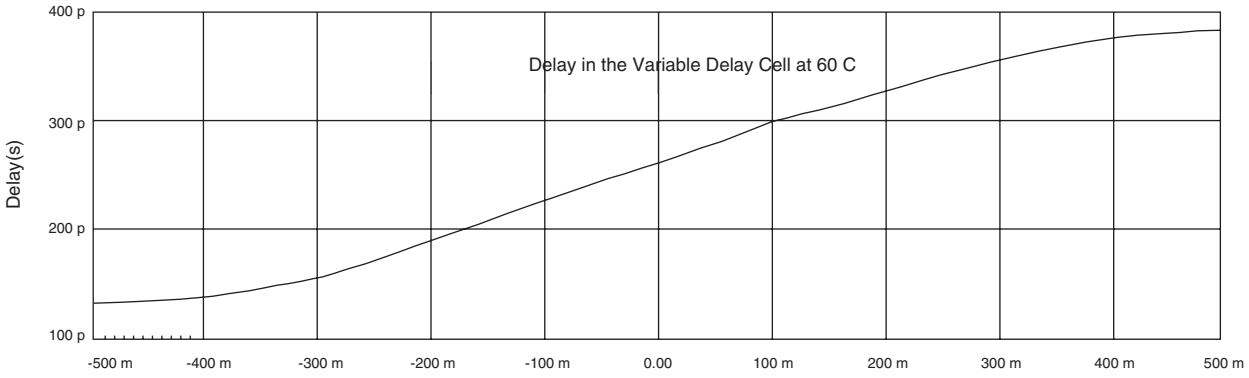
8.7.8 Sampling Delay Adjust

Sampling delay adjust (SDA pin) allows to fine tune the sampling ADC aperture delay TAD around its nominal value (160 ps). This functionality is enabled thanks to the SDAEN signal, which is active when tied to V_{EE} and inactive when tied to GND.

This feature is particularly interesting for interleaving ADCs to increase sampling rate.

The variation of the delay around its nominal value as a function of the SDA voltage is shown in the following graph (simulation result):

Figure 8-15. Typical Tuning Range is ±120 ps for Applied Control Voltage Varying Between -0.5V to 0.5V on SDA Pin



Note: The variation of the delay in function of the temperature is negligible.

9. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
AT84AS008CGL	CBGA152	Commercial *C* grade 0°C < Tc, Tj < 90°C	Standard	
AT84AS008VGL	CBGA152	Industrial *V* grade -20°C < TC, TJ < 110°C	Standard	
AT84AS008GL-EB	CBGA152	Ambient	Prototype	Evaluation board (delivered with a heat sink)

10. Appendix

Datasheet Status

Status		Validity
Objective specification	This datasheet contains target and goal specifications for discussion with the client and application validation	Before design phase
Target specification	This datasheet contains target and goal specifications for product development	Valid during the design phase
Preliminary specification Alpha-site	This datasheet contains preliminary data. Additional data may be published an a later date and could include simulation results	Valid before the characterization phase
Preliminary specification Beta-site	This datasheet also contains characterization results	Valid before the industrialization phase
Product specification	This datasheet contains final product specifications	Valid for production purposes
Limiting Values		
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability		
Application Information		
Where application information is given, it is advisory and does not form part of the specification		

10.1 Life Support Applications

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. e2v customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify e2v for any damages resulting from improper use or sale.

e2v

5404A–BDC–11/06